Reference Design and Implementation

Jupiter-F2
(Flash, EEPROM, ROM-only)

GPS Receiver Module

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1 Introduction

The Jupiter-F2 is an 11mm by 11mm integrated GPS receiver module using SiRFstar IV technology. This document expands upon the data sheet(s) to highlight particular areas to allow the hardware engineer to achieve a successful design implementation.

2 Powering the J-F2

2.1 1.8V Supply Voltage

Unlike older GPS receiver modules, the J-F2 requires a single always on supply voltage of 1.8 volts. Rather than having a "split" power supply design of main and backup, the J-F2 manages all of its power modes internally. The J-F2 will normally power up into the lowest power "hibernate" state upon initial application of power. Upon pulsing the ON-OFF signal, the J-F2 will transition to the "operate" state. Pulsing the ON-OFF signal a second time will transition the J-F2 back into the "hibernate" state.

The current power state of the J-F2 can be determined by monitoring the "SYSTEM-ON" signal. A logic low indicates the module is in "hibernate", whereas logic high indicates the module is in "operate" state.

If the 1.8 volt DC supply is removed from the J-F2 (regardless of power state) it will lose current RTC time and will lose the contents of the internal SRAM. To prevent improper startup, once power is removed, keep the power removed for approximately 10 seconds so the internal SRAM contents can clear reliably.

The J-F2 monitors the 1.8 volt supply and issues an internal hardware reset if the supply drops below 1.7 volts. This reset protects the flash memory from accidental writes during a power down condition. However, the reset also clears the RTC time and forces the J-F2 into a hibernate state.

To prevent this, the 1.8 volt supply must be regulated to be within ±50 mV of nominal voltage inclusive of load regulation and power supply noise and ripple. Noise and ripple outside of these limits can affect GPS sensitivity and also risk tripping the internal voltage supervisors, thereby shutting down the J-F2 unexpectedly. Regulators with very good load regulation are strongly recommended along with adequate power supply filtering to prevent power supply glitches as the J-F2 transitions between power states.

Aluminum electrolytic capacitors are not recommended at the input to the J-F2 due to their high ESR. Tantalum capacitors are recommended with a minimum value of 10uF in parallel with a 0.1uF ceramic capacitor. Ceramic capacitors alone can be used, but make sure the LDO is stable with such capacitors tied to the output.

As mentioned above, power supply voltage, noise and ripple must be between 1.75V and 1.85V for all frequencies up to 3 MHz. Above 3MHz, the noise and ripple component must not exceed ±16mV. To help meet these requirements, a separate LDO for the J-F2 is suggested.

2.2 Implementing Pseudo Battery Back-up

As mentioned above, the J-F2 cannot tolerate removal of the 1.8 volt supply without losing RTC time and SRAM data. The main supply voltage can be switched to a backup supply external to the J-F2 provided the receiver is allowed time to enter the hibernate state. This can be accomplished by monitoring the status of the SYSTEM-ON line, which will be low whenever the J-F2 is in the hibernate state. At this point, the main supply can be safely switched over to the backup supply provided the 1.8 volt supply stays within specification. Similarly, the switch back to the main supply must occur prior to placing the J-F2 into full power mode.

If the product containing the J-F2 needs to support abrupt removal of power, then the module will require a cold start reset upon reapplication of power.

2.3 Understanding ON-OFF and SYSTEM-ON

The J-F2 power is controlled by a state machine. This state machine is clocked by the internal 32 KHz RTC clock, and is controlled by internal signals as well as the ON-OFF and NRESET signals. The SYSTEM-ON signal reflects the power state of the J-F2, logic low for hibernate mode, and logic high for full power mode.

When power is first applied to the J-F2, the internal RTC must start up before the state machine can begin operating. ON-OFF signals applied before the state machine is ready for them will be ignored. The J-F2 signals the readiness to accept ON-OFF signals by outputting a pulse on the SYSTEM-ON line after power is first applied. This pulse is only output upon application of power, and is not output when the receiver is in hibernate or full power mode.

The ON-OFF signal is normally low. When it transitions high, it should stay high for a time equivalent to a minimum of 3 RTC clock cycles. The signal may then transition low and remain low until the next change in power state is desired.

The J-F2 powers up directly into the hibernate state. It is possible to have the module automatically transition to the full power state by tying the SYSTEM-ON output to the ON-OFF input. GPIO8 should also be tied high, which changes the ON-OFF signal to just an ON signal. However, this implementation eliminates the possibility of using the ON-OFF signal to change power states. If the serial command to place the J-F2 in hibernate mode is issued, the module will transition to the hibernate state with no way other than removal and reapplication of power (with resulting RTC and SRAM data loss) to force the module to power up. For some users, this may be all that is required if time and data retention are not important during a power down situation.

A single OR gate with one input being SYSTEM-ON and the other being an external pulse will allow the module to be turned back on with a suitable pulse, but it will not be possible to use a second pulse as it is blocked with the SYSTEM-ON signal. The only option to place the module in hibernate state is to issue the serial command.

If full ON-OFF control is desired along with having SYSTEM-ON auto-start the receiver, then additional logic is needed to detect the first falling edge of SYSTEM-ON and using this detection to gate off the SYSTEM-ON signal to the ON-OFF signal.

If GPIO8 is pulled to logic 1, then the ON-OFF input is modified to be just an ON input. It would not be possible to place the J-F2 into hibernate by pulsing ON-OFF in this case. This feature could be useful by inverting the RX input and applying it to the ON-OFF input, thus causing the receiver to enter full power mode when a serial message is received. Of course, the first message would not be processed as the receiver has not fully woken up.

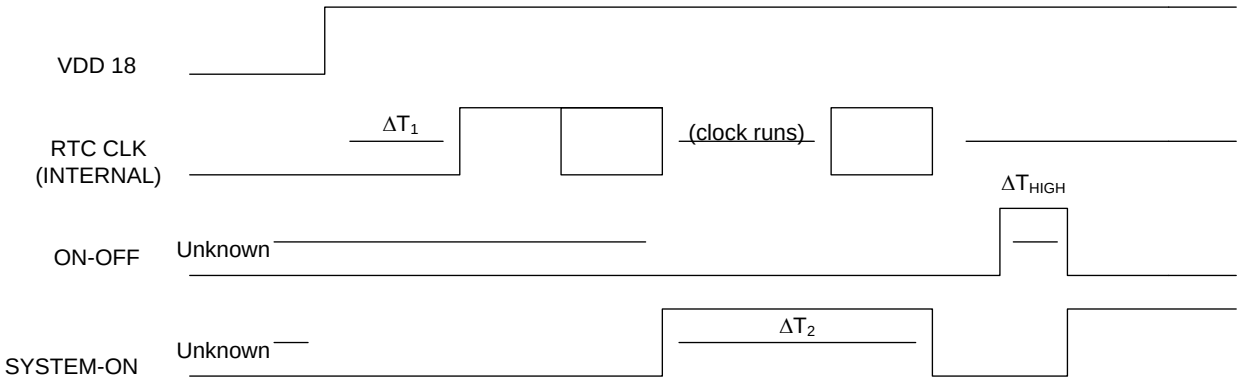

Figure 1 – Initial Application of Main Power

Timed Parameter	Prior Event/State	Symbol	Min	Typ	Max	Unit
RTC startup time	First power applied	ΔT_1	0	299	1000	ms
FSM Ready pulse	RTC running	ΔT_2		10		T_{RTC}
Min ON-OFF high		ΔT_{HIGH}	3			T_{RTC}
T_{RTC} is equivalent to one RTC (32.678KHz) clock cycle.						

Table 1 – Power State Timing

2.4 Reset Design Details

The J-F2 NRESET pin is normally connected to a 0.33uF ceramic capacitor. The J-F2 will generate an internal reset as appropriate. No external reset signal needs to be applied to the J-F2.

If an external reset is desired, the signal must be either open collector or open drain without any form of pullup. Do not pull this line high with either a pullup or a driven logic one. When this line is pulled low, the J-F2 will immediately drop into hibernate mode with some loss of data.

When the external reset is released, the J-F2 will go through its normal power up sequence provided the VCC_IN supply is within specifications.

3 Updating the Firmware: J-F2 Module (ONLY)

During normal operations, the BOOT signal should be tied to ground through a 100K pulldown resistor. This will ensure the GPS module executes the code out of the internal flash memory.

However, if the internal flash memory needs to be updated, the following steps should be performed to place the J-F2 module into a state suitable for programming the internal flash memory.

1. Either remove all power to the module, or force the module into hibernate state by pulsing the ON-OFF signal. Verify the state of the module by monitoring the SYSTEM-ON signal.
2. Pull the BOOT signal high through a 10K pull up resistor to +1.8 volts.
3. Apply main power if not already applied.
4. Pulse the ON-OFF signal to place the J-F2 module into BOOT mode.
5. Run the software utility to re-flash the J-F2 module. Clearing the entire flash memory is strongly recommended prior to programming.
6. Upon successful completion of re-flashing, remove main power to the module for a minimum of 10 seconds.
7. Pull the BOOT signal low through a 100K pull down resistor to GND.
8. Apply main power to the J-F2.
9. Pulse the ON-OFF signal to place the J-F2 into the normal operating state.

4 Updating Patch Code: EEPROM and ROM modules with Host Memory

Modules with EEPROM and ROM-only designs using external Host memory support firmware patching. Firmware patches are accumulated into patch data files, which in turn are made available with descriptions of their contents and applicability. A patch data file is cumulative in that it includes firmware improvements and enhancements made available in previous patches. It may also include configuration settings that differ from the ROM defaults, as in the default UART baud rate, for example. The desired patch data file must be distributed to the end-user device where it may be accessed by the Host processor.

The Host processor in the end-user device is required to run software that sends patch data from the patch file to the module using OSP Patch Protocol messages over the host serial port. Example source code to assist in the implementation of a patch downloader on the Host processor is available. Note that the module must be operating in full power mode during the patching process. The patch contents are loaded into patch RAM on the module, where they remain as long as main power is maintained. This avoids the reloading of patches into patch RAM when the system resumes normal operation from a low power state such as hibernate. At the end of the patching process the module performs an internal reset and restart.

Firmware patch for the EEPROM module is stored inside the I2C serial EEPROM. At power up, patches are retrieved from EEPROM and loaded into patch RAM. If main power is lost on the ROM-only module, the Host processor must re-send the patch data over the host serial port after the module is powered up. The Host processor can determine whether patch data must be sent to the module by polling the software version, which reflects the currently applied patch file version.

5 Main Serial Interface

The J-F2 has the capability to operate in serial UART mode, SPI mode or I2C mode depending upon how the J-F2 GPIO6 and GPIO7 pins are strapped at power up. Either leave the pin floating, apply a 10K resistor to +1.8V (PU) or apply a 10K resistor to GND (PD).

Mode	GPIO6 (internal pull-down)	GPIO7 (internal pull-up)
UART	PU	Leave floating or PU
I2C	Leave floating or PD	PD
SPI	Leave floating	Leave floating

Table 2 – Interface Operating Modes

5.1 UART Mode

The GPIO6 pin should be pulled high through a 10K resistor to the 1.8 volt supply. The GPIO7 pin can be left open or pulled high. Upon power up, the J-F2 will communicate using a standard asynchronous 8 bit protocol with messages appearing on the TX line, and commands and data being entered on the RX line. Note the GPIO6 and GPIO7 lines are read at power up or reset only and are not used afterwards. In particular, no flow control operations are performed.

5.2 I2C Mode

The GPIO7 pin should be pulled low through a 10K resistor to GND. The GPIO6 pin can be left open or pulled low. Upon power, the J-F2 acts as a master transmitter and a slave receiver. Pull-ups to a 1.8V to 3.6V power supply in the range of 1K to 2.2K are required on the RXA and TXA lines when used in I2C mode. In this mode, the pins are defined below:

Signal Name	I2C Function
RXA	I2C Data (DIO)
TXA	I2C Clock (CLK)

Table 3 – I2C Pin Assignments

Bit rates to 400K are achievable. Note the GPIO6 and GPIO7 lines are read at power up or reset only and are not used afterwards.

The operation of the I2C with a master transmit and slave receive mimics a UART operation, where both J-F2 and host can independently freely transmit. It is possible to enable the master transmit and slave receive at the same time, as the I2C bus allows for contention resolution between J-F2 and a host vying for the bus.

Note: This I2C port should not be confused with the secondary I2C port on the J-F2 which is reserved for external serial EEPROM and MEMS sensors.

5.3 SPI Mode

If both the GPIO6 and GPIO7 pins are left floating, the J-F2 will power up in slave SPI mode, supporting both SPI and Microwire formats. In this mode, the four pins are defined below:

Signal Name	SPI Function
GPIO7	SPI Chip Select (CS#)
GPIO6	SPI Clock (CLK)
RXA	SPI Data In (MOSI)
TXA	SPI Data Out (MISO)

Table 4 – SPI Mode Pin Assignments

Note: Data rates of 6.8 MHz are achievable.

6 MEMS Sensor/EEPROM Interface

The DR I2C port is used for connecting to MEMS sensors, such as accelerometer or magnetometer. Pullup resistors of approximately 2.2Kohm to 1.8 volts are required on the DR I2C CLK and DR I2C IO lines for proper operation.

Only an approved accelerometer (KIONIX part number KXTF9-4100, 3 x 3mm LGA 1.8V 3 axis accelerometer) can be used. The interrupt output of the accelerometer must be connected to GPIO4 of the J-F2.

Data for the approved magnetic sensor (Aichi Steel part number AIM304, 3.5 x 4.0mm 3V 3 axis magnetometer) is output in OSP message 72.

7 RF Front End Design

The J-F2 contains an integrated LNA and pre-select SAW filter. This allows the J-F2 to work well with a passive GPS antenna. If the antenna can not be located near the J-F2, then an active antenna (that is, an antenna with a low noise amplifier built in) can be used. The following items will be discussed in turn to assist in designing the "front end".

1. RF signal requirements
2. GPS antenna polarization
3. GPS antenna gain
4. System noise floor
5. Active versus passive antenna
6. RF trace losses
7. Implications of the pre-select SAW filter
8. External LNA gain
9. Powering the external LNA (active antenna)
10. RF interference
11. Shielding

7.1 Signal Requirements

The J-F2 can achieve Cold Start acquisition with a signal level of -147 dBm at its input. This means the J-F2 can find the necessary satellites, download the necessary ephemeris data and compute the location within a 5 minute period. In the GPS signal acquisition process, downloading and decoding the data is the most difficult task, which is why Cold Start acquisition requires a higher signal level than navigation or tracking signal levels. For the purposes of this discussion, autonomous operation is assumed, which makes the Cold Start acquisition level the important design constraint. If assistance data in the form of time or ephemeris aiding is available, then even lower signal levels can be used to compute a navigation solution.

The GPS signal is defined by IS-GPS-200E. This document states that the signal level received by a linearly polarized antenna having 3 dBi gain will be a minimum of -130 dBm when the antenna is in the worst orientation and the satellite is 5 degrees or more above the horizon.

In actual practice, the GPS satellites are outputting slightly more power than specified by IS-GPS-200E, and the signal level typically goes higher as the satellites have higher elevation angles.

The J-F2 will display a reported C/No of 40 dB-Hz for a signal level of -130 dBm into the RF input.

Each GPS satellite presents its own signal to the J-F2, and best performance is obtained when the signal levels are between -125 dBm and -117 dBm. These received signal levels are determined by

- GPS satellite transmit power
- GPS satellite elevation and azimuth
- Free space path loss
- Extraneous path loss such as rain.
- Partial or total path blockage such as foliage or building.
- Multipath caused by signal reflection
- GPS antenna
- Signal path after the GPS antenna.

The first three items in the list above are specified in IS-GPS-200E, readily available multiple sources online. IS-GPS-200E specifies a signal level minimum of -130 dBm will be presented to the receiver when using a linearly polarized antenna with 3 dBi gain.

The GPS signal is relatively immune to rainfall attenuation and does not really need to be considered.

However, the GPS signal is heavily influence by attenuation due to foliage, such as tree canopies, etc. as well as outright blockage caused by building, terrain or other items in the line of sight to the specific GPS satellite. This variable attenuation is highly dependent upon GPS satellite location. If enough satellites are blocked, say at a lower elevation, or all in a general direction, the geometry of the remaining satellites will result is a lower accuracy of position. The J-F2 reports this geometry in the form of PDOP, HDOP and VDOP.

For example, in a vehicular application, the GPS antenna may be placed embedded into the dashboard or rear package tray of an automobile. The metal roof of the vehicle will cause significant blockage, plus any thermal coating applied to the vehicle glass can attenuate the GPS signal by as much as 15 dB. Again, both of these factors will affect the performance of the receiver.

Multipath is a phenomena where the signal from a particular satellite is reflected and is received by the GPS antenna in addition to or in place of the original line of sight signal. The multipath signal has a path length that is longer than the original line of sight path and can either attenuate the original signal, or if received in place of the original signal add additional error is determining a solution because the distance to the particular GPS satellite is actually longer than expected. It is this phenomena that makes GPS navigation in urban canyons (narrow roads surround by high rise buildings) so challenging. In general, the reflecting of the GPS signal causes the polarization to reverse. The implications of this are covered in the next section.

7.2 GPS Antenna Polarization

The GPS signal as broadcast is a right hand circularly polarized signal. The best antenna to receive the GPS signal is a right hand circularly (RHCP) polarized antenna. Remember that IS-GPS-200E specifies the receive power level with a linearly polarized antenna. A linearly polarized antenna will have 3 dB loss as compared to an RHCP antenna assuming the same antenna gain (specified in dBi and dBic respectively).

An RHCP antenna is better at rejecting multipath than a linearly polarized antenna. This is because the reflected signal changes polarization to LHCP, which would be rejected by the RHCP antenna by typically 20 dB or so. If the multipath signal is attenuating the line of sight signal, then the RHCP antenna would show a higher signal level than a linearly polarized antenna because the interfering signal is rejected.

However, in the case where the multipath signal is replacing the line of sight signal, such as in an urban canyon environment, then the number of satellites in view could drop below that needed to determine a 3D solution. This is a case where a bad signal may be better than no signal. The system designer needs to make tradeoffs in their application to determine what is the better choice.

7.3 GPS Antenna Gain

Antenna gain is defined as the extra signal power from the antenna as compared to a theoretical isotropic antenna (equally sensitive in all directions).

For example, a 25mm by 25m square patch antenna on a reference ground plane (usually 70mm by 70mm) will give an antenna gain at zenith of 5 dBic. A smaller 18mm by 18mm square patch on a reference ground plane (usually 50mm by 50mm) will give an antenna gain at zenith of 2 dBic.

While an antenna vendor will specify a nominal antenna gain (usually at zenith, or directly overhead) they should supply antenna pattern curves specifying gain as a function of elevation, and gain at a fixed elevation as a function of azimuth. Pay careful attention to the requirement to meet these specifications, such as ground plane required and any external matching components. Failure to follow these requirements could result in very poor antenna performance.

It is important to note that GPS antenna gain is not the same thing as external LNA gain. Most antenna vendors will specify these numbers separately, but some combine them into a single number. It is important to know both numbers when designing and evaluating the front end of a GPS receiver.

For example, antenna X has an antenna gain of 5 dBiC at azimuth and an LNA gain of 20 dB for a combined total of 25 dB. Antenna Y has an antenna gain of -5 dBiC at azimuth and an LNA gain of 30 dB for a combined total of 25 dB. However, in the system, antenna X will outperform antenna Y by about 10 dB (refer to Section 7.4 for more details on system noise floor).

An antenna with higher gain will generally outperform an antenna with lower gain. Once the signals are above about -130 dBm for a particular satellite, no improvement in performance would be gained. However, for those satellite that are below about -125 dBm, a higher gain antenna would improve the gain and improve the performance of the GPS receiver. In the case of really weak signals, a good antenna could mean the difference between being able to use a particular satellite signal or not.

7.4 System Noise Floor

As mentioned earlier, the J-F2 will display a reported C/No of 40 dB-Hz for an input signal level of -130 dBm. The C/No number means the carrier (or signal) is 40 dB greater than the noise floor measured in a one Hz bandwidth. This is a standard method of measuring GPS receiver performance.

Thermal noise is -174 dBm/Hz at around room temperature. From this we can compute a system noise figure of 4 dB for the J-F2. This noise figure consists of the loss of the pre-select SAW filter, the noise figure of the LNA as well as implementation losses within the digital signal processing unit.

If a good quality external LNA is used with the J-F2, then the noise figure of that LNA (typically better than 1dB) could reduce the overall system noise figure of the J-F2 from 4 dB to around 2 dB. Some of the factors in the system noise figure are implementation losses due to quantization and other factors and don't scale with improved front end noise figure.

7.5 Active versus Passive Antenna

If the GPS antenna is placed near the J-F2 and the RF traces losses are not excessive (nominally 1 dB), then a passive antenna can be used. This would normally be the lowest cost option and most of the time the simplest to use. However, if the antenna needs to be located away from the J-F2 then an active antenna may be required to obtain the best system performance. The active antenna has its own built in low noise amplifier to overcome RF trace or cable losses after the active antenna.

However, an active antenna has a low noise amplifier (LNA) with associated gain and noise figure. In addition, many active antenna have either a pre-select filter, a post-select filter or both.

7.6 RF Trace Losses

RF Trace losses are difficult to estimate on a PCB without having the appropriate tables or RF simulation software to estimate what the losses would be. A good rule of thumb would be to keep the RF traces as short as possible, make sure they are 50 ohms impedance and don't contain any sharp bends.

7.7 Implications of the Pre-select SAW Filter

The J-F2 module contains a SAW filter used in a pre-select configuration with the built in LNA, that is the RF input of the J-F2 ties directly into the SAW filter. Any circuit connected to the input of the J-F2 would see a complex impedance presented by the SAW filter, particularly out of band, rather than the relatively broad and flat return loss presented by the LNA. Filter devices pass the desired in band signal to the output, resulting in low reflected energy (good return loss), and reject the out of band signal by reflecting it back to the input, resulting in high reflected energy (bad return loss).

If an external amplifier is to be used with the J-F2, the overall design should be checked for RF stability to prevent the external amplifier from oscillating. Amplifiers that are unconditionally stable at the output will be fine to use with the J-F2.

If an external filter is to be connected directly to the J-F2, care needs to be used in making sure neither the external filter or the internal SAW filter performance is compromised. These components are typically specified to operate into 50 ohms impedance, which is generally true in band, but would not be true out of band. If there is extra gain associated with the external filter, then a 6 dB Pi or T resistive attenuator is suggested to improve the impedance match between the two components.

7.8 External LNA Gain and Noise Figure

The J-F2 can be used with an external LNA such as what might be found in an active antenna. Because of the internal LNA, the overall gain (including signal losses past the external LNA) should not exceed 14 dB. Levels higher than that can affect the jamming detection capability of the J-F2. If a higher gain LNA is used, either a resistive Pi or T attenuator can be inserted after the LNA to bring the gain down to 14 dB or the J-F2 can be switched into a low gain mode by issuing an OSP command to do so.

The external LNA should have a noise figure better than 1 dB. This will give an overall system noise figure of around 2 dB assuming the LNA gain is 14 dB, or if higher the low gain mode is selected within the J-F2.

The external LNA, if having no pre-select filter, needs to be able to handle other signals other than the GPS signal. These signals are typically at much higher levels. The amplifier needs to stay in the linear region when presented with these other signals. Again, the system designer needs to determine all of the unintended signals and their possible levels that can be presented and make sure the external LNA will not be driven into compression. If this were to happen, the GPS signal itself would start to be attenuated and the GPS performance would suffer.

7.9 Powering the External LNA (active antenna)

The external LNA needs a source of power. Many of the active antennas accept a 3 volt or 5 volt DC voltage that is impressed upon the RF signal line. This voltage is not supplied by the J-F2, but can be easily supplied by the host design.

Two approaches can be used. The first is to use an inductor to tie directly to the RF trace. This inductor should be at self resonance at L1 (1.57542 GHz) and should have good Q for low loss. The higher the Q, the lower the loss. The side of the inductor connecting to the antenna supply voltage should be bypassed to ground with a good quality RF capacitor, again operating at self resonance at the L1 frequency.

The second approach is to use a quarter wave stub in place of the inductor. The length of the stub is designed to be exactly a quarter wavelength, which has the effect of making an RF short at L1 at one end of the stub to appear as an RF open. The RF short is created by the good quality RF capacitor operating at self resonance.

The choice between the two would be determined by:

- RF path loss introduced by either the inductor or quarter wave stub.
- Cost of the inductor.
- Space availability for the quarter wave stub.

Simulations done by Navman Wireless show the following:

- Murata LQG15HS27NJ02 Inductor on FR4 — 0.65 dB of additional signal loss
- Quarter wave stub on FR4 — 0.59 dB of additional signal loss
- Coilcraft B09TJLC air coil inductor — 0.37 dB of additional signal loss

This additional loss occurs after the LNA so it is generally not significant unless the circuit is being designed to work with either an active or a passive antenna.

7.10 RF Interference

RF Interference into the GPS receiver tends to be the biggest problem when determining why the system performance is not meeting expectations. As mentioned earlier, the GPS signals are at -130 dBm and lower. If signal higher than this are presented to the receiver it can be overwhelmed. The J-F2 can reject up to 8 CW in-band jamming signals, but would still be affected by non-CW signals.

The most common source of interference is digital noise. This is created by the fast rise and fall times and high clock speeds of modern digital circuitry. For example, a popular netbook computer uses an Atom processor clocked at 1.6 GHz. This is only 25 MHz away from the GPS signal, and depending upon temperature of the SAW filter, can be within the passband of the GPS receiver. Because of the nature of the address and data lines, this would be broadband digital noise at a relatively high level.

Such devices are required to adhere to a regulatory standard for emissions such as FCC Part 15 Subpart J Class B or CISPR 22. However, these regulatory emission levels are far higher than the GPS signal.

Shielding the RF circuitry generally is ineffective because the interference is getting into the GPS antenna itself, the most sensitive portion of the RF path. The antenna cannot be shielded because then it can't receive the GPS signals.

There are two solutions, one is to move the antenna away from the source of interference or the second is to shield the digital interference to prevent it from getting to the antenna.

8 Reference Design

The J-F2 Reference Design is presented in the figure below.

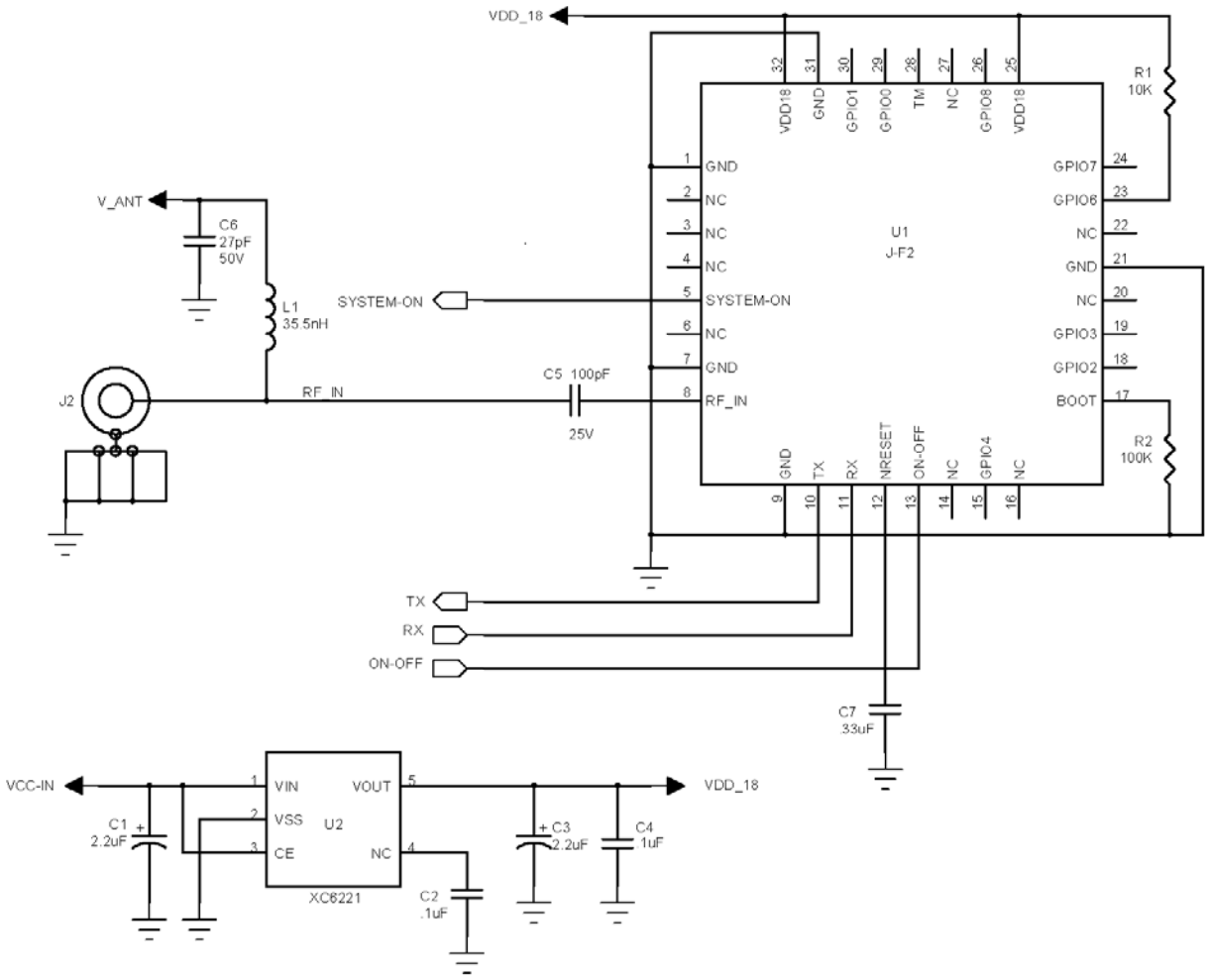

Figure 2 – J-F2 Reference Design

Along with power and ground, the minimum number of signals required to operate the J-F2 properly are four digital signals and one RF signal.

The RF input can be connected directly to a GPS antenna. The reference design shows a DC power feed for an active antenna. C5 is used to block the DC voltage from entering the J-F2. The inductor L1 is chosen to be self resonant at the GPS frequency, 1.57542 GHz, to minimize loading on the RF trace. Capacitor C6 is chosen to be self resonant at the GPS frequency such that is looks pretty close to an RF short at that frequency. V_ANT is the supply voltage for the external active antenna.

TX is the normal digital output and as configured in the reference design, is a serial UART with a default bit rate of 4800 bps, 1 stop bit and 8 data bits. This is a 1.8 volt logic level signal. As is the case with all serial data, the idle state is logic one.

RX is the normal digital input and as configured in the reference design, is a serial UART with a default bit rate of 4800 bps, 1 stop bit and 8 data bits. This is a 1.8 volt logic level signal, but is tolerant to 3.6 volts. As is the case with all serial data, the idle state is logic one.

SYSTEM-ON is an output indicating the power state of the J-F2. If the module is in Hibernate mode the logic level will be zero, and if powered up and running, the logic level will be one. This is a 1.8 volt logic level.

ON-OFF is an input to control the power state of the J-F2. Upon first applying power, the J-F2 enters the hibernate state with SYSTEM-ON low. Wait until the SYSTEM-ON pulse goes high then low to indicate the J-F2 is ready to accept an ON-OFF pulse. Then ON-OFF can be pulsed high for minimum of 100 microseconds to change the power state. SYSTEM-ON will then go to a logic one.

If the user wishes the J-F2 to power up into the ON state and is willing to live with reduced power management options, then ON-OFF can be tied directly to SYSTEM-ON. In this case, GPIO8 should be pulled high with a pullup resistor to VDD_18. This pullup changes the operation of the ON-OFF input to that of just ON.

If the user plans on controlling ON-OFF from an external source, then GPIO8 should be tied low with a 100Kohm resistor to help minimize leakage current.

Resistor R1 as shown pulls GPIO6 high, which determines the input/output configuration of the J-F2 to be serial I/O.

The power supply shown is a minimal design for the J-F2 power requirements. The power supply must have tight voltage regulation under varying line and load conditions to prevent falsely tripping the internal voltage supervisor within the J-F2.

The NRESET input is tied to a 0.33uF capacitor to reduce susceptibility to noise on the power supply. It is not necessary to supply an external signal to this pin.

Note: Connection to Boot signal is not required for EEPROM and ROM-only modules.

9 Software Configuration

The J-F2 can be configured by means of software in order to fit better into the overall system. This section describes certain aspects of the receiver that can be configured.

9.1 Internal LNA

The J-F2 offers two modes of operation, high gain mode and low gain mode, for the internal LNA. The high gain mode is the default mode and provides 16 to 20dB of gain. This is the default gain mode. The low gain mode provides 6 to 10dB of gain.

In general, the high gain mode is intended for use with passive antennas, while the low gain mode is used when there is an external LNA as part of the RF front end (e.g. active antenna). The recommended external LNA gain is 20dB.

High gain mode is selected by software when the receiver starts up. A version of J-F2 software is offered for system designs that require the low gain mode. The Tracker Config message (OSP MID178, SID2) can be used to change the LNA mode. Note that the use of the Tracker Config message is not recommended. Contact Navman Wireless technical support if this approach is required in your system.

9.2 Low Power Modes

The J-F2 module can be operated in one of four power management modes; Full Power, TricklePower™, Push-To-Fix™, and Micro Power. The latter three of these modes offer progressively lower power consumption profiles. Depending upon the requirements of the system design regarding frequency of position updates and availability of GPS signals in the operational environment, the designer can choose a mode that provides the best trade-off of performance versus power consumption.

Each of the power management modes can be commanded using the Power Mode Request Message (MID218), which is available as part of the OSP message set. More details regarding low power operation can be found in the Low Power Operating Modes Application Note.

9.2.1 Full Power

This mode consumes the most average power, but it is the most accurate navigation mode and supports the most dynamic motion scenarios.

9.2.2 TricklePower™

This mode is a duty-cycling mode. It provides navigation updates at a fixed rate and retains a high quality of GPS accuracy and dynamic motion response, but at a lower average power cost as compared to Full Power operation. TricklePower mode produces significant power savings in strong signal conditions.

9.2.3 Push-To-Fix

This mode provides for even lower power consumption than TricklePower. It is intended for applications that require infrequent position reports. The position is reported periodically by the receiver (once every 30 minutes by default) and also when requested. To request a position update, a pulse is asserted on the ON-OFF pin.

9.2.4 Micro Power Mode (MPM)

Micro Power mode is the lowest power operating mode. Rather than providing position updates at a reduced rate, it is predicated on maintaining the availability of a navigation solution by maintaining hot start conditions in the receiver at all times. The receiver is put into Full Power by pulsing the ON-OFF pin. It is put back into Micro Power mode by sending a Power Mode Request command to the receiver.

9.3 Host Serial Interface

As mentioned above in Section 5, the host serial interface can be configured as a UART, I2C or SPI port by strapping one or both pins GPIO 6 and GPIO 7 to certain levels at power up. The data rate for I2C is fixed at 400 kbps. The slave SPI supports a maximum clock input rate of 6.8 MHz. The UART can operate at baud rates of 4800, 9600, 19200, 38400, 57600, 115200, 230400 and 460800 bps.

9.3.1 NMEA Protocol Considerations

The lower UART baud rates are typically used for NMEA protocol. Note should be taken however of the bandwidth limitation at 4800 baud. By default, the J-F2 module communicates using NMEA at 4800 baud, with the periodic output messages limited to the GGA, GSA and RMC messages at once per second and the GSV message once every five seconds. At 9600 baud or higher, additional output messages may be enabled.

If the J-F2 is operated in TricklePower mode, a baud rate of at least 38400 is recommended. This reduces the time required for data output and allows the receiver to drop into the lowest power state for a longer average time.

Use the Set Serial Port (PSRF100) NMEA command to change the baud rate. This command can also be used to switch the protocol to OSP as described in the next section. Use the Query/Rate Control (PSRF103) to enable and disable output messages and set their output rates.

9.3.2 OSP Considerations

The higher baud rates are used for OSP. OSP offers a richer set of commands and more types of data output than does NMEA. Use the Set Serial Port (PSRF100) NMEA command to switch the protocol from NMEA to OSP. The minimum recommended baud rate for OSP is 38400, provided that debug data messages are not enabled. If data debug messages are enabled, the minimum baud rate is 115200 in order to prevent data from being dropped. The protocol can be switched back to NMEA using the Switch to NMEA Protocol command (Message ID 129).

9.4 MEMS Configuration

The J-F2 module interfaces to MEMS sensors using the dead reckoning (DR) I2C bus as mentioned in Section 5. The sensors that may be connected are an accelerometer and a magnetometer, also called a digital compass.

A Sensor Configuration OSP message (Message ID 234, Sub ID 1) must be sent to the J-F2 in order to configure it to interface with the connected sensor or sensors. The configuration data in this message is extensive and is described in detail in the OSP Manual. After the sensor interface has been configured, the sensors must be enabled using the Sensor Switch message (Message ID 234, Sub ID 2).

Once the sensor interface has been configured and the sensors enabled, the sensor data will be output by the J-F2 in OSP Message 72, Sub ID 1. Note that a data message is output for each sensor and can contain several sets of data from the given sensor.

9.5 Advanced Features

9.5.1 CW Jamming Detection

The J-F2 module detects, tracks and removes narrow-band interfering signals (jammers) without the need for external components or tuning. It monitors a frequency band that is +/- 4MHz from the L1 frequency for jammers. Any number of jammers that occur outside of a +/-1MHz center band are removed by the J-F2 with a 2MHz band pass filter. Up to eight jammers inside this center band are removed using a notch filter.

Data regarding detected jammers is output using OSP messages. Message ID 92, Sub ID 1, reports up to eight of the most recently detected interferers. This feature is useful both in the design stage and during the production stage for uncovering issues related to unexpected jamming.

9.5.2 SBAS

The J-F2 receiver is capable of using Satellite-Based Augmentation System (SBAS) satellites as a source of both differential corrections and satellite range measurements. These systems (WAAS, EGNOS, MSAS) use geostationary satellites to transmit regional differential corrections via a GPS-compatible signal. The use of SBAS corrections can improve typical position accuracy to 3m or less in open-sky applications.

Note that only an SBAS can be used as source of differential corrections. Other sources such as data from RTCM beacons are not supported.

By default the J-F2 does not attempt to acquire SBAS satellites. This can be changed by sending in a DGPS Source command (MID 133) and specifying the source of DGPS corrections as SBAS. When the receiver acquires SBAS satellites, it will demodulate and use corrections data from the satellite signal.

The receiver can be configured to compute SBAS satellite range measurements and use them in the navigation solution. This can be enabled through a control bit in the OSP Mode Control command (MID 136). See the OSP Manual for details.

9.5.3 2-D Acquisition

By default, the J-F2 will compute a 2-D solution when possible when performing initial acquisition. In a 2-D solution, the receiver assumes a value for altitude and uses it to estimate the horizontal position. Under warm and hot start conditions, the receiver uses the last known value of altitude, which is a good assumption in most situations.

However under cold start conditions, the last position is unknown, and the receiver assumes a value of 0. In situations where the true altitude is significantly higher than that, the horizontal position estimate will be noticeably impacted.

The use of 2-D acquisition is established by software when the receiver starts up. A version of J-F2 software is offered for applications that require a calculated altitude (3-D solution) when the receiver first enters navigation.

10 Handling and soldering

10.1 Moisture Sensitivity

The J-F2 module has a moisture sensitivity level rating of 3 as defined by IPC/JEDEC J-STD-020. This rating is assigned due to some of the components used within the J-F2.

The J-F2 is supplied in trays or tape and reel and is hermetically sealed with desiccant and humidity indicator card. The J-F2 parts must be placed and reflowed within 48 hours of first opening the hermetic seal provided the factory conditions are less than 30°C and less than 60% and the humidity indicator card indicates less than 10% relative humidity.

If the package has been opened or the humidity indicator card indicates above 10%, then the parts will need to be baked prior to reflow. The parts may be baked at +125°C ± 5°C for 48 hours. However, the trays, nor the tape and reel can withstand that temperature. Lower temperature baking is feasible if the humidity level is low and time is available. Please see IPC/JEDEC J-STD-033 for additional information.

Additional information can be found on the MSL tag affixed to the outside of the hermetical seal bag.

Note: JEDEC standards are available for free from the JEDEC website http://www.jedec.org.

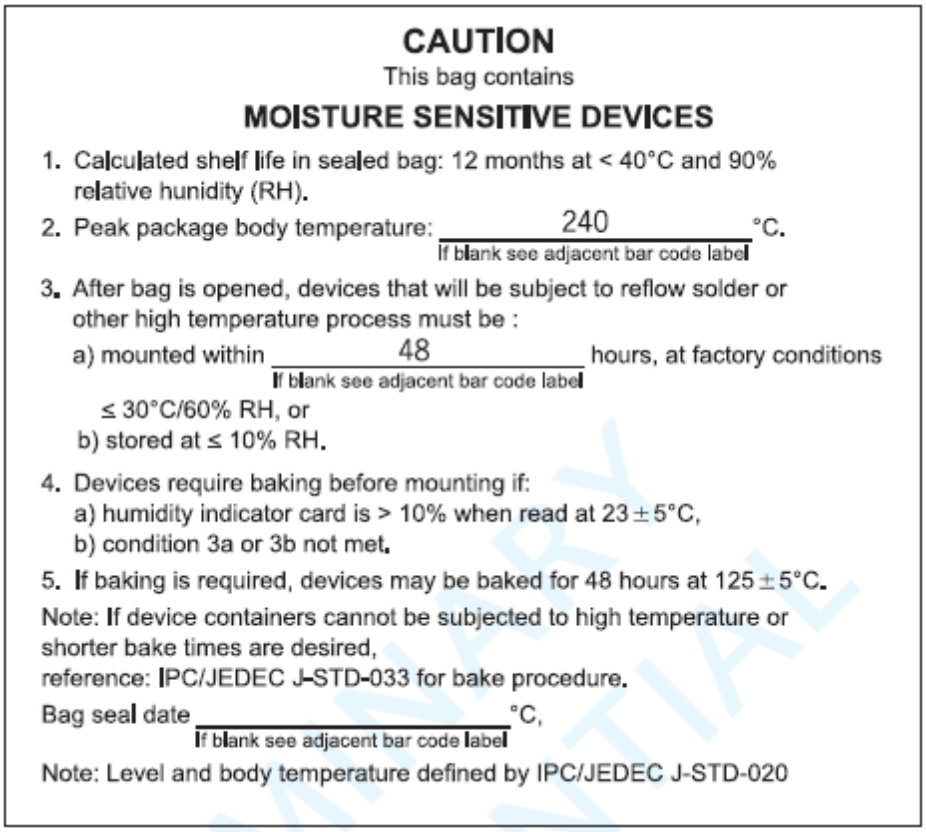

Figure 3 – Label for Moisture Sensitive Devices

10.2 ESD

The J-F2 is an electrostatic discharge sensitive device and should be handled in accordance with JESD625-A requirements for Handling Electrostatic Discharge Sensitive (ESDS) Devices. Although the J-F2 is a module, the expecting handling of the J-F2 during assembly and test is identical to that of a semiconductor device.

Note: JEDEC standards are available for free from the JEDEC website http://www.jedec.org.

10.3 Reflow

The J-F2 is compatible with lead free soldering processes as defined in IPC/JEDEC J-STD-020. The reflow profile must not exceed the profile given IPC/JEDEC J-STD-020 Table 5-2, “Classification Reflow Profiles”. Although IPC/JEDEC J-STD-020 allows for three reflows, the assembly process for the J-F2 uses one of those profiles. Thus the J-F2 is limited to two reflows.

Note: JEDEC standards are available for free from the JEDEC website http://www.jedec.org.

When reflowing a dual-sided SMT board, it is important to reflow the side containing the J-F2 module last. This prevents heavier components within the J-F2 becoming dislodged if the solder reaches liquidus temperature while the module is inverted.

10.4 Assembly Issues

Due to the piezo-electric components within the J-F2, the component should be placed close to the end of the assembly process to minimize shock to the module. During board singulation, pay careful attention to unwanted vibrations and resonances introduced into the board assembly by the board router.

11 PCB Layout Details

The PCB footprint on the receiving board should match the J-F2 pad design shown below. The solder mask opening is generally determined by the component geometry of other parts on the board and can be followed here.

Standard industry practice is to use a paste mask stencil opening the same dimensions as the pad design.

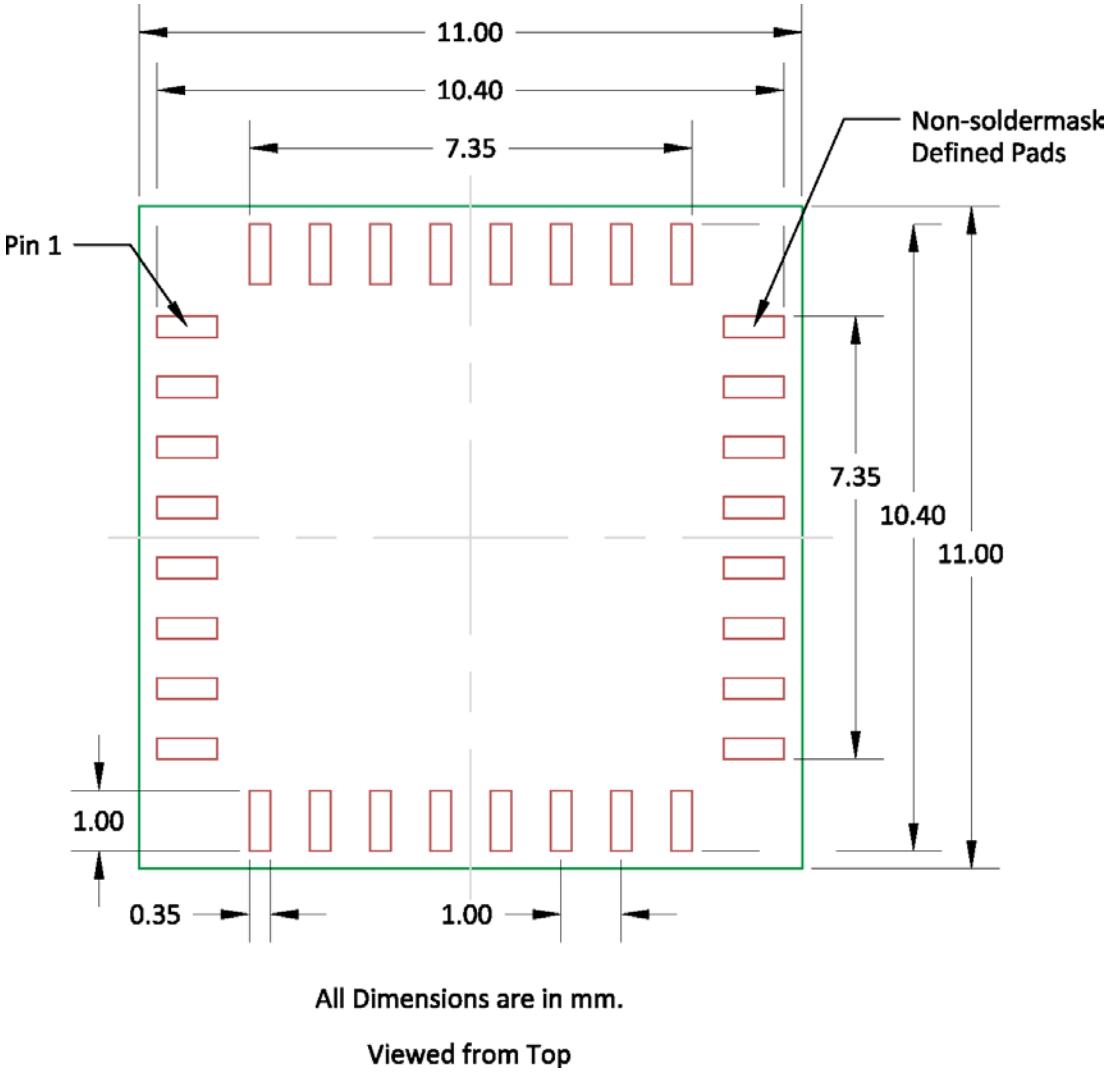

Figure 4 – J-F2 Pad Design

12 Revision History

Date	Revision	Changes
6/3/11	-	Initial Release
6/6/11	A	Update reference design, Figure 2.
6/28/11	B	Update product naming. Remove reference to J-R2 and J-H2.