GE863-GPS & GE863-GPS V2 HW differences Application Note

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APPLICABLE PRODUCTS

PRODUCT
GE863-GPS

Contents

1.   Introduction

1.1.   Scope

This application note is intended to highlight the differences from the hardware point of view, between the GE863-GPS and the GE863-GPS V2, with the aim to help the system integrator in the design a host application and therefore a PCB, which might host all the GE863-GPS. However, this option might require a minimum part list change of the host PCB.

Moreover, this document might help also the system integrator to migrate its application from the use of one version of the GE863-GPS to the GE863-GPS V2.

1.2.   Contact Information, Support

For general contact, technical support, to report documentation errors and to order manuals, contact Telit's Technical Support Center (TTSC) at:

> TS-EMEA@telit.com
> TS-NORTHAMERICA@telit.com
> TS-LATINAMERICA@telit.com
> TS-APAC@telit.com

Alternatively, use:
http://www.telit.com/en/products/technical-support-center/contact.php
For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:
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To register for product news and announcements or for product questions contact Telit's
Technical Support Center (TTSC).
Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.
Telit appreciates feedback from the users of our information.

1.3.   Document Organization

This document contains the following chapters:
Chapter 1: "Overview" provides a scope for this document, target audience, contact and support information, and text conventions.
Chapter 2: "General considerations" is about what customer has to know before design activity.
Chapter 3: "Comparison Table" describes the differences between the modules.
Chapter 4: "Mechanical Dimension" : highlight the differences between the module's packaging.

: contains the revision history of the present document.

1.4. Text Conventions

Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

Tip or Information – Provides advice and suggestion that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

1.5. Related Documents

- GE863-GPS documentation

2.   General considerations

Before start with a design of an application that makes use of the GE863-GPS, all the contents of the HW User Guides of the product must be known. This application note is intended to highlight only the differences between those products, and help on some project aspects.

3. Comparison table

The following table highlights <u>ONLY the differences</u> in the pin-out functions between the GE863-GPS and the GE863-GPS V2.

- The yellow color highlights pins that have common features, but that have small difference.

- The blue color highlights the pin on GE863-GPS V2 not implemented all or part of the function.

	GE863-GPS				GE863-GPS V2			
Ball	Signal	I/O	Description	Type	Signal	I/O	Description	Type
1	GPIO13	I/O	GPIO13	CMOS 2.8V MAX 3.3V	RESERVED	-	NOT implemented	-
2	GPIO12	I/O	GPIO12 pull-up 47KΩ	CMOS 2.8V MAX 3.3V	RESERVED	-	NOT implemented	-
3	GPIO11	I/O	GPIO11 pull-up 4.7KΩ	CMOS 2.8V MAX 3.3V	RESERVED	-	NOT implemented	-
4	GPIO10/ DVI2_TX	I/O	GPIO10 DVI2_TX (Digital Voice Interface)	CMOS 2.8V MAX 3.3V	GPIO10/ DVI2_TX	I/O	GPIO10 DVI2_TX (Digital Voice Interface)	CMOS 2.8V MAX 3.1V
5	GPIO9	I/O	GPIO9	CMOS 2.8V MAX 3.3V	GPIO9	I/O	GPIO9	CMOS 2.8V MAX 3.1V
6	GPIO8	I/O	GPIO8	CMOS 2.8V MAX 3.3V	GPIO8	I/O	GPIO8	CMOS 2.8V MAX 3.1V
7	RESERVED	-	RESERVED	-	RESERVED	-	RESERVED	-
8	GND	-	Ground	Power	GND	-	Ground	Power
9	EAR_MT-	AO	Handset earphone signal output, phase -	Audio	EAR_MT-	AO	Handset earphone signal output, phase -	Audio
10	EAR_MT+	AO	Handset earphone signal output, phase +	Audio	EAR_MT+	AO	Handset earphone signal output, phase +	Audio
11	EAR_HF+	AO	Handsfree ear output, phase +	Audio	EAR_HF+	AO	Handsfree ear output, phase +	Audio
12	EAR_HF-	AO	Handsfree ear output, phase -	Audio	EAR_HF-	AO	Handsfree ear output, phase -	Audio
13	MIC_MT+	AI	Handset microphone signal input; phase+	Audio	MIC_MT+	AI	Handset microphone signal input; phase+	Audio
14	MIC_MT-	AI	Handset microphone signal input; phase-	Audio	MIC_MT-	AI	Handset microphone signal input; phase-	Audio
15	MIC_HF+	AI	Handsfree microphone input; phase +	Audio	MIC_HF+	AI	Handsfree microphone input; phase +	Audio
16	MIC_HF-	AI	Handsfree microphone input; phase -	Audio	MIC_HF-	AI	Handsfree microphone input; phase -	Audio
17	GND	-	Ground	Power	GND	-	Ground	Power
18	SIMCLK	O	External SIM signal - Clock	1.8/3V ONLY	SIMCLK	O	External SIM signal - Clock	1.8/3V ONLY
19	SIMRST	O	External SIM signal - Reset	1.8/3V ONLY	SIMRST	O	External SIM signal - Reset	1.8/3V ONLY
20	SIMIO	I/O	External SIM signal - Data I/O	1.8/3V ONLY	SIMIO	I/O	External SIM signal - Data I/O	1.8/3V ONLY
21	SIMIN	I/O	External SIM signal - Presence (active low) Pull-up 47KΩ	CMOS 2.8V MAX 3.3V	SIMIN	I/O	External SIM signal - Presence (active low) Internal pull-up	CMOS 2.8V MAX 3.1V
22	SIMVCC	-	External SIM signal - Power	1.8/3V ONLY	SIMVCC	-	External SIM signal - Power	1.8/3V ONLY
23	ADC_IN1	AI	Analog /Digital converter input	A/D	ADC_IN1	AI	Analog /Digital converter input	A/D
24	VRTC	AO	VRTC Backup capacitor	Power	VRTC	AO	VRTC Backup capacitor	Power
25	TX_TRACE		TX data for GPS control (TX data for Debug in case of GE863-GPS/PY/SIM)	CMOS 2.8V MAX 3.3V	TX_TRACE		TX data for GPS control NOT implemented. TX data for Debug in case of GE863-GPS/PY/SIM implemented.	CMOS 2.8V MAX 3.1V
26	RX_TRACE		RX data for GPS control (RX data for Debug in case of GE863-GPS/PY/SIM)	CMOS 2.8V MAX 3.3V	RX_TRACE		RX data for GPS control NOT implemented. RX data for Debug in case of GE863-GPS/PY/SIM implemented.	CMOS 2.8V MAX 3.1V
27	VBATT	-	Main power supply	Power	VBATT	-	Main power supply	Power
28	GND	-	Ground	Power	GND	-	Ground	Power

29	STAT_LED	O	Status indicator led	CMOS 1.8V	STAT_LED	O	Status indicator led	CMOS 1.8V
30	AXE	I	Handsfree switching Pull-up 100KΩ	CMOS 2.8V MAX 3.3V	AXE	I	Handsfree switching Internal pull-up	CMOS 2.8V MAX 3.1V
31	VAUX1	-	Power output for external accessories	-	VAUX1	-	Power output for external accessories. Always ON.	-
32	GPIO4/ DVI2_CLK	I/O	GPIO4 Configurable general purpose I/O pin/ DVI2_CLK (Digital Voice Interface) pull-up 4.7KΩ	CMOS 2.8V MAX 3.3V	GPIO4/DVI2_ CLK	I/O	GPIO4 Configurable general purpose I/O pin/ DVI2_CLK (Digital Voice Interface) NO pull-up WARNING: DVI2_CLK and GPIO4 cannot be used at the same time. GPIO4 must be set as INPUT when DVI is used. DVI must be disabled when GPIO4 is used.	CMOS 2.8V MAX 3.1V
33	GPIO2 / JDR	I/O	GPIO2 Configurable general purpose I/O pin / Jammer Detect Output	CMOS 2.8V MAX 3.3V	GPIO2 / JDR	I/O	GPIO2 Configurable general purpose I/O pin / Jammer Detect Output	CMOS 2.8V MAX 3.1V
34	GPIO1	I/O	GPIO1 Configurable general purpose I/O pin	CMOS 2.8V MAX 3.3V	GPIO1	I/O	GPIO1 Configurable general purpose I/O pin	CMOS 2.8V MAX 3.1V
35	CHARGE	AI	Charger input	Power	RESERVED	-	NOT implemented	-
36	GND	-	Ground	Power	GND	-	Ground	Power
37	C103/TXD	I	Serial data input (TXD) from DTE	CMOS 2.8V MAX 3.3V	C103/TXD	I	Serial data input (TXD) from DTE	CMOS 2.8V MAX 3.1V
38	C104/RXD	O	Serial data output to DTE	CMOS 2.8V MAX 3.3V	C104/RXD	O	Serial data output to DTE	CMOS 2.8V MAX 3.1V
39	C108/DTR	I	Input for Data terminal ready signal (DTR) from DTE	CMOS 2.8V MAX 3.3V	C108/DTR	I	Input for Data terminal ready signal (DTR) from DTE	CMOS 2.8V MAX 3.1V
40	C105/RTS	I	Input for Request to send signal (RTS) from DTE	CMOS 2.8V MAX 3.3V	C105/RTS	I	Input for Request to send signal (RTS) from DTE	CMOS 2.8V MAX 3.1V
41	C106/CTS	O	Output for Clear to send signal (CTS) to DTE	CMOS 2.8V MAX 3.3V	C106/CTS	O	Output for Clear to send signal (CTS) to DTE	CMOS 2.8V MAX 3.1V
42	C109/DCD	O	Output for Data carrier detect signal (DCD) to DTE	CMOS 2.8V MAX 3.3V	C109/DCD	O	Output for Data carrier detect signal (DCD) to DTE	CMOS 2.8V MAX 3.1V
43	C107/DSR	O	Output for Data set ready signal (DSR) to DTE	CMOS 2.8V MAX 3.3V	C107/DSR	O	Output for Data set ready signal (DSR) to DTE	CMOS 2.8V MAX 3.1V
44	C125/RING	O	Output for Ring indicator signal (RI) to DTE	CMOS 2.8V MAX 3.3V	C125/RING	O	Output for Ring indicator signal (RI) to DTE	CMOS 2.8V MAX 3.1V
45	GND	-	Ground	Power	GND	-	Ground	Power
46	ON_OFF*	I	Input command for switching power ON or OFF (toggle command). pull-up 47KΩ	Pull up to VBATT	ON_OFF*	I	Input command for switching power ON or OFF (toggle command). ON_OFF* must be tied low at least 5 seconds.	Pull up to VBATT
47	RESET*	I	Reset input	MAX 2.0V	RESET*	I	Reset input	MAX 1.8V
48	GND	-	Ground	Power	GND	-	Ground	Power
49	ANTENNA	O	GSM Antenna output - 50 Ω	RF	ANTENNA	O	GSM Antenna output - 50 Ω	RF
50	GND	-	Ground	Power	GND	-	Ground	Power
51	GPIO7 / BUZZER	I/O	GPIO7 / BUZZER output	CMOS 2.8V MAX 3.3V	GPIO7 / BUZZER	I/O	GPIO7 / BUZZER output	CMOS 2.8V MAX 3.1V
52	PWRMON	O	Power ON Monitor	CMOS 2.8V MAX 3.3V	PWRMON	O	Power ON Monitor	CMOS 2.8V MAX 3.1V
53	GPIO5/ RFTXMON	I/O	GPIO5 / RF TX_ON signaling output	CMOS 2.8V MAX 3.3V	GPIO5 RFTXMON	I/O	GPIO5 / RF TX_ON signaling output	CMOS 2.8V MAX 3.1V
54	GPIO6 ALARM	I/O	GPIO6 / ALARM output	CMOS 2.8V MAX 3.3V	GPIO6 ALARM	I/O	GPIO6 / ALARM output	CMOS 2.8V MAX 3.1V

55	GPIO3	I/O	GPIO3 pull-up 47KΩ	CMOS 2.8V MAX 3.3V	GPIO3	I/O	GPIO3 NO pull-up	CMOS 2.8V MAX 3.1V
56	GND	-	Ground	Power	GND	-	Ground	Power
57	RESERVED	-	RESERVED	-	RESERVED	-	RESERVED	-
58	CLK SSC	I/O	Python Debug (CLK)	CMOS 2.8V MAX 3.3V	RESERVED	-	NOT implemented	-
59	GPIO17/ DVI2_WAO	I/O	GPIO17 Configurable general purpose I/O pin/ DVI2_WAO (Digital Voice Interface)	CMOS 2.8V MAX 3.3V	DVI2_WAO	-	GPIO17 NOT implemented. DVI2_WAO implemented.	CMOS 2.8V MAX 3.1V
60	GPIO14	I/O	GPIO	CMOS 2.8V MAX 3.3V	RESERVED	-	NOT implemented	-
61	MRST SSC	I/O	Python Debug (MRST)	CMOS 2.8V MAX 3.3V	RESERVED	-	NOT implemented	-
62	RESERVED	-	RESERVED	-	RESERVED	-	RESERVED	-
63	DAC_OUT	O	DAC out		DAC_OUT	O	DAC out	
64	GPIO16	I/O	GPIO	CMOS 2.8V MAX 3.3V	RESERVED	-	NOT implemented	-
65	RESERVED	-	RESERVED	-	RESERVED	-	RESERVED	-
66	MTSR SSC	I/O	Python Debug (MTSR)	CMOS 2.8V MAX 3.3V	RESERVED	-	NOT implemented	-
67	GND	-	Ground	Power	GND	-	Ground	Power
68	TX_GPS	-	GPS serial Port (TX)	-	TX_GPS	-	GPS serial Port (TX)	-
69	GND	-	Ground	Power	GND	-	Ground	Power
70	RESERVED	-	RESERVED	-	RESERVED	-	RESERVED	-
71	GPIO15	I/O	GPIO	-	RESERVED	-	NOT implemented	-
72	GND	-	Ground	Power	GND	-	Ground	Power
73	RX_GPS	-	GPS serial Port (RX)	-	RX_GPS	-	GPS serial Port (RX)	-
74	RESERVED	-	RESERVED	-	RESERVED	-	RESERVED	-
75	PPS	O	1 Pulse per Second signal 100 KΩ pull down	CMOS 2.8V	PPS	O	1 Pulse per Second signal 100 KΩ pull down	CMOS 1.8V
76	GPIO18/ DVI2_RX	I/O	GPIO18 Configurable general purpose I/O pin/ DVI2_RX (Digital Voice Interface)	CMOS 2.8V MAX 3.3V	DVI2_RX	I	GPIO18 NOT implemented. DVI2_RX implemented.	CMOS 2.8V MAX 3.1V
77	GND	-	Ground	Power	GND	-	Ground	Power
78	RX_GPS_BIN	-	GPS serial Port (RX) – SIRF BINARY	CMOS 2.8V	RESERVED	-	NOT implemented	-
79	GND	-	Ground	Power	GND	-	Ground	Power
80	TX_GPS_BIN	-	GPS serial Port (TX) – SIRF BINARY	CMOS 2.8V	RESERVED	-	NOT implemented	-
81	RESERVED	-	RESERVED	-	RESERVED	-	RESERVED	-
82	GND	-	Ground	Power	GND	-	Ground	Power
83	GPS_ANT	-	GPS ANTENNA		GPS_ANT		GPS ANTENNA GPS ANTENNA power supply NOT implemented GPS ANTENNA detection NOT implemented	
84	GND_GPS	-	GPS_ANTENNA GND	Power	GND_GPS	-	GPS_ANTENNA GND	Power

⚠️ **NOTE:**
For a compatible design, all the balls corresponding to "RESERVED" MUST NOT be connected.

3.1. GPIO Logic levels

The GE863-GPS V2 have a lower tolerance against the high level input compared to the GE863-GPS, which are highlighted in red in the following subparagraphs. **The same levels must be applied on the serial port pins also.**

3.1.1. GE863-GPS V2

Where not specifically stated, all the interface circuits work at 2.8V CMOS logic levels.
The following table shows the logic level specifications used in the GE863-GPS V2 interface circuits:

Absolute Maximum Ratings - Not Functional

Parameter	Min	Max
Input level on any digital pin when on	-0.3V	+3.1V
Input voltage on analog pins when on	-0.3V	+3.0 V

Operating Range - Interface levels (2.8V CMOS)

Level	Min	Max
Input high level	2.1V	3.1V
Input low level	0V	0.5V
Output high level	2.2V	3.0V
Output low level	0V	0.35V

Operating Range - Interface levels (1.8V CMOS)

Level	Min	Max
Input high level	1.6V	2.2V
Input low level	0V	0.4V
Output high level	1,65V	2.2V
Output low level	0V	0.35V

3.1.2.   GE863-GPS

Where not specifically stated, all the interface circuits work at 2.8V CMOS logic levels.
The following table shows the logic level specifications used in the GE863-GPS interface circuits:

Absolute Maximum Ratings -Not Functional

Parameter	Min	Max
Input level on any digital pin when on	-0.3V	+3.6V
Input voltage on analog pins when on	-0.3V	+3.0 V

Operating Range - Interface levels (2.8V CMOS)

Level	Min	Max
Input high level	2.1V	3.3V
Input low level	0V	0.5V
Output high level	2.2V	3.0V
Output low level	0V	0.35V

Operating Range - Interface levels (1.8V CMOS)

Level	Min	Max
Input high level	1.6V	2.2V
Input low level	0V	0.4V
Output high level	1,65V	2.2V
Output low level	0V	0.35V

⚠️ NOTE:
For a compatible design, the narrower logic levels of the GE863-GPS V2 be chosen; otherwise there is the risk to damage the unit.
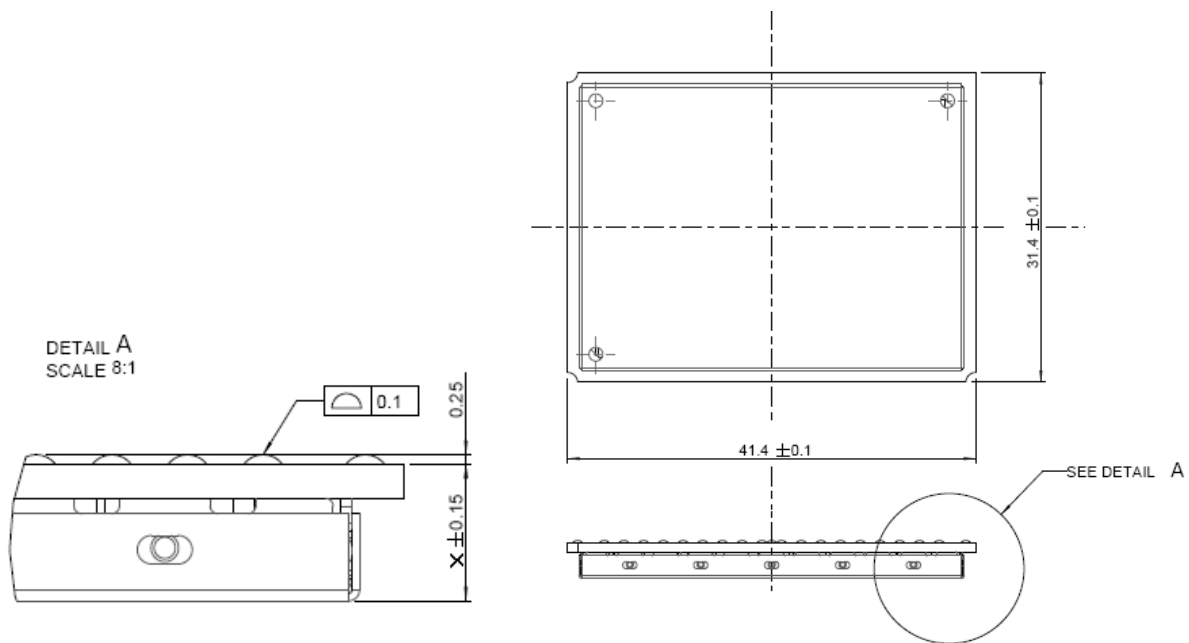
4.   Mechanical Dimensions

The following the differences from mechanical point of view:

The Telit GE863 module's overall dimensions are:

	GE863-GPS	GE863-GPS V2
Length	41.4 mm	41.4 mm
Width	31.4 mm	31.4 mm
Thickness (x)	3.6 mm	4.0 mm

5. Document History

Revision	Date	Changes	Location
0	2012-09-11	First issue	Trieste