GL865-QUAD V4
HW User Guide

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TECHNICAL
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APPLICABILITY TABLE

PRODUCTS

- GL865-QUAD V4

Contents

1. INTRODUCTION

1.1. Scope

This document introduces the GL865-QUAD V4 module and presents possible and recommended hardware solutions for developing a product based on this module. All the features and solutions detailed in this document are applicable to all the variants listed in the applicability table.

Obviously, this document cannot embrace every hardware solution or every product that can be designed. Where the suggested hardware configurations need not be considered mandatory, the information given should be used as a guide and a starting point for properly developing your product with the Telit module.

1.2. Audience

This document is intended for Telit customers, who are integrators, about to implement their applications using our GL865-QUAD V4 modules.

1.3. Contact Information, Support

For general contact, technical support services, technical questions and report documentation errors contact Telit Technical Support at:

- TS-EMEA@telit.com
- TS-AMERICAS@telit.com
- TS-APAC@telit.com
- TS-SRD@telit.com

Alternatively, use:

http://www.telit.com/support

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

http://www.telit.com

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

1.4. Text Conventions

Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

1.5. Related Documents

2. GENERAL PRODUCT DESCRIPTION

2.1. Overview

The GL865-QUAD V4 module is a quad-band 850/900/1800/1900 MHz GSM / GPRS communication product which allows integrators to plan on availability for even the longest lifecycle applications, highly recommended for new designs specified for 2G coverage worldwide.

The product is fully voice capable, the analog audio interface make it suitable for applications such as voice enabled alarm panels, mHealth patient monitors and specialty phones such as those for the elderly or sensory-impaired.

The GL865-QUAD V4 operates with 2.8 V GPIOs, minimizing power consumption and making it even more ideally suited for battery powered and wearable device applications.

2.2. Product Variants and Frequency Bands

Product	2G Band (MHz)	3G Band (MHz)	4G Band (MHz)	Region
GL865-QUAD V4	850, 900, 1800, 1900	-	-	-

Refer to “RF Section” for details information about frequencies and bands.

2.3. Target Market

GL865-QUAD V4 can be used for telematics applications where tamper-resistance, confidentiality, integrity, and authenticity of end-user information are required, for example:

- Emergency call
- Telematics services
- Road pricing
- Pay-as-you-drive insurance
- Stolen vehicles tracking
- Internet connectivity

2.4. Main features

Function	Features
Modem	• 2G (GSM/GPRS) Quad Band • SMS support (text and PDU) • Alarm management • Real Time Clock
Audio	• Analog audio
Intefaces	• Main UART is typically used for AT command access • Secondary UARTused for Diagnostic monitoring and debugging • 8 GPIOs • Antenna port

2.5. TX Output Power

Band	Power Class
850/900 MHz	Class 4 (2W)
1800/1900 MHz	Class 1 (1W)

2.6. RX Sensitivity

Band	Sensitivity (dBm)
850 MHz	-110
900 MHz	-110
1800 MHz	-110
1900 MHz	-108

2.7. Mechanical Specifications

2.7.1. Dimensions

The overall dimensions of GL865-QUAD V4 are:

- Length: 24.4 mm
- Width: 24.4 mm
- Thickness: 2.6 mm

2.7.2. Weight

The nominal weight of the module is 2.6 grams.

2.8. Temperature Range

		Note
Operating Temperature Range	–40°C ÷ +85°C	The module is fully functional(*) in all the temperature range, and it fully meets the 3GPP specifications.
Storage and non-operating Temperature Range	–40°C ÷ +85°C	

(*) Functional: the module is able to make and receive voice calls, data calls, SMS and make data traffic.

3. PINS ALLOCATION

Warning: GL865-QUAD V4 is adopting a modified 56-pin xL865 Form Factor, pin to pin compatible with the previous 48-pin xL865 FF and with 8 additional pads.

The numbering of the pins has been changed accordingly and attention has to be paid when comparing with previous 48-pin xL865 FF design.

3.1. Pin-out

Pin	Signal	I/O	Function	Type	Comment
Audio					
24	EAR-	O	Earphone signal (-)	Audio	
25	EAR+	O	Earphone signal (+)	Audio	
26	MIC-	I	Microphone signal (-)	Audio	
28	MIC+	I	Microphone signal (+)	Audio	
23	GND	-		-	
SIM card interface					
11	SIMVCC	-	External SIM signal - Power supply for the SIM	1.8 / 3V	
12	SIMRST	O	External SIM signal - Reset	1.8 / 3V	
13	SIMCLK	O	External SIM signal – Clock	1.8 / 3V	
14	SIMIO	I/O	External SIM signal - Data I/O	1.8 / 3V	

Asynchronous Auxiliary Serial Port				
53	TX_AUX	O	Auxiliary UART (TX Data to DTE)	CMOS 2.8V
52	RX_AUX	I	Auxiliary UART (RX Data from DTE)	CMOS 2.8V
Prog. / Data + HW Flow Control				
1	C109/DCD	O	Output for Data carrier detect signal (DCD) to DTE	CMOS 2.8V
2	C125/RING	O	Output for Ring indicator signal (RI) to DTE	CMOS 2.8V
3	C107/DSR	O	Output for Data set ready signal (DSR) to DTE	CMOS 2.8V
4	C108/DTR	I	Input for Data terminal ready signal (DTR) from DTE	CMOS 2.8V
5	C105/RTS	I	Input for Request to send signal (RTS) from DTE	CMOS 2.8V
6	C106/CTS	O	Output for Clear to send signal (CTS) to DTE	CMOS 2.8V
9	C103/TXD	I	Serial data input from DTE	CMOS 2.8V
10	C104/RXD	O	Serial data output to DTE	CMOS 2.8V
DIGITAL IO				
48	GPIO_01	I/O	GPIO_01	CMOS 2.8V
47	GPIO_02	I/O	GPIO_02	CMOS 2.8V
46	GPIO_03	I/O	GPIO_03	CMOS 2.8V

45	GPIO_04	I/O	GPIO_04	CMOS 2.8V
33	GPIO_05	I/O	GPIO_05	CMOS 2.8V
32	GPIO_06	I/O	GPIO_06	CMOS 2.8V
31	GPIO_07	I/O	GPIO_07	CMOS 2.8V
30	GPIO_08	I/O	GPIO_08	CMOS 2.8V
ADC				
15	ADC_IN1	AI	Analog / Digital converter input	A/D
16	ADC_IN2	AI	Analog / Digital converter input	A/D
DAC				
17	DAC_OUT	AO	Digital/Analog converter output	D/A
RF SECTION				
40	ANTENNA	I/O	Main Antenna (50 ohm)	RF
Miscellaneous Functions				
34	VRTC	AO	VRTC Backup	2.8V
55	RESET*	I	Reset Input	1.8V
51	VAUX	O	Supply Output for external accessories / Power ON Monitor	2.8V
Power Supply				

44	VBATT	-	Main power supply (Baseband)	Power
43	VBATT_PA	-	Main power supply (Radio PA)	Power
27	GND	-	Ground	Power
21	GND	-	Ground	Power
38	GND	-	Ground	Power
39	GND	-	Ground	Power
41	GND	-	Ground	Power
42	GND	-	Ground	Power
54	GND	-	Ground	Power
RESERVED				
7	RESERVED	-	RESERVED	
8	RESERVED	-	RESERVED	
18	RESERVED	-	RESERVED	
19	RESERVED	-	RESERVED	
20	RESERVED	-	RESERVED	
22	RESERVED	-	RESERVED	
29	RESERVED	-	RESERVED	
35	RESERVED	-	RESERVED	
36	RESERVED	-	RESERVED	
37	RESERVED	-	RESERVED	

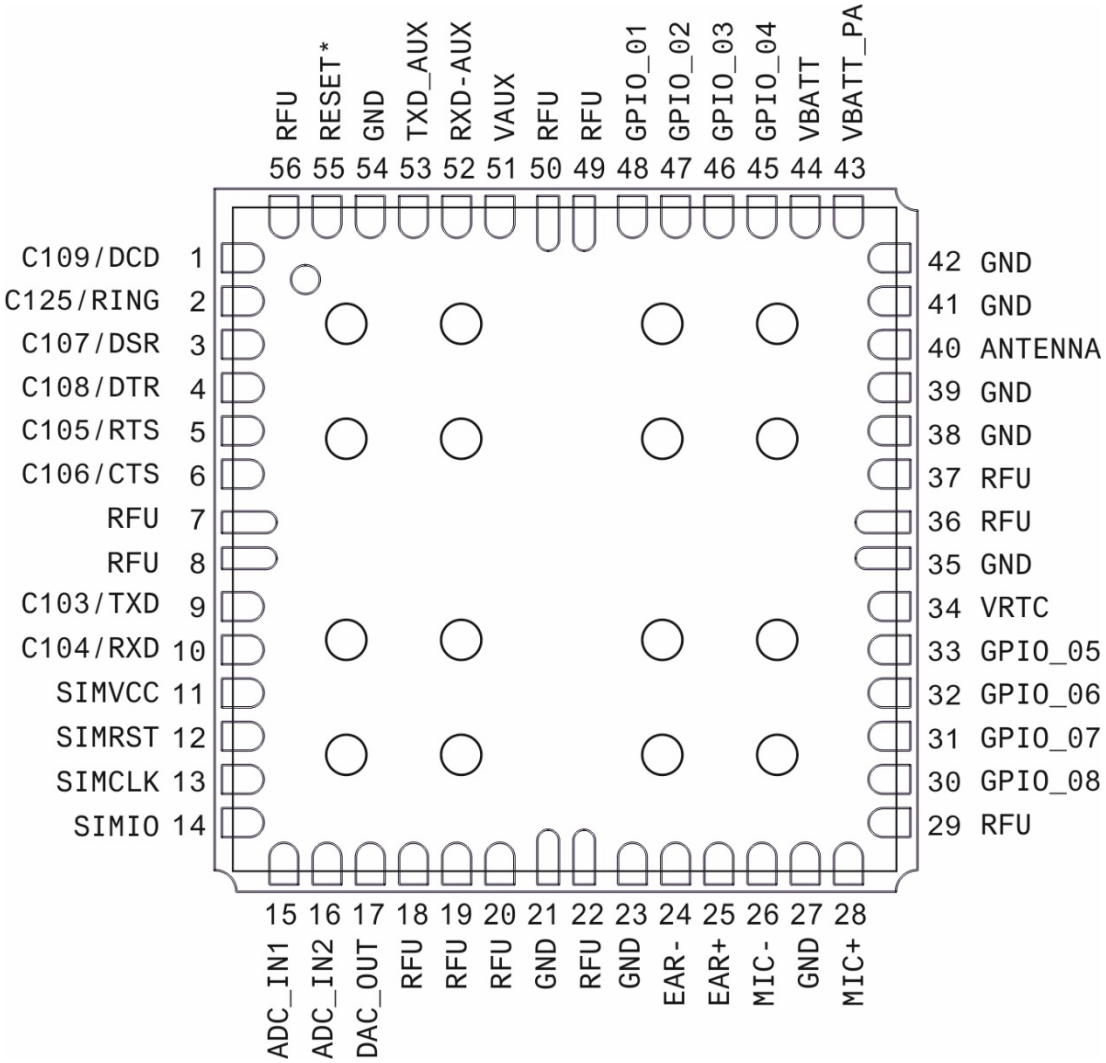
49	RESERVED	-	RESERVED
50	RESERVED	-	RESERVED
56	RESERVED	-	RESERVED

WARNING:

Reserved pins must not be connected.

3.2. VQFN Pads Layout

TOP VIEW



4. POWER SUPPLY

The power supply circuitry and board layout are a very important part in the full product design and they strongly reflect on the product overall performances, hence read carefully the requirements and the guidelines that will follow for a proper design.

4.1. Power Supply Requirements

The external power supply must be connected to VBATT & VBATT_PA signals and must fulfil the following requirements:

Power Supply	Value
Nominal Supply Voltage	3.8V
Normal Operating Voltage Range	3.40 V÷ 4.20 V

NOTE:

The Operating Voltage Range MUST never be exceeded; care must be taken when designing the application's power supply section to avoid having an excessive voltage drop. If the voltage drop is exceeding the limits it could cause a Power Off of the module.

4.2. Power Consumption

The values reported in the following table have been measured in nominal conditions (3.8V@25°C) with 5% max error:

Mode	Band	Average (mA)	Mode Description
IDLE mode			
AT+CFUN=1	All	13 (DRX9)	Power Saving Disabled (+ESLP=0)
AT+ESLP=1	All	1 (DRX9)	Power Saving Enabled See AT Commands Guide
Operative Mode			
GSM Voice Call	GSM900	220	PCL5
	DCS1800	145	PCL0
GPRS Data Call	GSM900	360	PS Class 10 @ Gamma3
	DCS1800	210	

The GSM system is made in a way that the RF transmission is not continuous, but it is packed into bursts at a base frequency of approx. 217 Hz, and the relative current peaks can be as high as about 2A. Therefore the power supply has to be designed to withstand these current peaks without big voltage drops; this means that both the electrical design and the board layout must be designed for this current flow.

If the layout of the PCB is not well designed a strong noise floor is generated on the ground and the supply; this will reflect on all the audio paths producing an audible annoying noise at approx. 217 Hz; if the voltage drop during the peak current absorption is too much, then the device may even shutdown as a consequence of the supply voltage drop.

NOTE:

The electrical design for the Power supply should be made ensuring it will be capable of a peak current output of at least 2A (3.80V supply).

4.3. General Design Rules

The principal guidelines for the Power Supply Design embrace three different design steps:

- the electrical design
- the thermal design
- the PCB layout

4.3.1. Electrical Design Guidelines

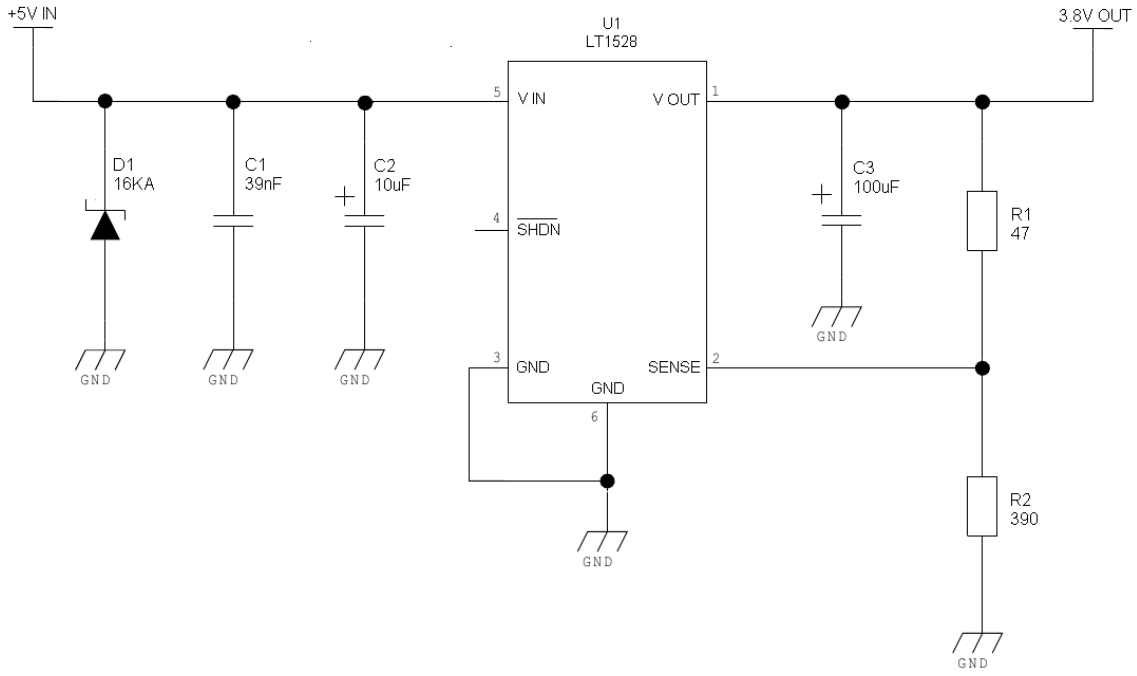
The electrical design of the power supply depends strongly from the power source where this power is drained. We will distinguish them into three categories:

- +5V input (typically PC internal regulator output)
- +12V input (typically automotive)
- Battery

4.3.1.1. +5V Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, hence there's not a big difference between the input source and the desired output and a linear regulator can be used. A switching power supply will not be suited because of the low drop out requirements.
- When using a linear regulator, a proper heat sink shall be provided in order to dissipate the power generated.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks close to the Module, a 100µF capacitor is usually suited.
- Make sure the low ESR capacitor on the power supply output rated at least 10V.

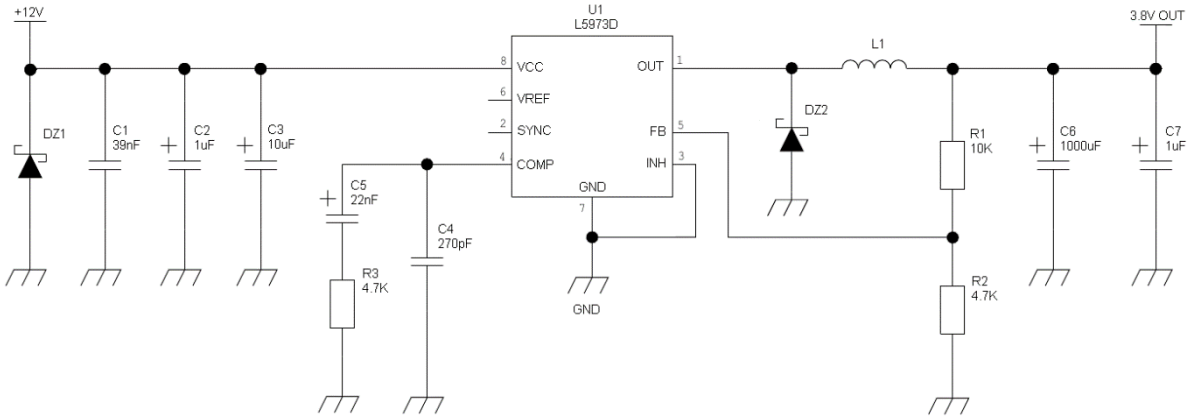
An example of linear regulator with 5V input is:



4.3.1.2. +12V Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, hence due to the big difference between the input source and the desired output, a linear regulator is not suited and shall not be used. A switching power supply will be preferable because of its better efficiency.
- When using a switching regulator, a 500kHz or more switching frequency regulator is preferable because of its smaller inductor size and its faster transient response. This allows the regulator to respond quickly to the current peaks absorption.
- In any case the frequency and Switching design selection is related to the application to be developed due to the fact the switching frequency could also generate EMC interferences.
- For car PB battery the input voltage can rise up to 15,8V and this should be kept in mind when choosing components: all components in the power supply must withstand this voltage.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100µF capacitor is usually suited.
- Make sure the low ESR capacitor on the power supply output is rated at least 10V.
- For Car applications a spike protection diode should be inserted close to the power input, in order to clean the supply from spikes.

An example of switching regulator with 12V input is in the below schematic:



4.3.1.3. Battery Source Power Supply Design Guidelines

The desired nominal output for the power supply is 3.8V and the maximum voltage allowed is 4.2V, hence a single 3.7V Li-Ion cell battery type is suited for supplying the power to the Telit GL865-QUAD V4 module.

- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100µF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor (usually a tantalum one) is rated at least 10V.
- A protection diode should be inserted close to the power input, in order to save the GL865-QUAD V4 from power polarity inversion. Otherwise the battery connector should be done in a way to avoid polarity inversions when connecting the battery.
- The battery must be rated to supply peaks of current up to 2A.

NOTE:

DON'T USE any Ni-Cd, Ni-MH, and Pb battery types directly connected with GL865-QUAD V4. Their use can lead to overvoltage on the GL865-QUAD V4 and damage it. USE ONLY Li-Ion battery types.

4.3.2. Thermal Design Guidelines

Worst case as reference values for thermal design of GL865-QUAD V4 are:

- Average current consumption: 500 mA
- Supply voltage: 3.80V

NOTE:

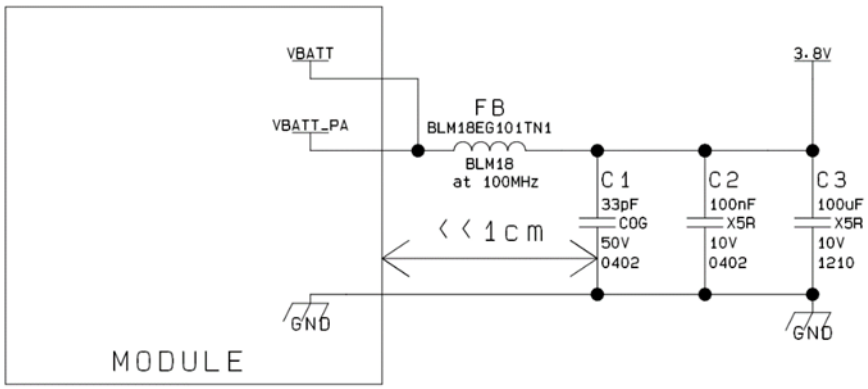
Make PCB design in order to have the best connection of GND pads to large surfaces.

4.3.3. Power Supply PCB layout Guidelines

As seen on the electrical design guidelines the power supply shall have a low ESR capacitor on the output to cut the current peaks on the input to protect the supply from spikes The placement of this component is crucial for the correct working of the circuitry. A misplaced component can be useless or can even decrease the power supply performance.

- The Bypass low ESR capacitor must be placed close to the Telit GL865-QUAD V4 power input pads or in the case the power supply is a switching type it can be placed close to the inductor to cut the ripple provided the PCB trace from the capacitor to the GL865-QUAD V4 is wide enough to ensure a dropless connection even during an 2A current peak.
- The protection diode must be placed close to the input connector where the power source is drained.
- The PCB traces to the GL865-QUAD V4 and the Bypass capacitor must be wide enough to ensure no significant voltage drops occur. This is for the same reason as previous point. Try to keep this trace as short as possible.
- To reduce the EMI due to switching, it is important to keep very small the mesh involved; thus the input capacitor, the output diode (if not embodied in the IC) and the regulator have to form a very small loop.This is done in order to reduce the radiated field (noise) at the switching frequency (100-500 kHz usually).
- A dedicated ground for the Switching regulator separated by the common ground plane is suggested.
- The placement of the power supply on the board should be done in such a way to guarantee that the high current return paths in the ground plane are not overlapped to any noise sensitive circuitry as the microphone amplifier/buffer or earphone amplifier.
- The power supply input cables should be kept separate from noise sensitive lines such as microphone/earphone cables.
- The insertion of EMI filter on VBATT pins is suggested in those designs where antenna is placed close to battery or supply lines. A ferrite bead like Murata BLM18EG101TN1 or Taiyo Yuden P/N FBMH1608HM101 can be used for this purpose.

The below figure shows the recommended circuit:



4.4. RTC

The VRTC pin brings out the Real Time Clock supply, which is separate from the rest of the digital part, allowing having only RTC going on when all the other parts of the device are off.

To this power output a backup battery can be added in order to increase the RTC autonomy during power off of the main battery (power supply). NO Devices must be powered from this pin.

For additional details on the Backup solutions please refer to the related application note (xL865 RTC Backup Application Note).

4.5. VAUX Power Output

A regulated power supply output is provided in order to supply small devices from the module. The signal is present on pin 51 and it is in common with the PWRMON (module powered ON indication) function.

This output is always active when the module is powered ON.

The operating range characteristics of the supply are:

Item	Min	Typical	Max
Output voltage	2.7V	2.8V	*2.9V*
Output current	-	-	10mA
Output bypass capacitor (inside the module)		1uF	

NOTE:

The Output Current MUST never be exceeded; care must be taken when designing the application section to avoid having an excessive current consumption.

If the Current is exceeding the limits it could cause a Power Off of the module.

NOTE:

VAUX max output current is shared with the other GPIOs for a maximum load of 10mA.

WARNING:

The current consumption from VAUX increases the modem temperature if the max output current is exceeded.

5. DIGITAL SECTION

5.1. Logic Levels

ABSOLUTE MAXIMUM RATINGS:

Parameter	Min	Max
Input level on any digital pin (CMOS 2.8) with respect to ground	-0.3V	+3.1V

OPERATING RANGE - INTERFACE VOLTAGE LEVELS (2.8V CMOS):

Parameter	Min	Max
Input high level	2.1V	3.1V
Input low level	0V	0.7V
Output high level	2.4V	3.1V
Output low level	0V	0.4V

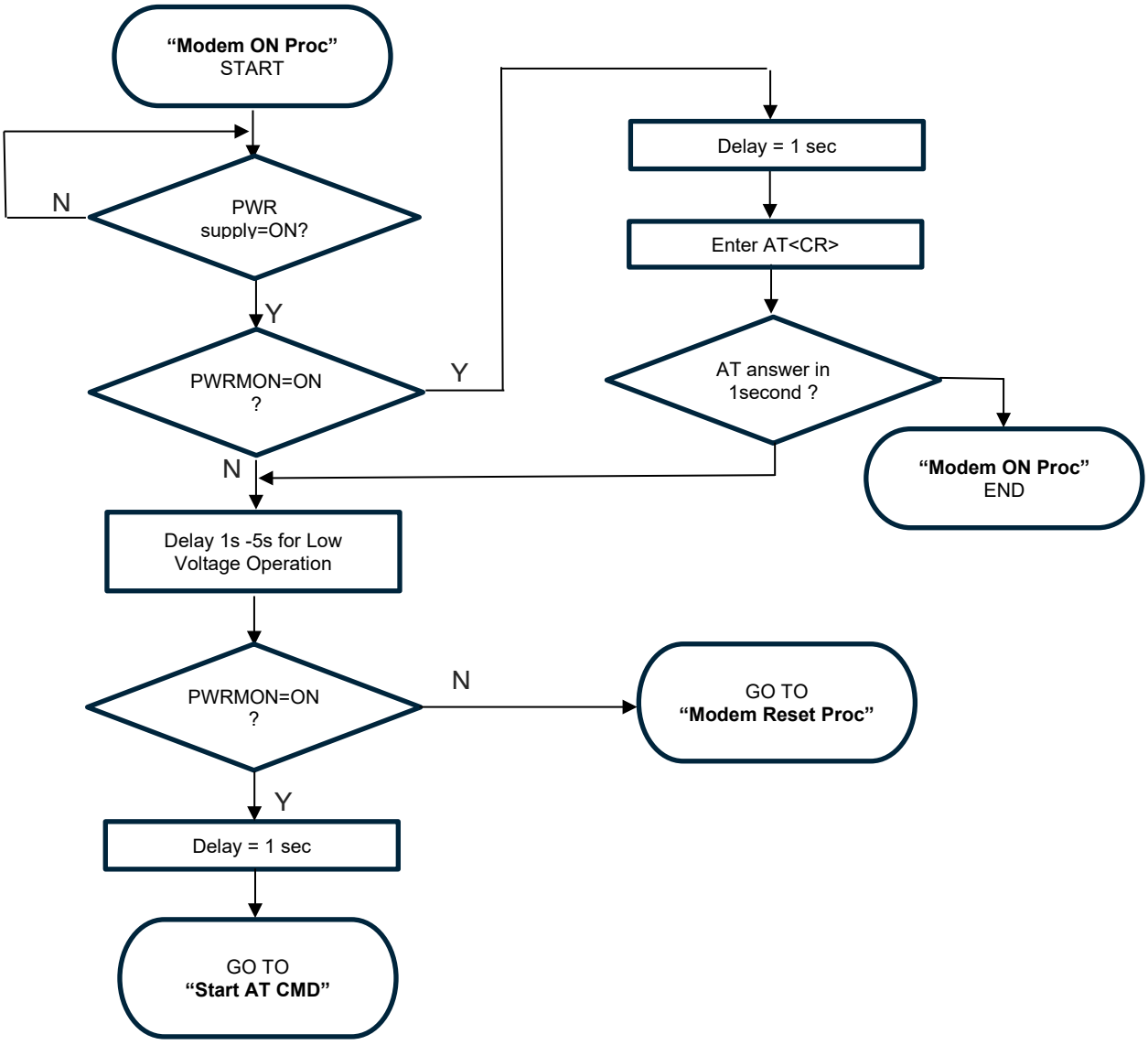
CURRENT CHARACTERISTICS:

Parameter	AVG
Output Current	1mA
Input Current	1uA

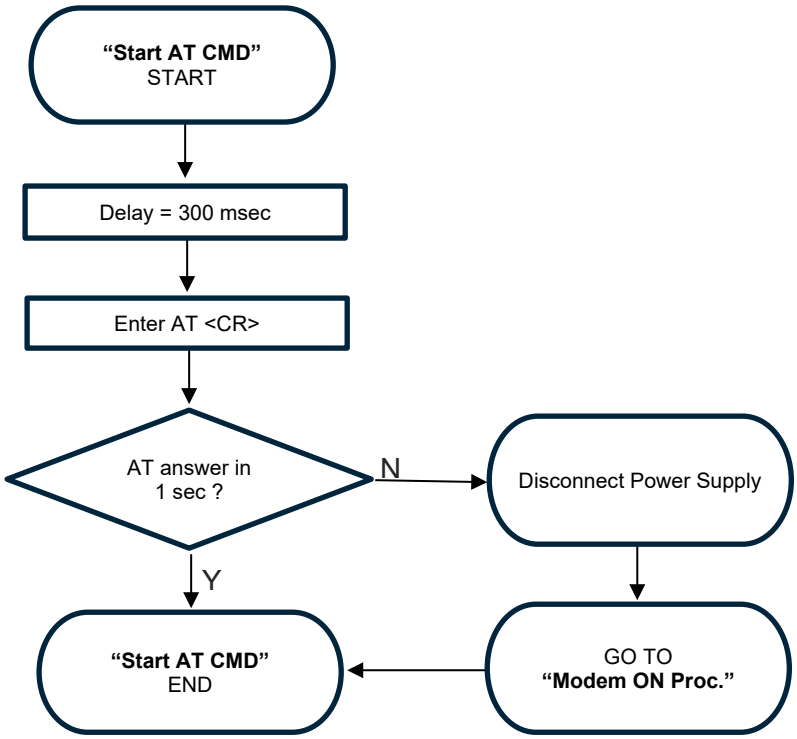
5.2. Auto-Turning ON

To Auto-turn on the GL865-QUAD V4, the power supply must be applied on the power pins VBATT and VBATT_PA, after 250 m-seconds, the VAUX pin will be at the high logic level and the module can be consider fully operating.

A flow chart (draft) showing the proper turn on procedure is displayed below:



A flow chart (draft) showing the AT commands managing procedure is displayed below:



NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the GL865-QUAD V4 when the module is powered off or during an ON/OFF transition.

5.3. Power Off

Turning off of the device can be done with General turn OFF.

General turn OFF – disconnect the power supply from the both power pins VBATT and VBATT_PA at the same time. In this case all parts of the module are in OFF condition, any power consumption is present.

NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the GL865-QUAD V4 when the module is powered off or during an ON/OFF transition.

5.4. Reset

RESET* is used to restart the GL865-QUAD V4. Whenever this signal is pulled low, the GL865-QUAD V4 is reset. When the device is reset it stops any operation. After the release of the line, the GL865-QUAD V4 is restarted, without doing any detach operation from the network where it is registered.

To restart the GL865-QUAD V4, the pad RESET* must be tied low for at least 200 milliseconds and then released.

The signal is internally pulled up so the pin can be left floating if not used.

If used, then it **must always be connected with an open collector transistor**, to permit to the internal circuitry the power on reset and under voltage lockout functions.

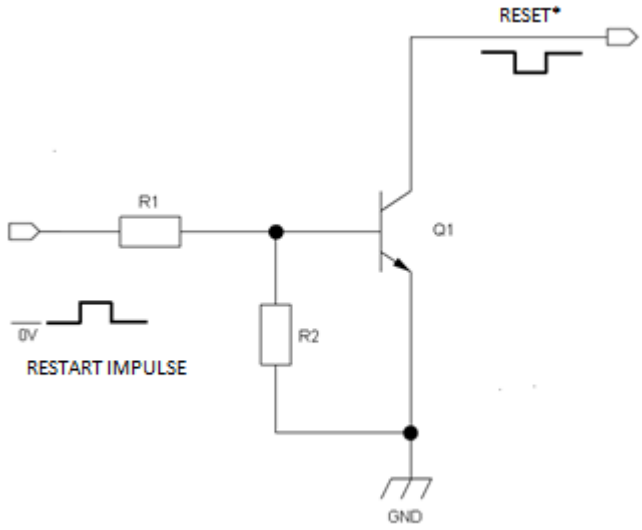
PINS DESCRIPTION

Signal	Function	I/O	PAD
RESET*	Restart of the Module	I	55

WARNING:

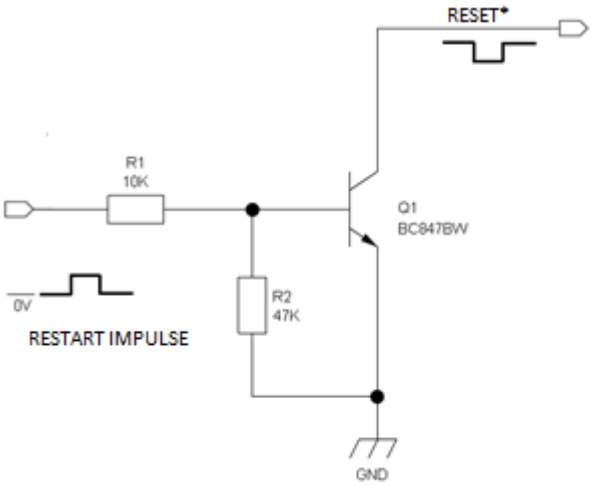
The hardware restart must not be used during normal operation of the device since it does not detach the device from the network. It shall be kept as an emergency exit procedure.

A typical circuit is the following:



For example:

Let us assume you need to drive the RESET* pad with a totem pole output of a +3/5 V microcontroller:



NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the GL865-QUAD V4 when the module is powered off or during an ON/OFF transition.

NOTE:

Do not use any pull up resistor on the RESET* line nor any totem pole digital output. Using pull up resistor may bring to latch up problems on the GL865-QUAD V4 power regulator and improper functioning of the module.

To proper power on again the module please refer to the related paragraph (“Power ON”)

The restart must always be implemented on the boards and should be used only as an emergency exit procedure.

5.5. Communication ports

5.5.1. Serial Ports

The GL865-QUAD V4 module is provided with by 2 Asynchronous serial ports:

- MODEM SERIAL PORT 1 (Main)
- MODEM SERIAL PORT 2 (Auxiliary)

Several configurations can be designed for the serial port on the OEM hardware, but the most common are:

- RS232 PC com port
- microcontroller UART @ 2.8V (Universal Asynchronous Receive Transmit)
- microcontroller UART @ 5V or other voltages different from 2.8V

Depending from the type of serial port on the OEM hardware a level translator circuit may be needed to make the system work. On the GL865-QUAD V4 the ports are CMOS 2.8.

5.5.1.1. Modem serial port 1 (USIF0)

The serial port 1 on the GL865-QUAD V4 is a +2.8V UART with all the 7 RS232 signals. It differs from the PC-RS232 in the signal polarity (RS232 is reversed) and levels.

The following table is listing the available signals:

RS232 Pin	Signal	Pad	Name	Usage
1	C109/DCD	1	Data Carrier Detect	Output from the GL865-QUAD V4 that indicates the carrier presence
2	C104/RXD	10	Transmit line *see Note	Output transmit line of GL865-QUAD V4 UART
3	C103/TXD	9	Receive line *see Note	Input receive of the GL865-QUAD V4 UART
4	C108/DTR	4	Data Terminal Ready	Input to the GL865-QUAD V4 that controls the DTE READY condition
5	GND	21, 38, 39, 41, 42, 54	Ground	Ground
6	C107/DSR	3	Data Set Ready	Output from the GL865-QUAD V4 that indicates the module is ready
7	C106/CTS	6	Clear to Send	Output from the GL865-QUAD V4 that controls the Hardware flow control

8	C105/RTS	5	Request to Send	Input to the GL865-QUAD V4 that controls the Hardware flow control
9	C125/RING	2	Ring Indicator	Output from the GL865-QUAD V4 that indicates the incoming call condition

NOTE:

According to V.24, some signal names are referred to the application side, therefore on the GL865-QUAD V4 side these signal are on the opposite direction:

TXD on the application side will be connected to the receive line (here named C103/TXD)

RXD on the application side will be connected to the transmit line (here named C104/RXD)

For a minimum implementation, only the TXD, RXD lines can be connected, the other lines can be left open provided a software flow control is implemented.

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the GL865-QUAD V4 when the module is powered off or during an ON/OFF transition.

5.5.1.2. Modem serial port 2 (USIF1)

The secondary serial port on the GL865-QUAD V4 is a CMOS 2.8V with only the RX and TX signals.

The signals of the GL865-QUAD V4 serial port are:

PAD	Signal	I/O	Function	Type	NOTE
53	TX_AUX	O	Auxiliary UART (TX Data to DTE)	CMOS 2.8V	
52	RX_AUX	I	Auxiliary UART (RX Data from DTE)	CMOS 2.8V	

NOTE:

Serial port 2 is currently used only for debug purposes.

NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the GL865-QUAD V4 when the module is powered off or during an ON/OFF transition.

5.6. General purpose I/O

The GL865-QUAD V4 module is provided by a set of Configurable Digital Input / Output pins (CMOS 2.8V). Input pads can only be read; they report the digital value (high or low) present on the pad at the read time. Output pads can only be written or queried and set the value of the pad output.

An alternate function pad is internally controlled by the GL865-QUAD V4 firmware and acts depending on the function implemented.

The following table shows the available GPIO on the GL865-QUAD V4:

PAD	Signal	I/O	Drive Strength	Default State	NOTE
48	GPIO_01	I/O	1 mA	INPUT	
47	GPIO_02	I/O	1 mA	INPUT	
46	GPIO_03	I/O	1 mA	INPUT	
45	GPIO_04	I/O	1 mA	INPUT	
33	GPIO_05	I/O	1 mA	INPUT	
32	GPIO_06	I/O	1 mA	INPUT	
31	GPIO_07	I/O	1 mA	INPUT	
30	GPIO_08	I/O	1 mA	INPUT	

5.6.1. Using a GPIO as INPUT

The GPIO pads, when used as inputs, can be connected to a digital output of another device and report its status, provided this device has interface levels compatible with the 2.8V CMOS levels of the GPIO.

NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the GL865-QUAD V4 when the module is powered off or during an ON/OFF transition.

5.6.2. Using a GPIO as OUTPUT

The GPIO pads, when used as outputs, can drive 2.8V CMOS digital devices or compatible hardware. When set as outputs, the pads have a push-pull output and therefore the pull-up resistor may be omitted.

5.7. External SIM Holder

Please refer to 0 the related User Guide (SIM Holder Design Guides, 80000NT10001a).

5.8. ADC Converter

The GL865-QUAD V4 is provided by two AD converter. It is able to read a voltage level in the range of 0÷2.8 volts applied on the ADC pin input, store and convert it into 10 bit word.

The input lines are named as **ADC_IN1** (available on Pad **15**) and **ADC_IN2** (available on Pad **16**).

The following table is showing the ADC characteristics:

Item	Min	Typical	Max	Unit
Input Voltage range	0	-	2.8	Volt
AD conversion	-	-	10	bits

5.8.1. Using ADC Converter

The ADC could be controlled using an AT command.

The command is **AT#ADC=1,2** to read ADC_IN1 and **AT#ADC=2,2** to read ADC_IN2.

The read value is expressed in mV

Refer to SW User Guide or AT Commands Reference Guide for the full description of this function.

5.9. DAC Converter

The GL865-QUAD V4 provides a Digital to Analog Converter. The signal (named DAC_OUT) is available on pin **17** of the GL865-QUAD V4. The on board DAC is a 10 bit converter, able to generate an analogue value based on a specific input in the range from 0 up to 1023. However, an external low-pass filter is necessary.

The following table is showing the ADC characteristics:

Item	Min	Max	Unit
Voltage range (filtered)	0	2.8	Volt
Range	0	1023	Steps

The precision is 10 bits so, if we consider that the maximum voltage is 2V, the integrated voltage could be calculated with the following formula:

Integrated output voltage = (2 *value) / 1023

DAC_OUT line must be integrated (for example with a low band pass filter) in order to obtain an analog voltage.

5.9.1. Enabling DAC

An *AT command* is available to use the DAC function.

The command is: **AT#DAC= [**<*enable*> **[,** <*value*>**]]**

<value> - scale factor of the integrated output voltage (0..1023 – 10 bit precision)

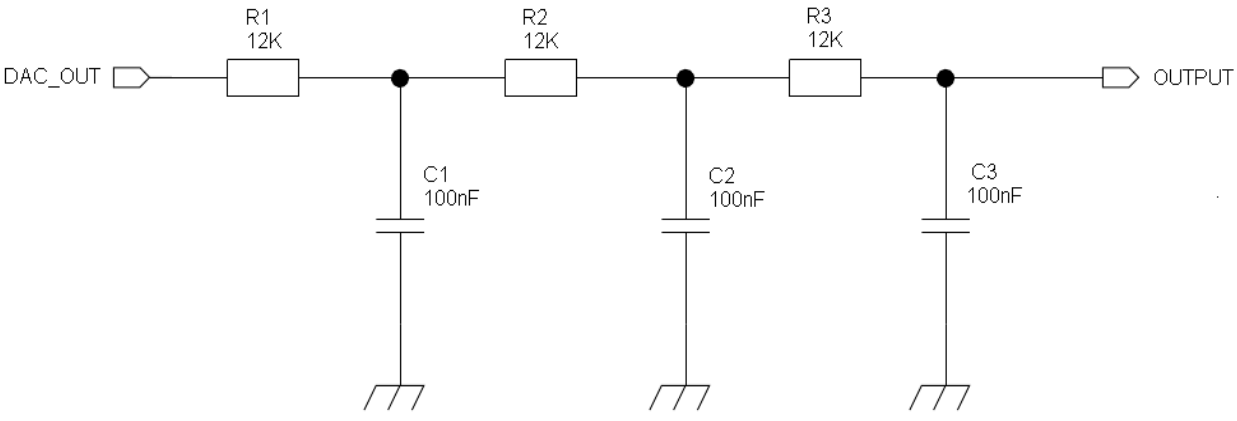
it must be present if ***<enable>=1***

Refer to SW User Guide or AT Commands Reference Guide for the full description of this function.

NOTE:

The DAC frequency is selected internally. D/A converter must not be used during POWERSAVING.

5.9.2. LOW Pass filter Example



6. RF SECTION

6.1. Bands Variants

The following table is listing the supported Bands:

Product	Supported 2G bands
GL865-QUAD V4	GSM900, GSM850, DCS1800, PCS1900

6.2. TX Output power

Product	Band	Power Class
GL865-QUAD V4	GSM900, GSM850, DCS1800, PCS1900	Class 4 (2W) @ 850/900 MHz, Class 1 (1W) @ 800/1900 MHz

6.3. Antenna requirements

The antenna connection and board layout design are the most important aspect in the full product design as they strongly affect the product overall performances, hence read carefully and follow the requirements and the guidelines for a proper design.

The antenna and antenna transmission line on PCB for a Telit GL865-QUAD V4 device shall fulfil the following requirements:

Item	Value
Frequency range	824-894 MHz GSM850 band 880-960 MHz GSM900 band 1710-1885MHz DCS1800 band 1850-1990MHz PCS1900 band
Gain	2.95dBi @GSM900 and 8.84dBi @DCS1800 2.95dBi @GSM850 and 8.84dBi @PCS1900
Impedance	50 ohm
Input power	> 2W
VSWR absolute max	≤ 10:1 (limit to avoid permanent damage)
VSWR recommended	≤ 2:1 (limit to fulfill all regulatory requirements)

6.3.1. PCB Design guidelines

When using the GL865-QUAD V4, since there's no antenna connector on the module, the antenna must be connected to the GL865-QUAD V4 antenna pad by means of a transmission line implemented on the PCB.

This transmission line shall fulfil the following requirements:

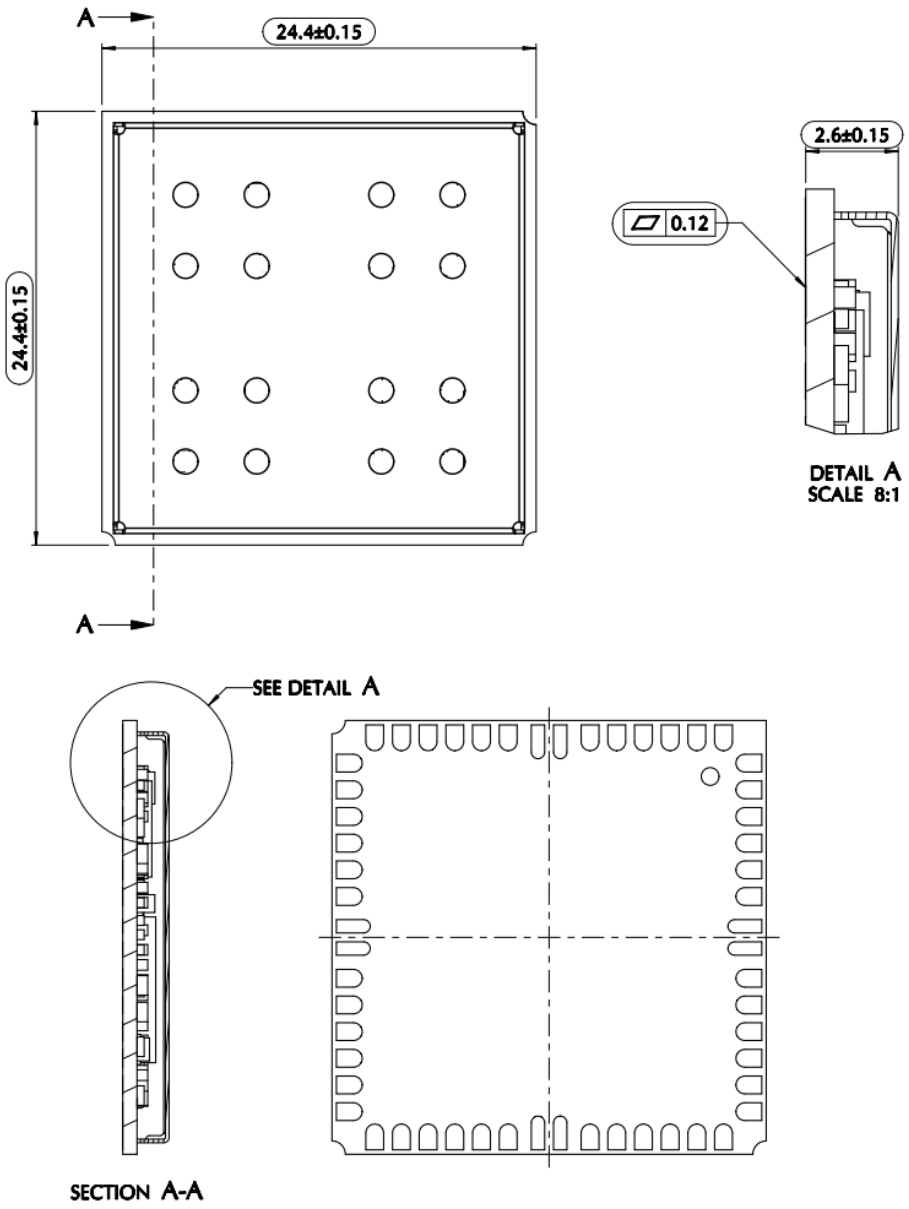
Item	Value
Characteristic Impedance	50 ohm (+-10%)
Max Attenuation	0,3 dB
Coupling	Coupling with other signals shall be avoided
Ground Plane	Cold End (Ground Plane) of antenna shall be equipotential to the GL865-QUAD V4 ground pins

The transmission line should be designed according to the following guidelines:

- Make sure that the transmission line's characteristic impedance is 50ohm ;
- Keep line on the PCB as short as possible, since the antenna line loss shall be less than about 0,3 dB;
- Line geometry should have uniform characteristics, constant cross section, avoid meanders and abrupt curves;
- Any kind of suitable geometry / structure (Microstrip, Stripline, Coplanar, Grounded Coplanar Waveguide...) can be used for implementing the printed transmission line afferent the antenna;
- If a Ground plane is required in line geometry, that plane has to be continuous and sufficiently extended, so the geometry can be as similar as possible to the related canonical model;
- Keep, if possible, at least one layer of the PCB used only for the Ground plane; If possible, use this layer as reference Ground plane for the transmission line;
- It is wise to surround (on both sides) the PCB transmission line with Ground, avoid having other signal tracks facing directly the antenna line track.
- Avoid crossing any un-shielded transmission line footprint with other signal tracks on different layers;
- The ground surrounding the antenna line on PCB has to be strictly connected to the main Ground Plane by means of via holes (once per 2mm at least), placed close to the ground edges facing line track;
- Place EM noisy devices as far as possible from GL865-QUAD V4 antenna line;
- Keep the antenna line far away from the GL865-QUAD V4 power supply lines;
- If EM noisy devices (such as fast switching ICs, LCD and so on) are present on the PCB hosting the LE910, take care of the shielding of the antenna line by burying it in an inner layer of PCB and surround it with Ground planes, or shield it with a metal frame cover.
- If EM noisy devices are not present around the line, the use of geometries like Microstrip or Grounded Coplanar Waveguide has to be preferred, since they typically ensure less attenuation if compared to a Stripline having same length;

7. MECHANICAL DESIGN

7.1. Drawing



NOTE:

Dimensions in mm.

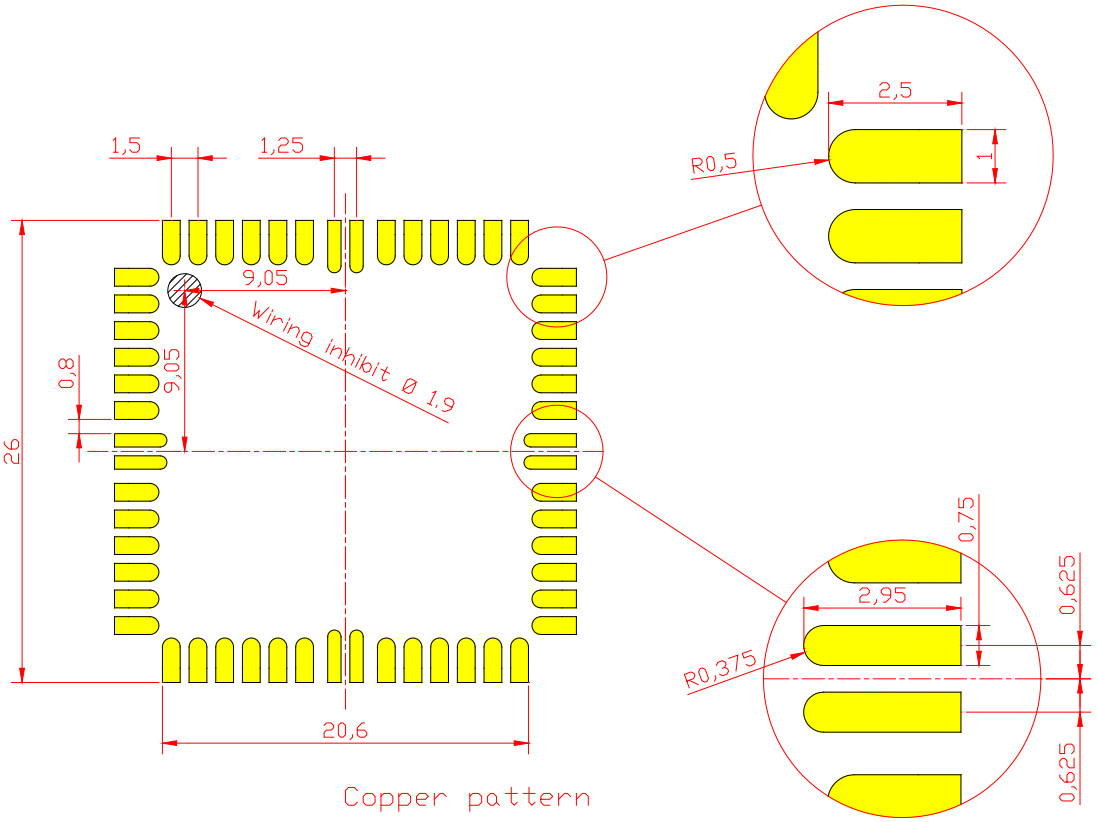
General Tolerance ±0.1, Angular Tolerance ±1°, The tolerance is not cumulative.

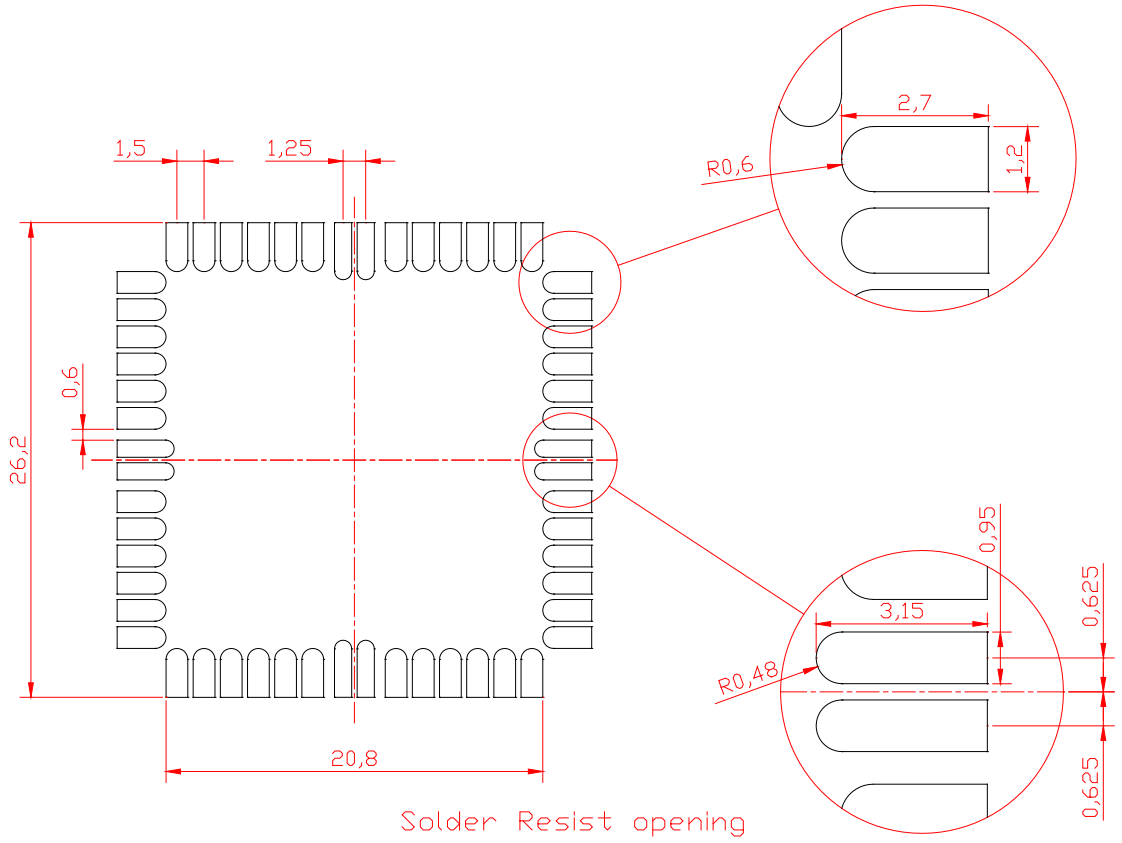
8. APPLICATION PCB DESIGN

The GL865-QUAD V4 modules have been designed in order to be compliant with a standard lead-free SMT process.

8.1. Footprint

TOP VIEW





In order to easily rework the GL865-QUAD V4 is suggested to consider on the application a 1.5 mm placement inhibit area around the module.

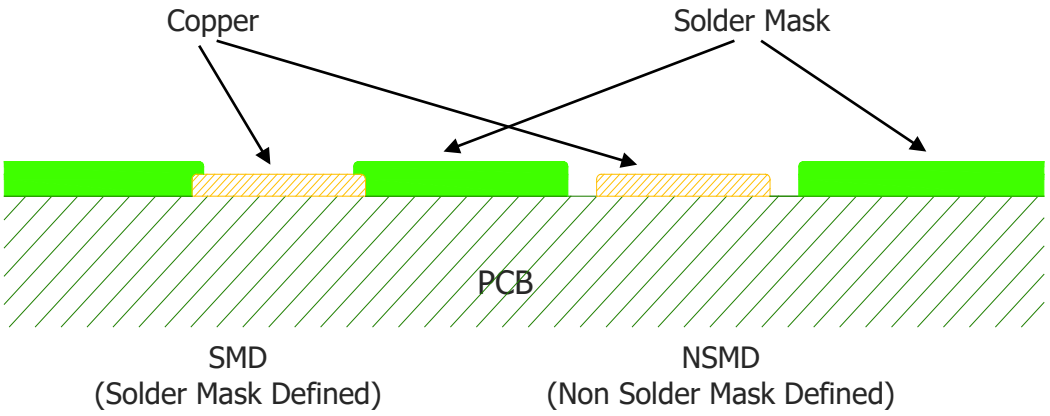
It is also suggested, as common rule for an SMT component, to avoid having a mechanical part of the application in direct contact with the module.

NOTE:

In the customer application, the region under WIRING INHIBIT (see figure above) must be clear from signal or ground paths.

8.2. PCB pad design

Non solder mask defined (NSMD) type is recommended for the solder pads on the PCB.



8.3. PCB pad dimensions

The recommendation for the PCB pads dimensions are 1:1 with module pads.

It is not recommended to place via or micro-via not covered by solder resist in an area of 0,3 mm around the pads unless it carries the same signal of the pad itself

Holes in pad are allowed only for blind holes and not for through holes.

Recommendations for PCB pad surfaces:

Finish	Layer Thickness (um)	Properties
Electro-less Ni / Immersion Au	3 –7 / 0.03 – 0.15	good solder ability protection, high shear force values

The PCB must be able to resist the higher temperatures which are occurring at the lead-free process. This issue should be discussed with the PCB-supplier. Generally, the wettability of tin-lead solder paste on the described surface plating is better compared to lead-free solder paste.

It is not necessary to panel the application's PCB, however in that case it is suggested to use milled contours and predrilled board breakouts; scoring or v-cut solutions are not recommended.

8.4. Stencil

Stencil's apertures layout can be the same of the recommended footprint (1:1), we suggest a thickness of stencil foil ≥ 120 µm.

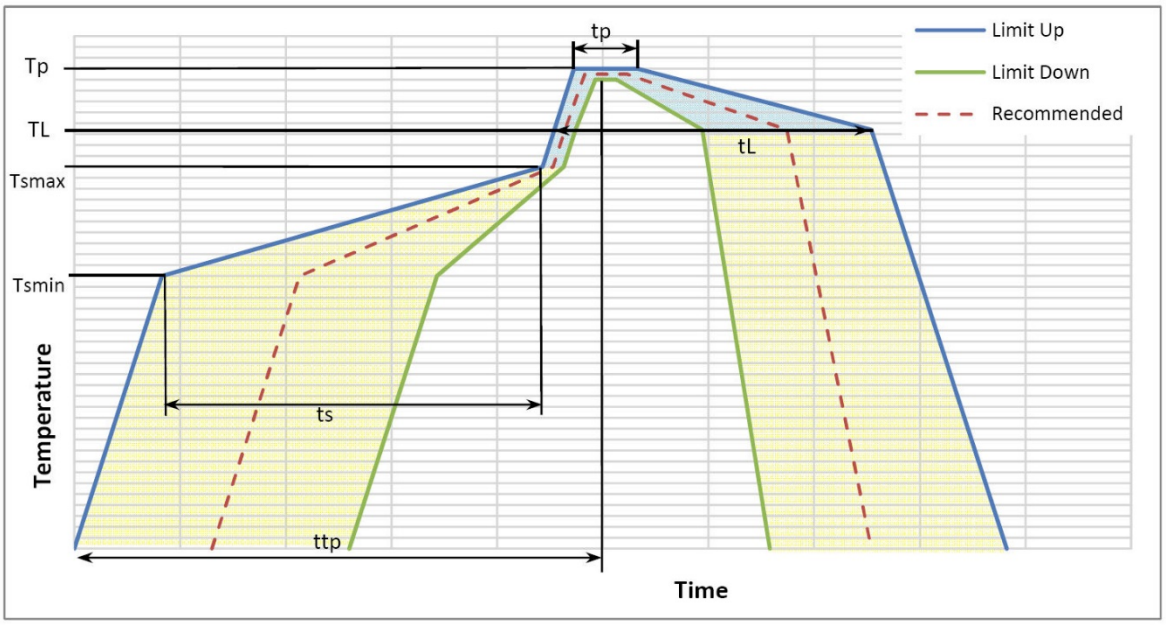
8.5. Solder paste

Item	Lead Free
Solder Paste	Sn/Ag/Cu

We recommend using only "no clean" solder paste in order to avoid the cleaning of the modules after assembly.

8.6. Solder Reflow

Recommended solder reflow profile:



Profile Feature	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max
Preheat **– Temperature Min (Tsmin)** **– Temperature Max (Tsmax)** **– Time (min to max) (ts)**	 150°C 200°C 60-180 seconds
Tsmax to TL **– Ramp-up Rate**	3°C/second max
Time maintained above: **– Temperature (TL)** **– Time (tL)**	 217°C 60-150 seconds
Peak Temperature (Tp)	245 +0/-5°C
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds
Ramp-down Rate	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

NOTE:

All temperatures refer to topside of the package, measured on the package body surface

WARNING:

THE GL865-QUAD V4 MODULE WITHSTANDS ONE REFLOW PROCESS ONLY.

WARNING:

The above solder reflow profile represents the typical SAC reflow limits and does not guarantee adequate adherence of the module to the customer application throughout the temperature range. Customer must optimize the reflow profile depending on the overall system taking into account such factors as thermal mass and warpage.

9. SAFETY RECOMMENDATIONS

9.1. READ CAREFULLY

Be sure the use of this product is allowed in the country and in the environment required. The use of this product may be dangerous and has to be avoided in the following areas:

- Where it can interfere with other electronic devices in environments such as hospitals, airports, aircrafts, etc.
- Where there is risk of explosion such as gasoline stations, oil refineries, etc. It is responsibility of the user to enforce the country regulation and the specific environment regulation.

Do not disassemble the product; any mark of tampering will compromise the warranty validity. We recommend following the instructions of the hardware user guides for a correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to be conforming to the security and fire prevention regulations. The product has to be handled with care, avoiding any contact with the pins because electrostatic discharges may damage the product itself. Same cautions have to be taken for the SIM, checking carefully the instruction for its use. Do not insert or remove the SIM when the product is in power saving mode.

The system integrator is responsible of the functioning of the final product; therefore, care has to be taken to the external components of the module, as well as of any project or installation issue, because the risk of disturbing the network or external devices or having impact on the security. Should there be any doubt, please refer to the technical documentation and the regulations in force. Every module has to be equipped with a proper antenna with specific characteristics. The antenna has

to be installed with care in order to avoid any interference with other electronic devices and has to guarantee a minimum distance from the body (20 cm). In case of this requirement cannot be satisfied, the system integrator has to assess the final product against the SAR regulation.

The European Community provides some Directives for the electronic equipment introduced on the market. All the relevant information’s are available on the European Community website:

http://ec.europa.eu/enterprise/sectors/rtte/documents/

The text of the Directive 99/05 regarding telecommunication equipment is available, while the applicable Directives (Low Voltage and EMC) are available at:

http://ec.europa.eu/enterprise/sectors/electrical/

10. ACRONYMS

LTE	Long Term Evolution
RF	Radio Frequency
EMC	Electromagnetic Compatibility
FDD	Frequency Division Duplexing
EM	Electromagnetic
EMI	Electromagnetic Interference
PCB	Printed Circuit Board
USB	Universal Serial Bus
HS	High Speed
DTE	Data Terminal Equipment
UMTS	Universal Mobile Telecommunication System
WCDMA	Wideband Code Division Multiple Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
UART	Universal Asynchronous Receiver Transmitter
HSIC	High Speed Inter Chip
SIM	Subscriber Identification Module
SPI	Serial Peripheral Interface
ADC	Analog – Digital Converter
DAC	Digital – Analog Converter
I/O	Input Output

GPIO	General Purpose Input Output
CMOS	Complementary Metal – Oxide Semiconductor
MOSI	Master Output – Slave Input
MISO	Master Input – Slave Output
CLK	Clock
MRDY	Master Ready
SRDY	Slave Ready
CS	Chip Select
RTC	Real Time Clock
ESR	Equivalent Series Resistance
VSWR	Voltage Standing Wave Radio
VNA	Vector Network Analyzer
PSM	Power Saving Mode according to 3GPP Rel.12
NAS	Non-Access Stratum

11. DOCUMENT HISTORY

Revision	Date	Changes
0	2018-03-07	First issue
1	2018-06-28	Adding ADC_IN1 and DAC support
2	2018-10-25	Review of chapter 2 Adding Power Consumption figures Updating Antenna gain requirements Review of par 4.3.3
3	2019-04-05	Warning note added to par 8.6
4	2020-09-17	Updated Chapter 2.GENERAL PRODUCT DESCRIPTION Updated audio interface Updated Chapter 4.2 Power Consumption

SUPPORT INQUIRIES

Link to **www.telit.com** and contact our technical support team for any questions related to technical issues.

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