GS2200M Low Power Wi-Fi Module Hardware User Guide

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Table of Contents

About This Manual

This manual describes the GS2200M Low Power module hardware specification.

Refer to the following sections:

Revision History

This version of the *GainSpan GS2200M Low Power WiFi Module Hardware user Guide* contains the following new information listed in Table 1, page 4.

Table 1 Revision History

Version	Date	Remarks
0.95	May 3015	Initial Preliminary Release
0.96	July 2015	Second Preliminary Draft with changes to Figure 1, page 18 to include additional ADC 16-bit. Updated RTC features, 2.2.5.1 RTC Main Features, page 23. Updated Power Supply diagrams, 2.2.8 Power Supply, page 32. Color-coded Pin MUX Description, Table 9, page 42. Updated 802.11 Output Power, Table 17, page 51. Added new package layout diagrams, Figure 9, page 56, Figure 10, page 57, and Figure 11, page 58.
0.97	December 2015	Updated the following sections: • 1.2 GS2200M Module Product Features, page 13 • 2.1 Architecture Description, page 17 Updated the following figures: • Figure 7GS2200M Battery Powered with Optimized Standby Support, page 35 • Figure 4GS2200M Always ON Power Supply Connection, page 32 • Figure 8GS2200M Device Pin-out Diagram (Module Top View), page 37 • Figure 9GS2200M Module Dimensions (in millimeters), page 56 • Figure 10GS2200M Module Dimensions (in millimeters) - (Continued), page 57 • Figure 11GS2200M Module Recommended PCB Footprint (in millimeters), page 58 Updated the following tables: • Table 8GS2200M Module Pin Signal Description, page 38 • Table 10GS2100M Pin Program and Code Restore, page 44 • Table 12Operating Conditions, page 46 • Table 16Typical Power Consumption in Different States, page 50 • Table 17802.11 Radio Parameters - (Typical - Nominal Conditions), page 51 Added the following figures: Figure 5GS2200M Regulator Powered with Optimized Standby Only, page 33 Figure 6GS2200M Regulator Powered with Optimized Standby and Radio Power, page 34

Table 1 Revision History (Continued)

Version	Date	Remarks
0.98	March 2016	Updated 802.11 Output Power, Receive sensitivity, Table 17, page 51.
0.99	December 2016	Updated DeepSleep current supply value in Table 16Typical Power Consumption in Different States, page 50
1.0	June 2017	Updated the table for typical Power Consumption in Different States, See Table 16, page 50

Audience

This manual is designed to help system designers build low power, cost effective, flexible platforms to add WiFi connectivity for embedded device applications using the GainSpan GS2200M based module.

Standards

The standards supported by the GainSpan module are IEEE 802.11 b/g/n.

Certifications

GainSpan GS2200M Low Power WiFi Module has Certification Compliance for the following:

Table 2 Certification Compliance

Category	Certification
Radio regulatory Certificates	FCC, IC, CE, TELEC
Wi-Fi Alliance Certificates	WPS 2.0, WMM, WMM-PS, WPA and WPA2 Enterprise, WPA and WPA2 Personal.

Documentation Conventions

This manual uses the following text and syntax conventions:

- Special text fonts represent particular commands, keywords, variables, or window sessions
- Color text indicates cross-reference hyper links to supplemental information
- Command notation indicates commands, subcommands, or command elements

Table 3, page 6, describes the text conventions used in this manual for software procedures that are explained using the AT command line interface.

Table 3 Document Text Conventions

Convention Type	Description
command syntax monospaced font	This monospaced font represents command strings entered on a command line and sample source code. `AT XXXX`
Proportional font description	Gives specific details about a parameter. `<Data> DATA`
UPPERCASE Variable parameter	Indicates user input. Enter a value according to the descriptions that follow. Each uppercased token expands into one or more other token.
lowercase Keyword parameter	Indicates keywords. Enter values exactly as shown in the command description.
[ ] Square brackets	Enclose optional parameters. Choose none; or select one or more an unlimited number of times each. Do not enter brackets as part of any command. `[parm1|parm2|parm3]`
? Question mark	Used with the square brackets to limit the immediately following token to one occurrence.
<ESC> Escape sequence	Each escape sequence <ESC> starts with the ASCII character 27 (0x1B). This is equivalent to the Escape key. `<ESC>C`
<CR> Carriage return	Each command is terminated by a carriage return.
<LF> Line feed	Each command is terminated by a line feed.
<CR> <LF> Carriage return Line feed	Each response is started with a carriage return and line feed with some exceptions.
< > Angle brackets	Enclose a numeric range, endpoints inclusive. Do not enter angle brackets as part of any command. `<SSID>`
= Equal sign	Separates the variable from explanatory text. Is entered as part of the command. `PROCESSID = <CID>`

Table 3 Document Text Conventions (Continued)

Convention Type	Description
. dot (period)	Allows the repetition of the element that immediately follows it multiple times. Do not enter as part of the command. `.AA:NN can be expanded to 1:01 1:02 1:03.`
A.B.C.D IP address	IPv4-style address. `10.0.11.123`
X:X::X:X IPv6 IP address	IPv6-style address. `3ffe:506::1` Where the : : represents all 0x for those address components not explicitly given.
LINE End-to-line input token	Indicates user input of any string, including spaces. No other parameters may be entered after input for this token. `string of words`
WORD Single token	Indicates user input of any contiguous string (excluding spaces). `singlewordnospaces`

Table 4, page 8, describes the symbol conventions used in this manual for notification and important instructions.

Table 4 Symbol Conventions

Icon	Type	Description
	Note	Provides helpful suggestions needed in understanding a feature or references to material not available in the manual.
	Alert	Alerts you of potential damage to a program, device, or system or the loss of data or service.
	Caution	Cautions you about a situation that could result in minor or moderate bodily injury if not avoided.
	Warning	Warns you of a potential situation that could result in death or serious bodily injury if not avoided.
	Electro-Static Discharge (ESD)	Notifies you to take proper grounding precautions before handling a product.

Documentation

The GainSpan documentation suite listed in Table 5, page 9 includes the part number, documentation name, and a description of the document. The documents are available from the GainSpan Portal. Refer to Accessing the GainSpan Portal, page 12 for details.

Table 5 Documentation List

Part Number	Document Title	Description
GS2200M_QSG_SKB_001279	GainSpanGS2200M SKB Quick Start Guide	Provides an easy to follow guide on how to unpack and setup GainSpan GS2000 based module kit for the GS2200M modules.
GS2K-SKB-HW-UG-001278	GainSpan GS2200M SKB Hardware User Guide	Provides users steps to program the on-board Flash on the GainSpan GS2000 based modules using DOS or Graphical User Interface utility provided by GainSpan. The user guide uses the evaluation boards as a reference example board.
GS2200-S2W-ADP-CMD-RG-001208	GainSpan GS2000 Based Module GS2200M S2W Adapter Command Reference Guide	Provides a complete listing of AT serial commands, including configuration examples for initiating, maintaining, and evaluation GainSpan GS2200M Serial to Wi-Fi based modules.

Documentation Feedback

We encourage you to provide feedback, comments, and suggestions so that we can improve the documentation. You can send your comments by logging into GainSpan Support Portal. If you are using e-mail, be sure to include the following information with your comments:

- Document name
- URL or page number
- Hardware release version (if applicable)
- Software release version (if applicable)

Contacting GainSpan Technical Support

Use the information listed in Table 6, page 10, to contact the GainSpan Technical Support.

Table 6 GainSpan Technical Support Contact Information

North America	1 (408) 627-6500 - techsupport@gainspan.com
Outside North America	Europe: EUsupport@gainspan.com China: Chinasupport@gainspan.com Asia: Asiasupport@gainspan.com
Postal Address	GainSpan Corporation 3590 North First Street Suite 300 San Jose, CA 95134 U.S.A.

For more Technical Support information or assistance, perform the following steps:

1. Visit http://www.telit.com. and select “GainSpan Modules” which will direct to the GainSpan portal http://www.gainspan.com.
2. Click **Contact**, and click **Request Support**.
3. Log in using your customer **Email** and **Password**.
4. Select the **Location**.
5. Select **Support Question** tab.
6. Select **Add New Question**.
7. Enter your technical support question, product information, and a brief description.

The following information is displayed:

- Telephone number contact information by region
- Links to customer profile, dashboard, and account information
- Links to product technical documentation

- Links to PDFs of support policies

Returning Products to GainSpan

If a problem cannot be resolved by GainSpan technical support, a Return Material Authorization (RMA) is issued. This number is used to track the returned material at the factory and to return repaired or new components to the customer as needed.

NOTE: *Do not return any components to GainSpan Corporation unless you have first obtained an RMA number. GainSpan reserves the right to refuse shipments that do not have an RMA. Refused shipments will be returned to the customer by collect freight.*

For more information about return and repair policies, see the customer support web page at: https://www.gainspan.com/secure/login.

To return a hardware component:

1. Determine the part number and serial number of the component.
2. Obtain an RMA number from Sales/Distributor Representative.
3. Provide the following information in an e-mail or during the telephone call:
   - Part number and serial number of component
   - Your name, organization name, telephone number, and fax number
   - Description of the failure
4. The support representative validates your request and issues an RMA number for return of the components.
5. Pack the component for shipment.

Guidelines for Packing Components for Shipment

To pack and ship individual components:

- When you return components, make sure they are adequately protected with packing materials and packed so that the pieces are prevented from moving around inside the carton.
- Use the original shipping materials if they are available.
- Place individual components in electrostatic bags.
- Write the RMA number on the exterior of the box to ensure proper tracking.

CAUTION! *Do not stack any of the components.*

Accessing the GainSpan Portal

To find the latest version of GainSpan documentation supporting the GainSpan product release you are interested in, you can search the GainSpan Portal website by performing the following steps:

NOTE: *You must first contact GainSpan to set up an account, and obtain a customer user name and password before you can access the GainSpan Portal.*

1. Visit http://www.telit.com. and select “GainSpan Modules” which will direct to the GainSpan portal http://www.gainspan.com.
2. Log in using your customer **Email** and **Password**.
3. Click the **Getting Started** tab to view a Quick Start tutorial on how to use various features within the GainSpan Portal.
4. Click the **Actions** tab to buy, evaluate, or download GainSpan products.
5. Click on the **Documents** tab to search, download, and print GainSpan product documentation.
6. Click the **Software** tab to search and download the latest software versions.
7. Click the **Account History** tab to view customer account history.
8. Click the **Legal Documents** tab to view GainSpan Non-Disclosure Agreement (NDA).

Ordering Information

To order GainSpan’s GS2200M low power module contact a GainSpan Sales/Distributor Representative. Table 7, page 12 lists the GainSpan device information.

Table 7 GS2200M Ordering Information

Device Description	Ordering Number	Revision
Low power module with on-board antenna	GS2200MIZ	1.0

NOTE: *Modules ship with test code ONLY. Designers must first program the modules with a released firmware version. Designers should bring out GPIO27 pin (option to pull this pin to VDDIO during reset or power-on) and UART0 or SPI0 pins to enable programming of firmware into the module. For details refer to the Programming the GainSpan Modules document.*

Chapter 1 GS2200M Overview

This chapter describes the GainSpan® GS2200M low power module hardware specification overview.

1.1 Product Overview

The GS2200M low power based module provides cost effective, low power, **compact**, and flexible platform to add WiFi connectivity for embedded devices for a variety of applications, such as wireless sensors and thermostats. It uses GS2000 SoC, which combines ARM® Cortex M3-based processors with a 802.11b/g/n Radio, MAC, security, PHY functions, RTC and SRAM. The module includes 4 MB FLASH and on board certified antenna. The module provides a WiFi and regulatory certified IEEE 802.11b/g/n radio with concurrent network processing services for variety of applications, while leverage existing 802.11 wireless network infrastructures.

1.2 GS2200M Module Product Features

- GS2200M 13.5mm (0.53in) x 17.85 mm (0.70in) x 2.13mm (0.086in) 66-pin PCB Surface Mount Package. One SKU is:
  - GS2200MIZ (on-board antenna)
- Simple API for embedded markets covering a large range of applications
- Fully compliant with IEEE 802.11b/g/n and regulatory domains:
  - 802.11n: 1x1 single stream, 20 MHz channels, 400/800ns GI, MCS0 – 7
    - Data rates of 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65.0, 72.2 Mbps
  - 802.11g: OFDM modulation for data rates of 6, 9, 12, 18, 24, 36, 48 and 54 Mb/s
  - 802.11b: CCK modulation rates of 5.5 and 11 Mbps; DSSS modulation for data rate of 1 and 2 Mbps
- WiFi Solution:
  - WiFi security (802.11i)
    - WPA™ - Enterprise, Personal
    - WPA2™ - Enterprise, Personal
    - Vendor EAP Type(s):

  - EAP-TTLS/MSCHAPv2, PEAPv0/EAP-MSCHAPv2, PEAPv1/EAP-GTC, EAP-FAST, EAP-TLS

- Hardware-accelerated high-throughput AES and RC4 encryption/decryption engines for WEP, WPA/WPA2 (AES-CCMP and TKIP).
- Additional dedicated encryption HW engine to support higher layer encryption such as IPSEC (IPv4 and IPv6), SSL/TLS, HTTPs, PKI, digital certificates, RNG, etc.

- Dual ARM Cortex M3 Processor Platform:
  - 1st Cortex M3 processor (WLAN CPU) for WLAN software
    - Implements 802.11b/g/n WLAN protocol services
      - 320 KB dedicated SRAM
      - 512 KB dedicated ROM
  - 2nd Cortex M3 processor (APP CPU) for networking software
    - Implements networking protocol stacks and user application software
      - 384 KB dedicated SRAM
      - 512 KB dedicated ROM
  - 64KB shared dual ported SRAM for inter-processor communications
  - 320KB assignable (under SW control) SRAM
  - Support processor clock frequencies for both CPU of up to 120MHz
  - Based on Advanced Microprocessor Bus Architecture (AMBA) system
    - AMBA Multilayer High-Speed Bus (AHB)
    - AMBA Peripheral Bus (APB)
  - On-module controller
    - Manages read/write/program/erase operations to the 4 MB flash memory device on the module
    - Supports higher performance QUAD SPI protocol operations
    - Active power management

- Interfaces:
  - SDIO:
    - Compliant to SDIO v2.0 specification
    - Interface clock frequency up to 40 MHz

NOTE: *Tested with current test platform up to 33 MHz.*

    - Data transfer modes: 4-bit, 1-bit SDIO, SPI
    - Device mode only (slave)
  - SPI:
    - Two (2) general-purpose SPI interfaces (each configurable independently as master or slave)
    - The SPI pins are muxed with other functions such as GPIO
    - Supports clock rates of up to 30 MHz (master mode) and up to 10 MHz (slave mode)
    - Protocols supported include: Motorola SPI, TI Synchronous Serial Protocol (SSP) and National Semiconductor Microwire
    - Supports SPI mode 0 thru 3 (software configurable)
  - UART:
    - Two (2) multi-purpose UART interfaces operating in full-duplex mode
      - 16450/16550 compatible
      - Optional support for flow control using RTS/CTS signaling for high data transfer rates
      - Standard baud rate from 9600 bps up to 921.6 kbps (additional support for higher non-standard rates using baud rates up to 7.5 MHz
  - GPIOs:
    - Up to 19 configurable general purpose I/O
  - Single 3.3V supply option
  - Three (3) PWM outputs
  - I^2C master/slave interface
  - One 12-bit ADC channel, sample rate from 10 kS/s to 2 MS/s
  - One 16-bit Sigma Delta ADC channel, sample rate from 32 kS/s to 80 kS/s
  - Three (3) RTC pins that can be configured as:
    - Up to two alarm inputs to asynchronously awaken the chip.
    - Support of up to two timer controlled outputs for sensors.

  - One or two DC_DC_CNTL pins to turn off external power during Standby mode.

- Embedded RTC (Real Time Clock) can run directly from battery.
- Power supply monitoring capability.
- Low-power mode operations
  - Standby, Sleep, and Deep Sleep
- FCC/IC/ETSI/TELEC/WiFi Certification

Chapter 2 GS2200M Architecture

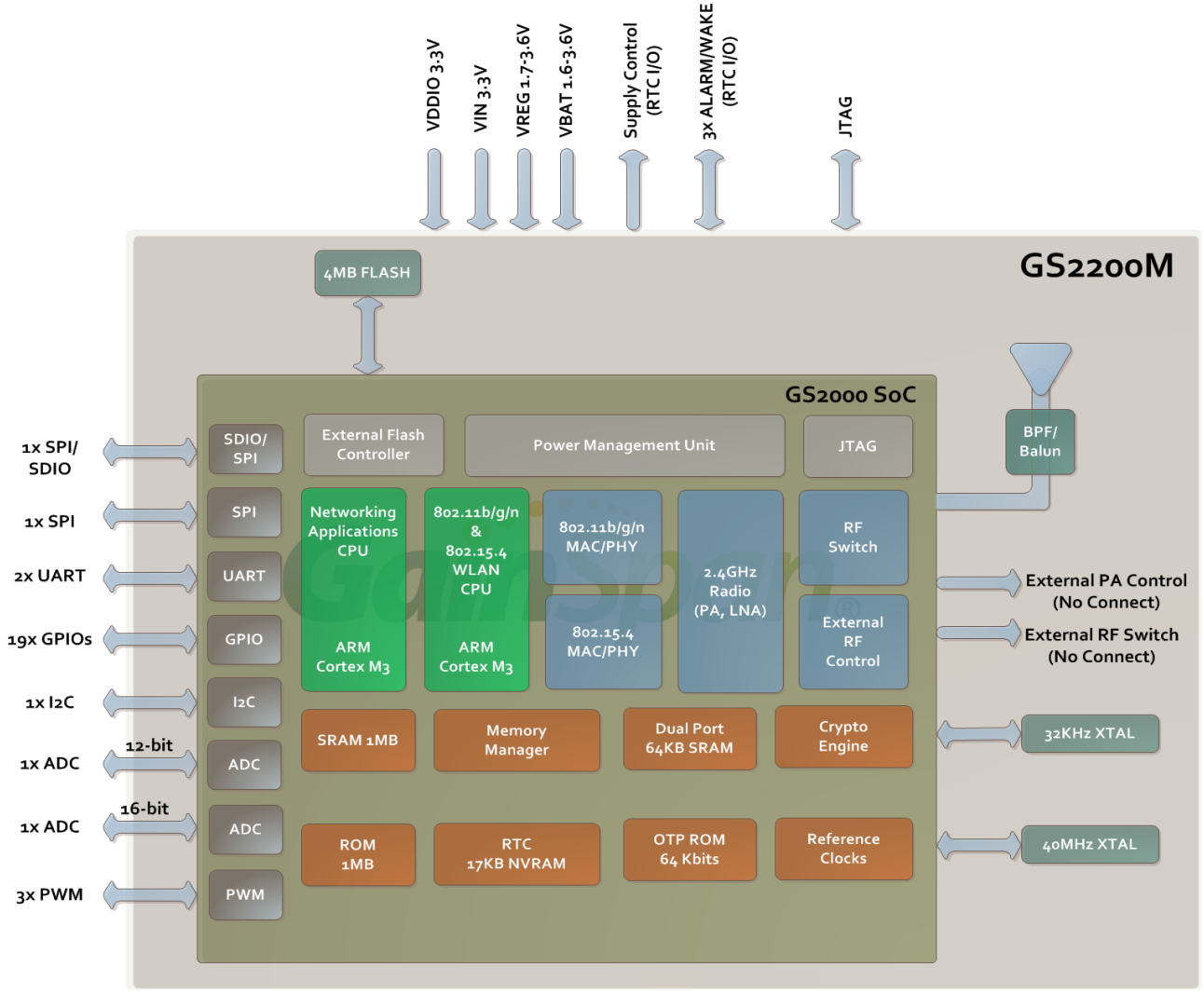
This chapter describes the GainSpan® GS2200M Low Power module architecture.

2.1 Architecture Description

The GainSpan GS2200M module (see Figure 1, page 18) is based on a highly integrated GS2000 ultra low power WiFi System-on-Chip (SoC) that contains the following:

- The GS2000 SoC contains two ARM Cortex M3 CPUs, a compatible 802.11 radio, security, on-chip memory, and variety of peripherals in a single package.
  - One ARM core is dedicated to Networking Subsystems, and the other dedicated to Wireless LAN Subsystems.
  - The module carries an 802.11/g/n radio with on board 32KHz & 40 MHz crystal circuitries, RF, and on-board antenna or external antenna options.
- On module 4 Mega Byte FLASH device that contains the user embedded applications and data such as web pages.
- Variety of interfaces are available such as two UART blocks using only two data lines per port with optional hardware flow controls, two SPI blocks (one SDIO is shared function with one for the SPI interfaces), I^2C with Master or slave operation, JTAG port, low-power 12-bit ADC capable of running at up to 2M samples/sec., GPIO's, and LED Drivers/GPIO with 16mA capabilities.
- GS2200M has a VRTC pin that is generally connected to always available power source such as battery or line power. This provides power to the Real Time Clock (RTC) block on the SoC. The module can be used with an external 1.8V switching regulator that is turned on/off when going into the lowest power mode, i.e., standby mode. The module also has VDDIO power supply input to provide the logic signal level for the I/O pins. VDDIO must turn on/off with the VIN_3V3 power, and must be either 'always ON' or be controlled by the DC_DC_CNTL pin.

Figure 1 GS2200M Block Diagram



2.2 Wireless LAN and System Control Subsystem

The WLAN CPU subsystem consists of the WLAN CPU, its ROM, RAM, 802.11b/g/n MAC/PHY, and peripherals. This CPU is intended primarily to implement the 802.11 MAC protocols. The CPU system has GPIO, Timer, and Watchdog for general use. A UART is provided as a debug interface. A SPI interface is provided for specific application needs. The WLAN CPU can access the RTC registers through an asynchronous AHB bridge. WLAN CPU has only Flash read access to the on-board flash memory. The WLAN subsystem interacts with the APP subsystem through a set of mailboxes and shared dual–port memories.

The CPUs provide debug access through a JTAG/serial port. For the GS2200M module, the complete JTAG port is brought out for both CPUs. The CPUs also include code and data trace and watch point logic to assist in-system debugging of SW.

The WLAN subsystem includes an integrated power amplifier, and provides management capabilities for an optional external power amplifier. In addition, it contains hardware support for AES-CCMP encryption (for WPA2) and RC4 encryption (for WEP & WPA TKIP) encryption/decryption.

2.2.1 Onboard Antenna / RF Port / Radio

The GS2200M modules have fully integrated RF frequency synthesizer, reference clock, and PA. Both TX and RX chain in the module incorporate internal power control loops. The GS2200M module also incorporate an on board antenna.

2.2.1.1 802.11 MAC

The 802.11 MAC implements all time critical functionality of the 802.11b/g/n protocols. It works in conjunction with the MAC SW running on the CPU to implement the complete MAC functionality. It interfaces with the PHY to initiate transmit/receive and CCA. The PHY registers are programmed indirectly through the MAC block. The MAC interfaces to the system bus and uses DMA to fetch transmit packet data and save receive packet data. The MAC SW exchanges packet data with the HW though packet descriptors and pointers.

Key Features

- Compliant to IEEE 802.11 (2012)
- Compliant to IEEE 802.11b/g/n (11n – 2009)
- Long and short preamble generation on frame-by-frame basis for 11b frames
- Transmit rate adaptation
- Transmit power control
- Frame aggregation (AMPDU, AMSDU)
- Block ACK (Immediate, Compressed)
- RTS/CTS, CTS-to-self frame sequences and SIFS

- Client and AP modes support
- Encryption support including: AES-CCMP, legacy WPA-TKIP, legacy WEP ciphers and key management
- WiFi Protected Setup 2.0 (WPS2.0) including both PIN and push button options
- 802.11e based QoS (including WMM, WMM-PS)
- WiFi Direct with concurrent mode, including Device/Service Discovery, Group Formation/Invitation, Client Power Save, WPS-PIN/Push Button

2.2.1.2 802.11 PHY

The 802.11 PHY implements all the standard required functionality and GainSpan specific functionality for 802.11b/g/n protocols. It also implements the Radar detection functionality to support 802.11h. The PHY implements the complete baseband Tx and Rx pipeline. It interfaces with the MAC to perform transmit and receive operations. It interfaces directly to the ADC and DAC. The PHY implements the Transmit power control, receive Automatic Gain Control and other RF control signals to enable transmit and receive. The PHY also computes the CCA for MAC use.

Key Features

- Compliant to 2.4GHz IEEE 802.11b/g/n (11n – 2009)
- Support 802.11g/n OFDM with BPSK, QPSK, 16-QAM and 64-QAM; 802.11b with BPSK, QPSK and CCK
- Support for following data rates:
  - 802.11n (20MHz): MCS0 - 7; 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65.0, 72.2 Mbps
  - 802.11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps
  - 802.11b: 1, 2, 5.5, 11 Mbps
- Support Full (800ns) & Half (400ns) Guard Interval (GI) modes (SGI and LGI)
- Support Space time block coding (STBC) for receive direction
- Complete front-end radio integration including PA, LNA and RF Switch

2.2.1.3 RF/Analog

The RF/Analog is a single RF transceiver for IEEE 802.11b/g/n (WLAN). The RF Interface block provides the access to the RF and analog control and status to the CPU. This block is accessible only from the WLAN CPU. It implements registers to write static control words. It provides read only register interface to read static status. It generates the dynamic control signals required for TX and RX based on the PHY signals. The AGC look up table to map the gain to RF gain control word is implemented in this block.

2.2.2 Network Services Subsystem

2.2.2.1 APP CPU

The Network services subsystem consists of an APP CPU which is based on an ARM CORTEX M3 core. It incorporates an AHB interface and a JTAG debug interface. The network RTOS, network stack, and customer application code run on this CPU.

2.2.2.2 Crypto Engine

The Network services subsystem contains a separate hardware crypto engine that provides a flexible framework for accelerating the cryptographic functions for packet processing protocols. The crypto engine has the raw generic interface for cipher and hash/MAC functions such as AES, DES, SHA, and RC4. It also includes two optional engines to provide further offload; the PKA and RNG modules. These provide additional methods for public key acceleration functions and random number generation. The engine includes a DMA engine that allows the engine to perform cryptographic operation on data packets in the system memory without any CPU intervention.

2.2.3 Memory Subsystem

The GS2200M module contains several memory blocks.

2.2.3.1 SRAM

The system memory is built with single port and dual port memories. Most of the memory consists of single port memory. A 64KB dual port memory is used for exchange of data between the two CPU domains. All the memories are connected to the system bus matrix in each CPU subsystem. All masters can access any of the memory within the subsystem.

The APP subsystem has 384KB of dedicated SRAM for program and data use.

The WLAN subsystem has 320KB of dedicated SRAM for program and data use.

These memories are divided into banks of 64KB each. The bank structure allows different masters to access different banks simultaneously through the bus matrix without incurring any stall. Code from the external Flash is loaded into the SRAM for execution by each CPU.

In addition, a static shared SRAM is provided. This consists of five 64KB memory blocks.

At any time, any of these memory blocks can be assigned to one of the CPU subsystem. These should be set up by the APP CPU SW at initialization time. The assignment is not intended to change during operation and there is no HW interlock to avoid switching in the middle of a memory transaction. The assignment to the WLAN CPU should be done starting from the highest block number going down to lowest block number. This result in the shared memory appearing as a single bank for each CPU subsystem, independent of the number of blocks assigned. The shared memory is mapped such that the SRAM space is continuous from the dedicated SRAM to shared SRAM.

A 64KB dual port memory is used for exchange of data between the two CPU domains. Each CPU subsystem can read or write to this memory using an independent memory port. SW must manage the memory access to avoid simultaneous write to the same memory location. The dual port memory appears as a single bank to each CPU subsystem.

2.2.3.2 ROM

ROM is provided in each CPU subsystem to provide the boot code and other functional code that are not expected to change regularly. Each CPU has 512KB of ROM.

2.2.3.3 OTP ROM

The GS2000 device includes a 64Kbit OTP ROM used for storing MAC ID and other information such as security keys etc. The APP and WLAN subsystem each contain 32Kbits (4Kbytes) of OTP memory.

2.2.3.4 Flash Interface

The GS2000 SoC has only internal ROM and RAM for code storage. There is no embedded Flash memory on the SoC. Any ROM patch code and new application code must reside in the on-module Flash device of the GS2200M module. Flash access from the two CPUs are independent. The APP CPU is considered the system Master and the code running on this CPU is required to initialize the overall chip and common interfaces. WLAN CPU access to the Flash is restricted to read DMA. Any write to the Flash from the WLAN CPU must be done through the APP CPU. The operational parameters of the DMA accesses are set by the APP CPU at system startup. The Flash code is transferred to internal RAM before execution.

2.2.4 Clocks

The GS2200M includes four basic clock sources:

- Low power 32KHz clock (see 2.2.5 Real Time Clock (RTC) Overview, page 23)
- 40MHz Xtal Oscillator
- PLL to generate the internal 120MHz (CPU) and 80MHz (PHY) clocks from the 40MHz Xtal.
- High speed RC oscillator 80MHz

Intermediate modes of operation, in which high speed clocks are active but some modules are inactive, are obtained by gating the clock signal to different subsystems. The clock control blocks within the device are responsible for generation, selection and gating of the clocked used in the module to reduce power consumption in various power states.

2.2.5 Real Time Clock (RTC) Overview

To provide global time (and date) to the system, the GS2200M module is equipped with a low-power Real Time Clock (RTC). The RTC is the always on block that manages the Standby state. This block is powered from a supply pin (VRTC) separate from the digital core and may be powered directly from a battery. The RTC implementation supports a voltage range of 1.6V to 3.6V.

2.2.5.1 RTC Main Features

- One 48-bit primary RTC counter as the primary reference for all timing events and standby awake management
- 3 programmable I/O pins with specific default behavior. These pins are in the RTC_IO domain.
  - Two (DC_DC_CNTL and DC_DC_CNTL_n) are setup as output pins to control external regulator
    - After first boot, one can be programmed as RTC_IO_4, similar to RTC_IO_2 below
  - One other (RTC_IO_2) which can be programmed to be either
    - Wakeup counter to generate periodic output (32-bit)
    - Alarm input to wake up the GS2200M module from its sleep states (deep-sleep/standby)
- Startup control counters with HW and SW override registers
- Power-on-reset control with brown-out detector
- RTC registers to hold RTC and wakeup control bits while the core domain is off
- 1Kbyte latch based memory (1.6-3.6V capable)
- 16KB of SRAM memory, divided into 4 equal blocks (1.2V capable)
- uLDO to supply the SRAM memory
- RTC logic is 1.6-3.6v capable
- 32 KHz RC oscillator
- 32768Hz crystal oscillator
- APB interface for CPU access
- Interrupts to CPU

An overview of RTC block diagram is shown in Figure 2, page 24. The RTC contains a low-power 32.768KHz RC oscillator which provides fast startup at first application of RTC power. It also supports an optional 32.768KHz crystal oscillator which can be substituted for the RC oscillator under software control. In normal operation the RTC is always powered up, even in the Power up state.

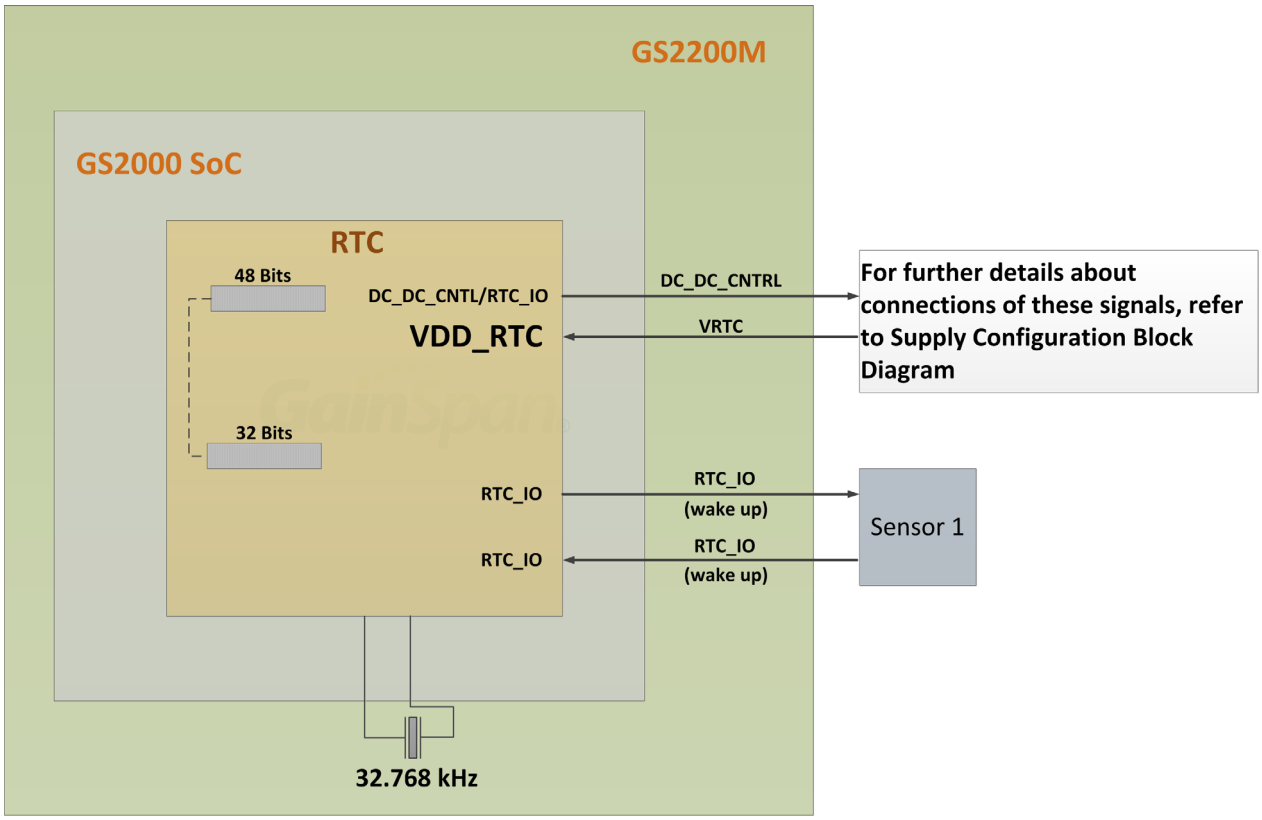
The DC_DC_CNTL programmable counter is 48-bits and provides up to 272 years worth of standby duration.

For the other RTC_IO pins, the programmable embedded counters (32-bit) are provided to enable periodic wake-up of the remainder of the external system, and provide a 1.5 days max period. The RTC_IO pins can be configured as inputs (ALARMS) or output (WAKE UP) pins.

The RTC includes a Power-On Reset (POR) circuit, to eliminate the need for an external component. The RTC contains low-leakage non-volatile (battery-powered) RAM, to enable storage of data that needs to be preserved. It also includes a brown-out detector that can be disabled by SW.

Total current consumption of the RTC is typically less than 5 µA with 1Kbyte of data storage, using the 32.768 kHz oscillator.

Figure 2 RTC Interface Diagram



2.2.5.2 Real Time Clock Counter

The Real Time Counter features:

- 48-bit length (with absolute duration of 272 years).
- Low-power design.

This counter is automatically reset by power-on-reset.

This counter wraps around (returns to “all-0” once it has reached the highest possible “all-1” value).

2.2.5.3 RTC I/O

There is one RTC_IO_2 pin that can be used to control external devices, such as sensors or wake up the module based on external events or devices.

2.2.5.4 DC_DC_CNTL

There are two polarities of the DC_DC_CNTL pin available. If one polarity is unused, it can become a second RTC_IO pin. During RTC Power-on-Reset (e.g., when the battery is first connected), the DC_DC_CNTL pin is held low; it goes high to indicate completion of RTC power-on-reset. This pin can be used as an enable into an external device such as voltage regulator. The DC_DC_CNTL also is held low when module is in standby and goes high to indicate wake up from standby.

2.2.6 GS2200M Peripherals

2.2.6.1 SDIO Interface

The SDIO interface is a full / high speed SDIO device (slave). The device supports SPI, 1-bit SD and 4-bit SD bus mode. The SDIO block has an AHB interface, which allows the CPU to configure the operational registers residing inside the AHB Slave core. The CIS and CSA area is located inside the internal memory of CPU subsystem. The SDIO Registers (CCCR and FBR) are programmed by both the SD Host (through the SD Bus) and CPU (through the AHB bus) via Operational registers. The SDIO block implements the AHB master to initiate transfers to and from the system memory autonomously.

During the normal initialization and interrogation of the card by the SD Host, the card will identify itself as an SDIO device. The SD Host software will obtain the card information in a tuple (linked list) format and determine if that card’s I/O function(s) are acceptable to activate. If the Card is acceptable, it will be allowed to power up fully and start the I/O function(s) built into it.

The SDIO interface implements Function 1 in addition to the default Function 0. All application data transfers are done through the Function 1.

The primary features of this interface are:

- Meets SDIO card specification version 2.0

- Conforms to AHB specification
- Host clock rate variable between 0 and 40 MHz

NOTE: *Tested with current test platform up to 33 MHz.*

- All SD bus modes supported including SPI, 1 and 4 bit SD
- Allows card to interrupt host in SPI, 1 and 4 bit SD modes
- Read and Writes using 4 parallel data lines
- Cyclic Redundancy Check CRC7 for command and CRC16 for data integrity-CRC checking optional in SPI mode
- Programmable through a standard AHB Slave interface
- Writing of the I/O reset bit in CCCR register generates an active low reset output synchronized to AHB Clock domain
- Card responds to Direct read/write (IO52) and Extended read/write (IO53) transactions
- Supports Read wait Control operation
- Supports Suspend/Resume operation

2.2.6.2 SPI Interface

The SPI interface is a master slave interface that enables synchronous serial communications with slave or master peripherals having one of the following: Motorola SPI-compatible interface, TI synchronous serial interface or National Semiconductor Microwire interface. In both master and slave configuration, the block performs parallel-to-serial conversion on data written to an internal 16-bit wide, 8-deep transmit FIFO and serial to parallel conversion on received data, buffering it in a similar 16-wide, 8 deep FIFO. It can generate interrupts to the CPU to request servicing transmit and receive FIFOs and indicate FIFO status and overrun/underrun. The clock bit rate is SW programmable. In master mode, the SPI block in GS2000 can perform up to 30 MHz and in slave mode up to 10 MHz serial clock. Clock rates higher than 20MHz in master mode or 6.66MHz in slave mode requires activation of the PLL's 120MHz clock source. The interface type, data size and interrupt masks are programmable. It supports DMA working in conjunction with the uDMA engine.

2.2.6.3 UART Interface

The UART interface implements the standard UART protocol. It is 16450/16550 compatible. It has separate 32 deep transmit and receive FIFOs to reduce CPU interrupts. The interface supports standard asynchronous communication protocol using start, stop and parity bits. These are added and removed automatically by the interface logic. The data size, parity and number of stop bits are programmable. It supports HW based flow control through CTS/RTS signaling. A fractional baud rate generator allows accurate setting of the

communication baud rate. It supports DMA working in conjunction with the uDMA engine.

2.2.6.4 I2C Interface

The I^2C interface block implements the standard based two wire serial I^2C protocol. The interface can support both master and slave modes. It supports multiple masters, high speed transfer (up to 3.4MHz), 7 or 10-bit slave addressing scheme, random and current address transfer. It also supports clock stretching to interface with slower devices. It can generate interrupts to the CPU to indicate specific events such as FIFO full/empty, block complete, no ack error, and arbitration failure.

2.2.6.5 GPIO

The GPIO block provides programmable inputs and outputs that can be controlled from the CPU SW through an APB interface. Any number of inputs can be configured as an interrupt source. The interrupts can be generated based on the level or the transition of a pin. At reset, all GPIO lines defaults to inputs. Each pin can be configured as input or output from SW control.

2.2.6.6 ADC_SAR_0

The ADC is a 12-bit, low-power, A-to-D converter capable of running at up to 2 Mbps. The ADC is accessible from the APP CPU only. The ADC contains an internal band-gap reference which provides a stable 1.4V reference voltage. Alternatively, the ADC can be programmed to use the VIN_3V3 external supply reference as the full-scale reference. The ADC uses an input clock range of 10KHz to 2MHz. The input clock is generated by an internal NCO (Number Controlled Oscillator). A conversion requires 1 clock cycles. The ADC supports three measurement modes, continuous, single or periodic.

The sample data will be stored in a CPU readable FIFO. The file is an 8-deep FIFO. The FIFO has SW configurable level interrupt. New samples are dropped if FIFO is full and new data is received prior to FW servicing the FIFO, then the sample is dropped.

2.2.6.7 Sigma Delta ADC

The ADC and DAC are 16-bit sigma-delta converters. There is 1 ADC channel. Having a differential pair for a total of two input pins. The sample rate can be 32KHz to 80KHz. The sigma delta converter ratio is 250. The ADC is a 1 channel converter. The channel can have an optional pre-amplifier stage. The gain can be set to 0db, 6db, 12db, 18db, or 24db. The delay of the channel of the ADC can be adjusted under SW control. The digital interface for the ADC and the DAC are 2's complement. ADC channel 0 can alternatively be used as a differential DAC.

2.2.6.8 PWM

The PWM consists of three identical PWM function blocks. The PWM function blocks can be used in two modes of operations:

- Independent PWM function blocks providing output signal with programmable frequency and duty cycle
- Synchronized PWM function blocks with programmable phase delay between each PWM output

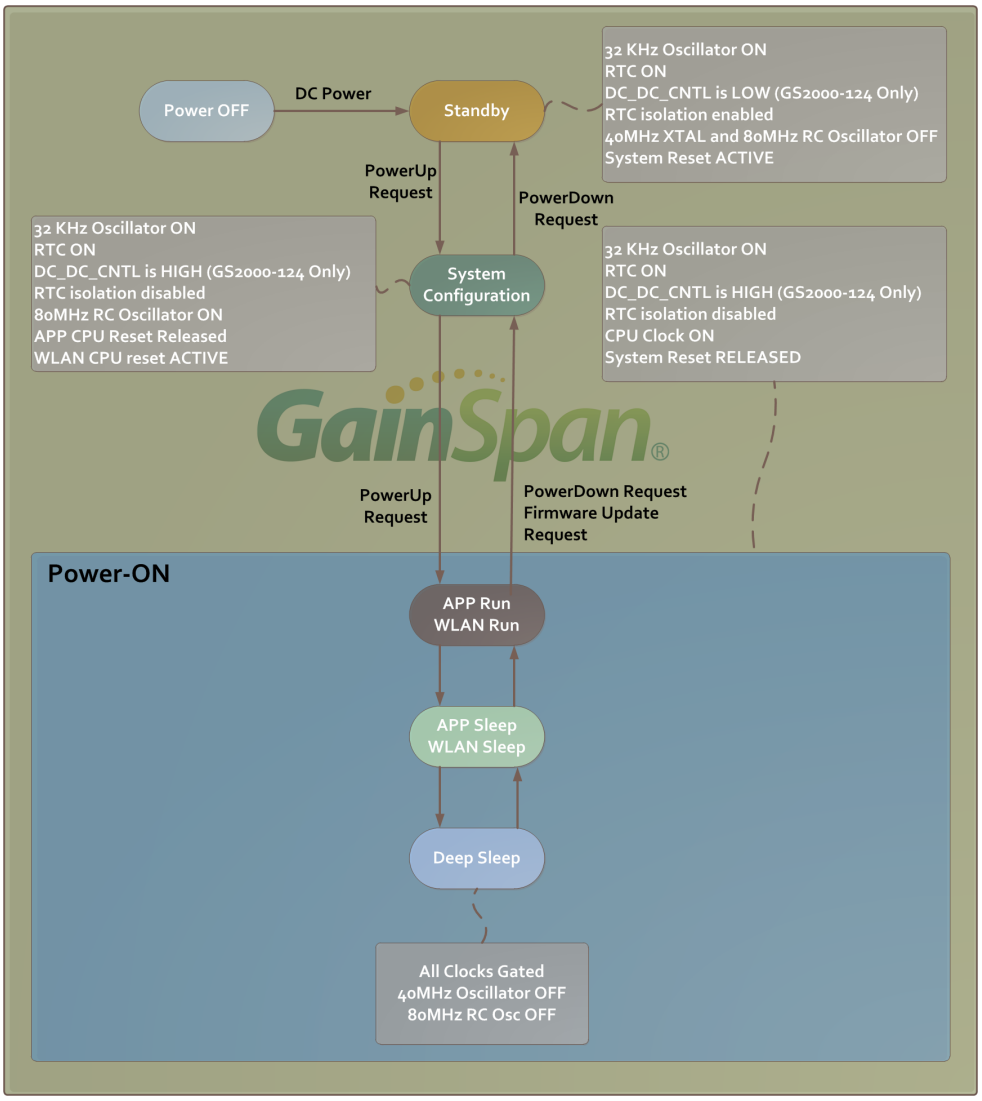
The PWM has the following features:

- 32-bit AMBA APB interface to access control, and status information
- Three identical PWM function blocks
- Each PWM block can be enabled independently
- All three PWM blocks can be started synchronously or chained with programmable delay
- Programmable 6-bit prescaler for the input clock (see 2.2.4 Clocks, page 22)
- Programmable frequency and duty cycle using 16 bit resolution in terms of clock cycles for ON and OFF interval time
- Combined interrupt line with independent masking of interrupts

2.2.7 System States

Figure 3, page 29 shows the power management/clock states of the GS2200M system.

Figure 3 GS2200M System States



The system states of the GS2200M system are as follows:

Power OFF: No power source connected to the system.

Standby: In the standby state, only the RTC portion of the GS2200M is powered from the VRTC pin. The other power supplies are turned off by the DC_DC_CNTL pin being low. To achieve the lowest standby current, other supply pins should be powered on/off together, controlled by the DC_DC_CNTL pin, including the VREG pin, VDDIO, and the VIN_3V3 pin.

In standby state, the 32.768KHz oscillator keeps running and only the RTC RAM retains the state (how many banks retain their state is SW configurable). SRAM, CPUs and I/Os are all in OFF state, as there is no VREG and no VDDIO being supplied to the GS2200M device.

This is the lowest-power-consumption state. In a typical application, the system returns to the Standby state between periods of activity, to keep the average power very low and enable years of operation using conventional batteries. During standby, the RTC isolates itself from the rest of the chip, since the signals from the rest of the chip are invalid. This prevents corruption of the RTC registers.

Exit from standby occurs when a pre-specified wakeup time occurs, or when one of the RTC_IO's configured as alarm inputs sees the programmed polarity of signal edge. When one of the wakeup conditions occurs, the RTC asserts reset to the chip and sets the DC_DC_CNTL pin high to enable power to the rest of the module. After power to the rest of the module is assumed to be good, the isolation between the RTC and the rest of the chip is released, and reset to the core logic is released. The system now starts booting.

NOTE: *During first battery plug, i.e., when power is applied the first time to the RTC power rail (VRTC), the power detection circuit in the RTC also causes a wakeup request.*

System Configuration: When a power-up is requested, the system transitions from the Standby state to the System Configuration state. In this state, the APP CPU is released from reset by the RTC. The WLAN CPU remains in the reset state during System Configuration. The APP CPU then executes the required system configurations, releases the WLAN CPU from reset, and transitions to the Power-ON state.

The System Configuration state is also entered on transition from the Power-ON state to the Standby state, to complete necessary preparations before shutting off the power to the core system.

Power-ON: This is the active state where all system components can be running. The Power-ON state has various sub-states, in which unused parts of the system can be in sleep mode, reducing power consumption. Sleep states are implemented by gating the clock signal off for a specific system component. Additionally, unneeded clock sources can be turned off. For example, receiving data over a slave SPI interface could be done with only the 80MHz RC oscillator active, and the 40MHz crystal and PLL turned off.

Sleep: In the Sleep state, the 40MHz crystal and the 80MHz RC oscillator remains running, but it is gated off to one or both CPUs. Each CPU can independently control its own entry into Sleep state. Any enabled interrupt will cause the interrupted CPU to exit from Sleep state, and this will occur within a few clock cycles.

Deep Sleep: Deep sleep is entered only when both CPUs agree that the wakeup latency is OK. In Deep Sleep mode, the 40MHz crystal oscillator and 80MHz RC oscillator are turned off to save power, but all power supplies remain turned on. Thus all registers, memory, and I/O pins retain their state. Any enabled interrupt will cause an exit from Deep Sleep state.

NOTE: *For the above power states, software controls which clocks stay turned on in each of the three states.*

The following are not system states, but are related design notes:

Power Control: The GS2200M was designed with the intent that power to the non-RTC portions of the chip be controlled from the DC_DC_CNTL signal. In applications where it is preferred that an external host control the power, this is OK if ALL power, including VRTC power, is turned on and off by the external host. In this case, all state is lost when power goes off, and the latencies from first battery plug apply.

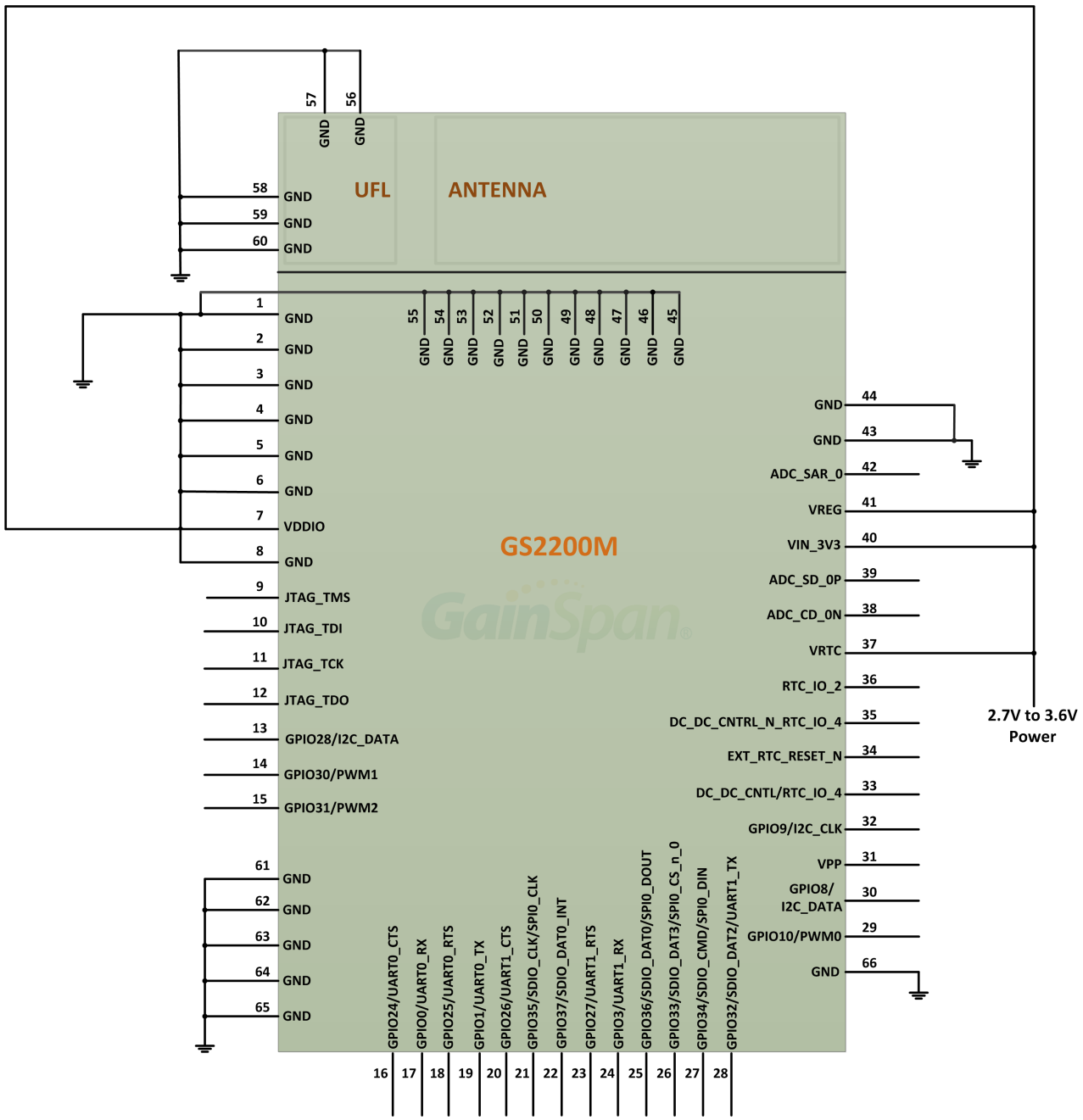
If these latencies are not acceptable, then the GS2200M MUST control power. The external host would use an alarm to wake it up, and a serial command to put it into standby. The DC_DC_CNTL pin would control the power supplies. It is NOT reliable for the external host to directly control the power supplies if VRTC is to be left turned on. This is because the RTC would not know when to isolate itself from the rest of the chip, and might get corrupted during power up or power down.

EXT_RTC_RESET_n pin: This is an input pin for resetting the entire module, including the RTC section of the device. It may be left floating, since there is a weak internal pull-up resistor. But if it is connected, then GainSpan recommends an external 5.1K pull-up resistor to VRTC.

2.2.8 Power Supply

This section shows various application power supply connections. Figure 4, page 32 shows the GS2200M always on power supply connection, Figure 5, page 33 shows the GS2200M in regulator powered with optimized standby mode only, Figure 6, page 34 shows GS2200M in regulator powered with optimized standby and radio power mode, and Figure 7, page 35 shows the GS2200M in battery powered with optimized standby mode.

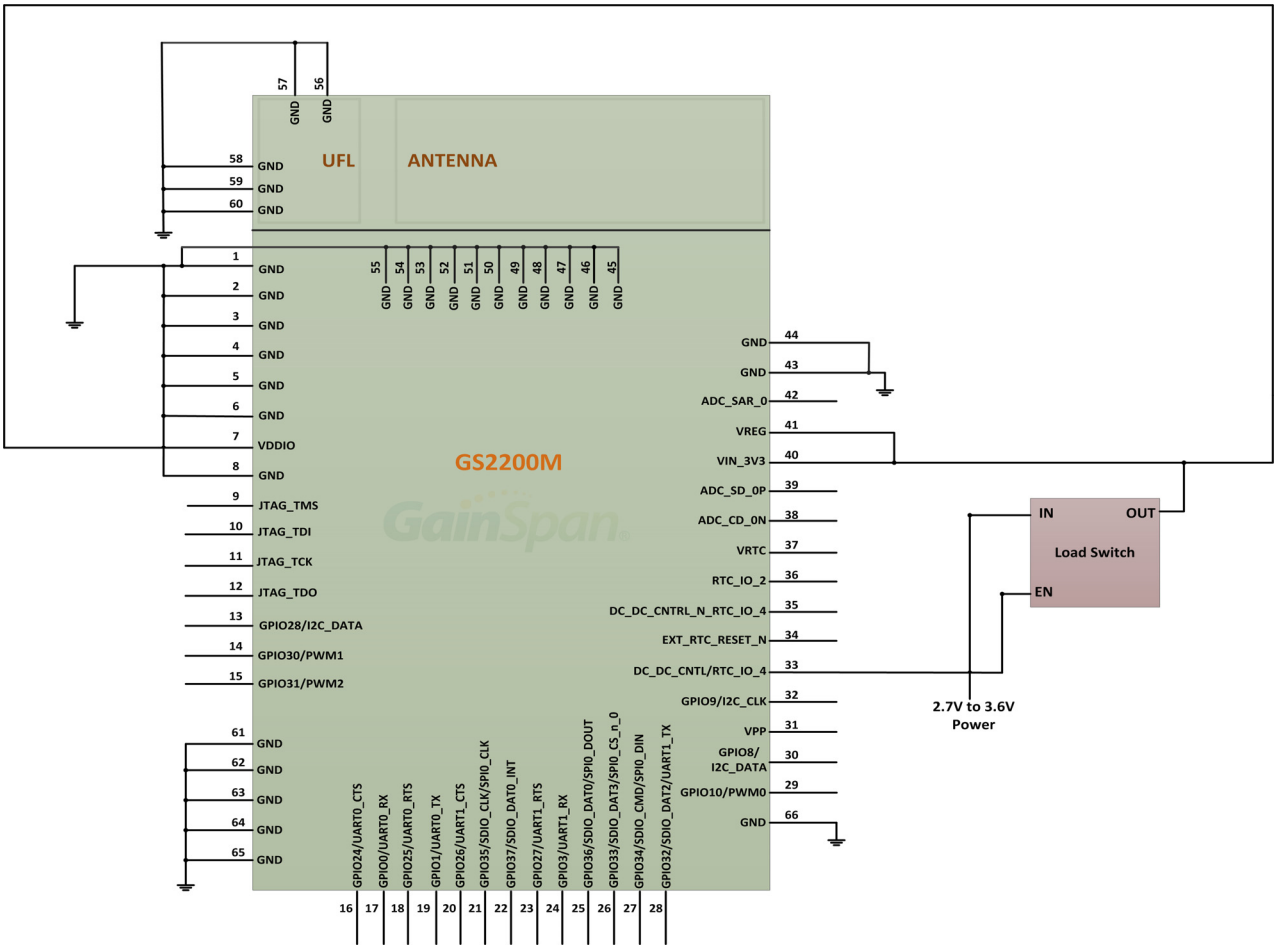
Figure 4 GS2200M Always ON Power Supply Connection



Notes:

1. With this connection method, standby current will not be optimized.

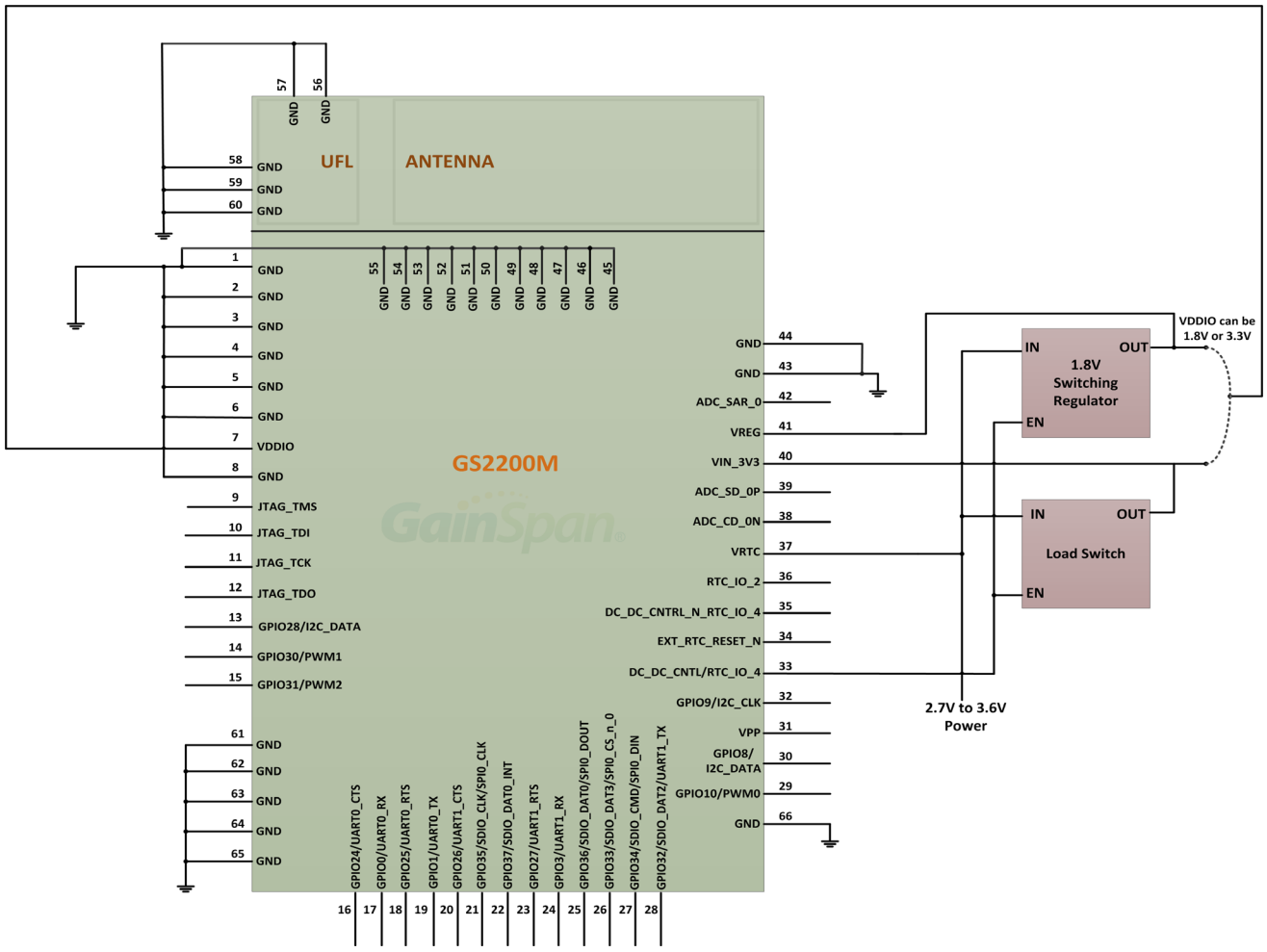
Figure 5 GS2200M Regulator Powered with Optimized Standby Only



Notes:

1. This connection applies for designs starting from regulated power, using GS2200M module and want optimized standby (lowest current consumption) state of the module. In this connection it is important to note the following:
2. Input voltage to VRTC must always be ON to keep the RTC powered so that the 32KHz crystal is running.
3. VDDIO, VREG, and VIN_3V3 power should be OFF during this state. Recommendation is to use DC_DC_CNTL to also control the unit supplying the voltage to VDDIO, VREG, and VIN_3V3
4. Select load switch component which has a ‘soft start’ feature. This will help to avoid any glitches to the input power when DC_DC_CNTL goes HIGH.
5. The load switch saves about 45uA in standby mode.

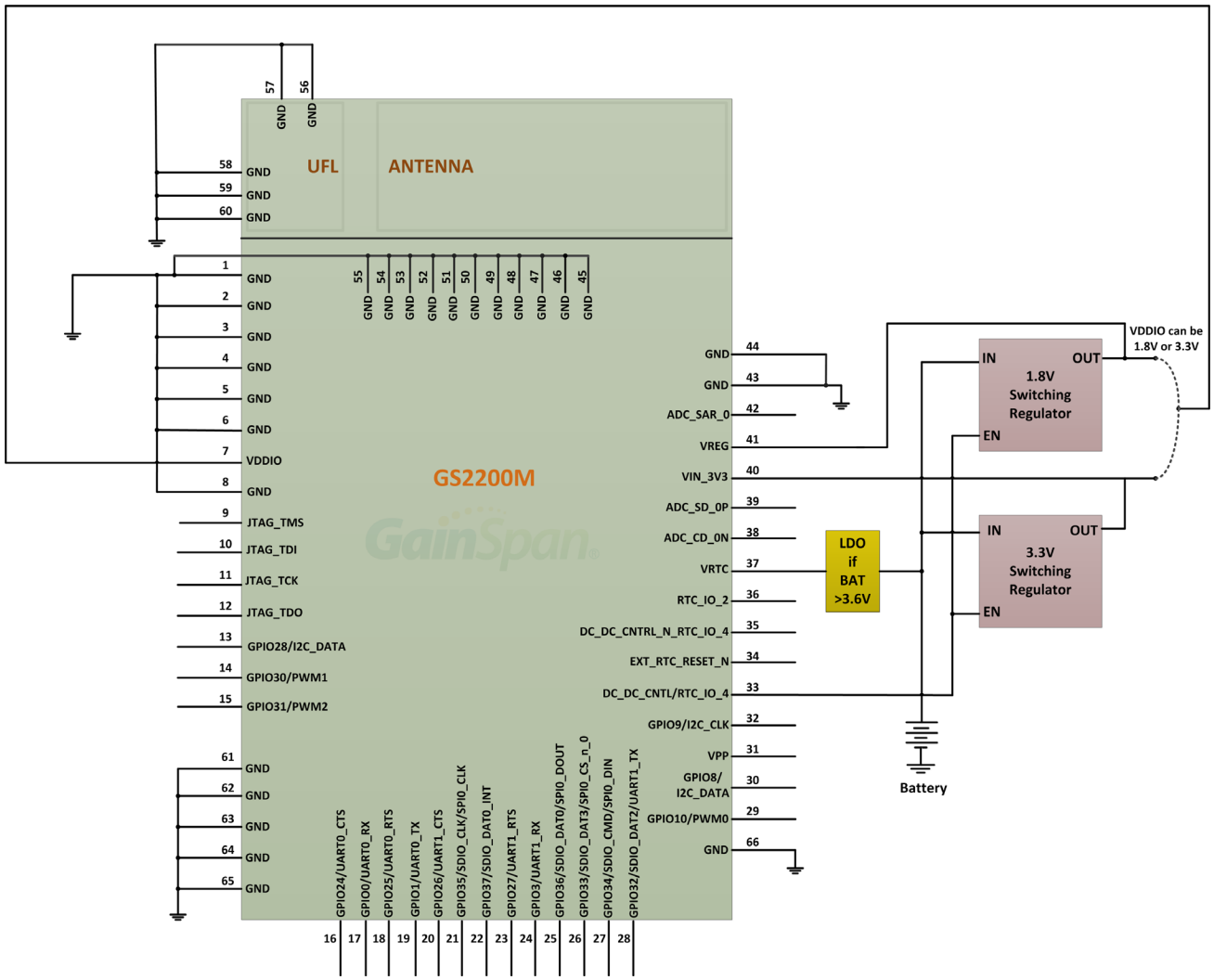
Figure 6 GS2200M Regulator Powered with Optimized Standby and Radio Power



Notes:

1. This connection applies for designs starting from regulated power, using GS2200M module and want optimized standby (lowest current consumption) state of the module. In this connection it is important to note the following:
2. Input voltage to VRTC must always be ON to keep the RTC powered so that the 32KHz crystal is running.
3. VDDIO, VREG, and VIN_3V3 power should be OFF during this state. Recommendation is to use DC_DC_CNTL to also control the unit supplying the voltage to VDDIO, VREG, and VIN_3V3
4. Select load switch and regulator components which have a ‘soft start’ feature. This will help to avoid any glitches to the input power when DC_DC_CNTL goes HIGH.
5. The 1.8V switching regulator saves about 50mA of input power Tx and Rx.

Figure 7 GS2200M Battery Powered with Optimized Standby Support



Notes:

1. This connection applies for designs (typically battery operated) using GS2200M module and want to optimized standby (lowest current consumption) state of the module. In this connection it is important to note the following:
2. Input voltage to VRTC must always be ON to keep the RTC powered so that the 32KHz crystal is running.
3. VDDIO, VREG, and VIN_3V3 power should be OFF during this state. Recommendation is to use DC_DC_CNTL to also control the unit supplying the voltage to VDDIO, VREG, and VIN_3V3
4. If Battery is between 1.6V and 3.6V, then VRTC should connect directly to the battery.

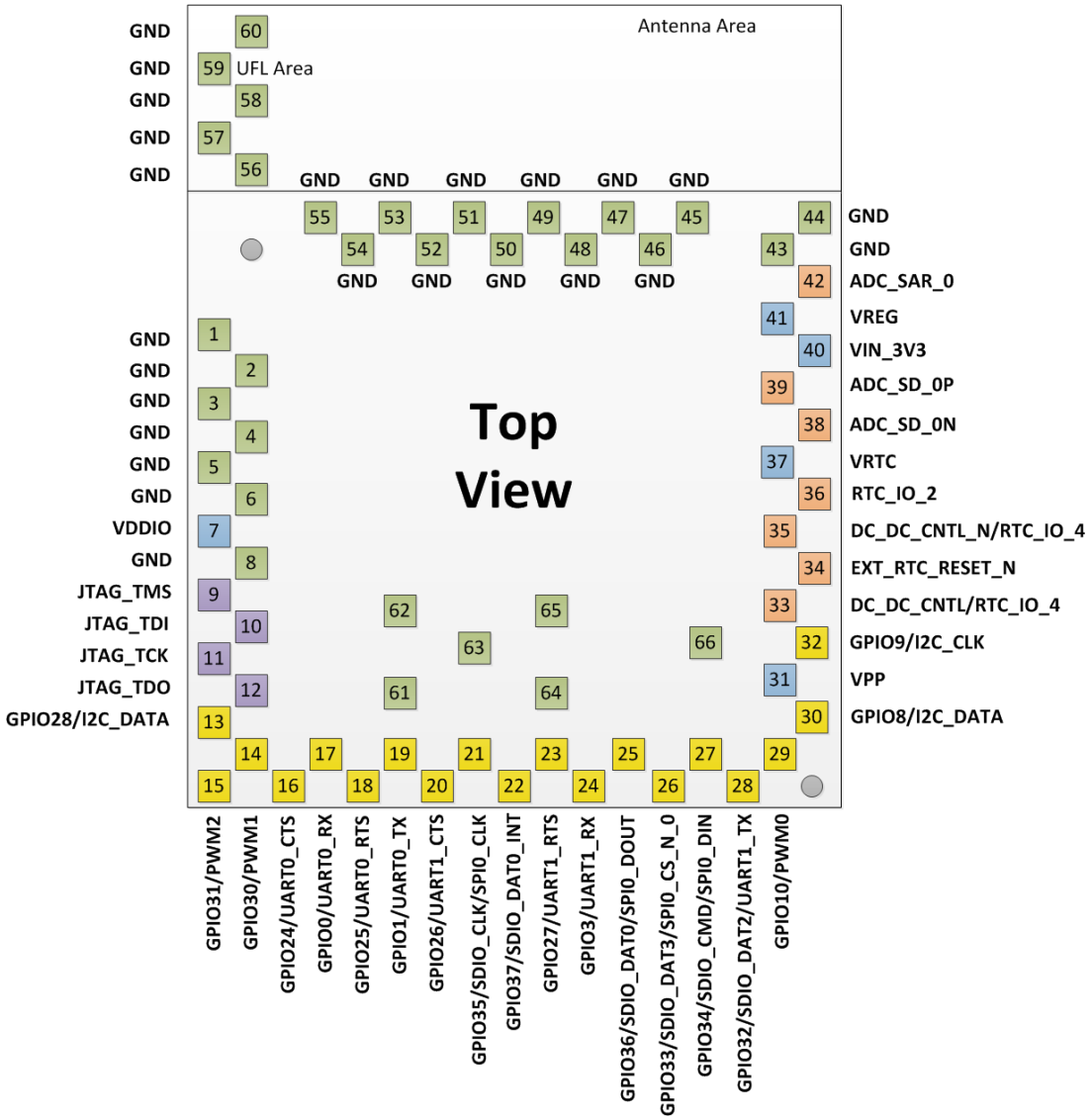
Chapter 3 Pin-out and Signal Description

This chapter describes the GainSpan® GS2200M Low Power module architecture.

3.1 GS2200M Device Pin-out

Figure 8, page 37 shows the GS2200M device pin-out diagram.

Figure 8 GS2200M Device Pin-out Diagram (Module Top View)



3.1.1 GS2200M Module Pins Description

Table 8, page 38 describes the GS2200M module pin signal description.

Table 8 GS2200M Module Pin Signal Description

Pins	Name	Voltage Domain	Internal Bias after Hardware Reset	Drive Strength (mA)	Signal State	Description
1-6	GND	0V	Not Applicable		Analog port	Ground
7	VDDIO	VDDIO	Not Applicable		Analog port	All I/O voltage domain (can be tied to VIN_3V3 or tied to HOST I/O supply)
8	GND	0V	Not Applicable		Analog port	Ground
9	JTAG_TMS	VDDIO	Pull-up (see Note 1)	4	Digital Input	JTAG Test Mode Select
10	JTAG_TDI	VDDIO	Pull-up (see Note 1)	4	Digital Input	JTAG Test Data In
11	JTAG_TCK	VDDIO	Pull-up (see Note 1)	4	Digital Input	JTAG Test Clock
12	JTAG_TDO	VDDIO	Pull-down (see Note1)	4	Digital Output	JTAG Test Data Out
13	GPIO 28/I2C_DATA	VDDIO	Pull-down (see Note 1, Note 4, and Note 5)	12	Digital Input/Output	GPIO/Inter-Integrated Circuit Data
14	GPIO30/PWM1	VDDIO	Pull-down (see Note 1 and Note 8)	16	Digital Input/Output	GPIO/Pulse Width Modulation Output 1
15	GPIO31/PWM2	VDDIO	Pull-down (see Note 1 and Note 8)	16	Digital Input/Output	GPIO/Pulse Width Modulation Output 2
16	GPIO24/UART0_CTS (see Note 7)	VDDIO	Pull-down (see Note 1)	12	Digital Input/Output	GPIO/UART0 Clear to Send input (see Note 7)
17	GPIO0/UART0_RX	VDDIO	Pull-down (see Note 1)	4	Digital Input/Output	GPIO/UART0 Receive Transmission
18	GPIO25/UART0_RTS (see Note 7)	VDDIO	Pull-down (see Note 1)	12	Digital Input/Output	GPIO/UART0 Clear to Send input
19	GPIO1/UART0_TX	VDDIO	Pull-down (see Note 1)	4	Digital Input/Output	GPIO/UART0 Transmission
20	GPIO26/UART1_CTS (see Note 7)	VDDIO	Pull-down (see Note 1)	4	Digital Input/Output	GPIO/UART1 Clear to Send

Table 8 GS2200M Module Pin Signal Description (Continued)

Pins	Name	Voltage Domain	Internal Bias after Hardware Reset	Drive Strength (mA)	Signal State	Description
21	GPIO35/SDIO_CLK_SPI0_CLK	VDDIO	Pull-down	4	Digital Input/Output	GPIO/SDIO Clock/SPI0 Clock Input from the HOST
22	GPIO37/SDIO_DAT1_INT (see Note 10)	VDDIO	Pull-down	4	Digital Input/Output	GPIO/SDIO Data Bit 1/SPI0 Chip Select Input 0 from the HOST (Active Low)
23	GPIO27/UART1_RTS	VDDIO	Pull-down (see Note 1, Note 3, and Note 7)	4	Digital Input/Output	GPIO/UART1 1 Request to Send Output (see Note 7). This pin is used for Program Mode.
24	GPIO3/UART1_RX	VDDIO	Pull-down (see Note 1)	4	Digital Input/Output	GPIO/UART1 Receive Input
25	GPIO36/SDIO_DAT0/SPI0_DOUT(see Note E-1)	VDDIO	Pull-down (see Note 1)	4	Digital Input/Output	GPIO/SDIO Data Bit0/SPI0 Transmit Data Output to the HOST
26	GPIO33/ SDIO_DAT3/ SPI0_CS_N_0	VDDIO	Pull-up (see Note 1)	4	Digital Input Output	GPIO/SDIO Data Bit 3/SPI0 Chip Select Input 0 from the HOST (Active Low)
27	GPIO34/ SDIO_CMD/ SPI0_DIN	VDDIO	Pull-down (see Note 1)	4	Digital Input/Output	GPIO/SDIO Command Input/SPI0 Receive Data Input from HOST
28	GPIO32/ SDIO_DAT2/ UART1_TX	VDDIO	Pull-down (see Note 1)	4	Digital Input/Output	GPIO/SDIO_DATA Bit 2/UART 1 Transmitter Output
29	GPIO10/PWM0	VDDIO	Pull-down (see Note 1)	4	Digital Input/Output	GPIO/PWM0
30	GPIO8/I2C_DATA	VDDIO	Pull-down (see Note 1 and Note 5)	12	Digital Input/Output	GPIO/Inter-Integrated Circuit Data
31	VPP (see Note 9)	VPP	Not Applicable		Analog port	Programming Voltage for OTP Memory
32	GPIO9/I2C_CLK	VDDIO	Pull-down (see Note 1 and Note 5)	12	Digital Input/Output	GPIO/Inter-Integrated Circuit Clock

Table 8 GS2200M Module Pin Signal Description (Continued)

Pins	Name	Voltage Domain	Internal Bias after Hardware Reset	Drive Strength (mA)	Signal State	Description
33	DC_DC_CNTRL/RTC_IO_4	VRTC	Output High	1	RTC Digital Input/Output	VIN_3V3 Regulator Control Output/RTC Digital Input/Output
34	EXT_RTC_RESET_N (see Note 6)	VRTC	Pull-up		Digital Input	Module Hardware Reset Input
35	DC_DC_CNTRL_N/RTC_IO_4	VRTC	Output Low	1	RTC Digital Input/Output	VIN_3V3 Regulator Control Output/RTC Digital Input/Output
36	RTC_IO_2 (see Note 2)	VRTC	Pull-down (see Note 1)	1	RTC Digital Input/Output	Embedded Real Time Clock Input/Output 2
37	VRTC	VRTC	Not Applicable		Analog port	Embedded Real Time Clock Power Supply
38	ADC_SD_0N	VIN_3V3	None (see Note 2)		Analog port	Sigma Delta ADC negative input
39	ADC_SD_0P	VIN_3V3	None		Analog port	Sigma Delta ADC positive input
40	VIN_3V3	VIN_3V3	Not Applicable		Analog port	Single Supply Port
41	VREG		Not Applicable			1.7V to 3.6V input to 1.2V LDO
42	ADC_SAR_0	VIN_3V3	Not Applicable (see Note 2)		Analog Input	General Analog to Digital Converter, Successive Approximation Register 0
43-66	GND	0V	Not Applicable		Analog port	Ground

Notes:

1. Pins with drive strength 4, 12, and 16 have one pull resistor (either up or down, not both), which is enabled at reset. RTC_IO pins have both pull_up and pull_down resisters. The RTC_IO pull down resisters are enabled at reset for non DC_DC_CNTL pins.
2. Can be left as no connect.
3. This pin enables programming of the module. If UART1_RTS (GPIO27) is high during reset or power on then the GS2200M will wait for Flash download via UART0 or SPI0 interface. Route this pin on the base board so it can be pulled up to VDDIO for programming the module.
4. GPIO28 is the primary function; if using GPIO8/9 as I2C function, then this pin cannot be used for I2C function.
5. If I^2C interface is used, provide 2K Ohm pull-ups, to VIN_3V3, for I2C_CLK and I2C_DATA.

6. EXT_RTC_RESET_n is an active low reset input, referenced to the VRTC voltage. It resets the whole module, including the RTC section. It may be left unconnected. If driven externally, GainSpan recommends a 5.1K pull-up resistor to VRTC.
7. RTS is an active LOW output, indicating that the UART FIFO has space to receive data. CTS is an active LOW input, indicating that data can be transmitted.
8. These pins have higher drive strength so they can drive LEDs directly.
9. This pin is generally reserved for GainSpan use, but if a design requires writing to OTP during production, then design must take into account connection to this pin. Otherwise, it should be left as a No Connect.
10. In the Serial-to-WiFi firmware when using SPI interface this pin is the host wake-up signal or the Ready to Send signal.

Errata

E1. The SPI0_DOUT and SPI1_OUT signals do not disable their drive and become Hi-Z when the associated chip select pin is high. This applies to all pin MUX locations for the SPI_DOUT signals. If there are multiple write only devices on the same SPI bus, then this is not an issue. This only becomes an issue when there are other read/write devices on the same SPI bus. The workaround is to add an external buffer chip, such as 74LVC1G125 between the SPI_DOUT pin and the SPI bus, with the enable connected to the chip select signal.

3.1.2 GS2200M Pin MUX Function

The GS2200M pins have multiple functions that can be selected using MUX function by software. Each pin has an independent MUX select register. Table 9, page 42 shows the various MUX functions for each pin. All pins are GPIO inputs at reset. For pins that are inputs to functional blocks only one pin may be assigned to any input function. For example, UART1_RX may be assigned to GPIO3 but not to both GPIO3 and GPIO37.

Table 9 GS2200M Pin MUX Description

Pin#	Pin Name	Mux3	Mux4	Mux5	Mux6	Mux7	Comments
1-6	gnd						Ground
7	vddio						
8	gnd						Ground
9	jtag_tms						
10	jtag_tdi						
11	jtag_tck						
12	jtag_tdo						
13	gpio28/i2c_data	i2c_data	spi1_clk	clk_hs_rc	tracedata(2)	spi1_cs_n_21	
14	gpio30/pwm1	pwm1	spi1_din	uart1_rx	clk_rtc	wuart_rx	
15	gpio31/pwm2	pwm2	spi1_dout[1]	uart1_tx	traceclk	wuart_tx	
16	gpio24/uart0_cts	uart0_cts	wuart_cts	pwm0	tracedata(3)	spi1_cs_n_0	
17	gpio0/uart0_cts	uart0_rx	wuart_rx	pwm2	tracedata(2)	spi1_din	
18	gpio25/uart0_rts	uart0_rts	wuart_rts	spi1_cs_n_7	tracedata[1]	spi1_clk	
19	gpio1/uart0_tx	uart0_tx	wuart_tx	pwm1	tracedata(0)	spi1_dout[1]	
20	gpio26/uart1_cts	uart1_cts	wuart_cts	i2s_din	spi1_cs_n_13	wspi_clk	
21	gpio35/sdio_clk/spi0_clk	sdio_clk	reserved	i2c_clk	traceclk	spi0_clk	Only 4mA for I2C
22	gpio37/sdio_dat1_int	sdio_data1	wuart_rx	uart1_rx	tracedata[3]	spi0_cs_n_10	
23	gpio27/uart1_rts	uart1_rts	wuart_rts	i2s_dout	uart1_tx	wspi_dout	
24	gpio3/uart1_rx	uart1_rx	wuart_rx	i2s_bitclk	spi1_cs_n_14	wspi_din	
25	gpio36/sdio_dat0/spi0_dout[1]	sdio_data0	reserved	i2c_data	reserved	spi0_dout[1]	Only 4mA for I2C
26	gpio33/sdio_dat3/spi0_cs_n_0	sdio_data3	reserved	uart1_rts	tracedata[0]	spi0_cs_n_0	
27	gpio34/sdio_cmd/spi0_din	sdio_cmd	reserved	uart1_cts	tracedata[1]	spi0_din	
28	gpio32/sdio_dat2/uart1_tx	sdio_data1	wuart_tx	uart1_tx	tracedata[2]	spi1_cs_n_12	
29	gpio10/pwm0	pwm0	reserved	reserved	tracedata[0]	clk_rtc	
30	gpio8/i2c_data	i2c_data	uart1_tx	reserved	tracedata[3]	reserved	
31	vpp						Programming voltage for OTP memory
32	gpio9/i2c_clk	i2c_clk	uart1_rx	reserved	tracedata[1]	i2s_lcrclk	
33	dc_dc_cntl/rtc_io_4						

Table 9 GS2200M Pin MUX Description (Continued)

Pin#	Pin Name	Mux3	Mux4	Mux5	Mux6	Mux7	Comments
34	ext_rtc_reset_n						
35	dc_dc_cntl_n/rtc_io_4						
36	rtc_io_2						
37	vrtc						
38	adc_sd_0n						Sigma-delta ADC0 negative input or DAC output
39	adc_sd_0p						Sigma-delta ADC0 positive input or DAC output
40	vin_3v3						Includes Flash, PA, and ADC
41	vreg						1.7V to 3.6V input to 1.2V LDO
42	adc_sar_0						SAR ADC0 input
43-66	gnd						Ground

Note 1. The SPI0_DOUT and SPI1_OUT signals do not disable their drive and become Hi-Z when the associated chip select pin is high. This applies to all pin MUX locations for the SPI_DOUT signals. If there are multiple write only devices on the same SPI bus, then this is not an issue. This only becomes an issue when there are other read/write devices on the same SPI bus. The workaround is to add an external buffer chip, such as 74LVC1G125 between the SPI_DOUT pin and the SPI bus, with the enable connected to the chip select signal.

3.1.3 GS2200M Program and Code Restore Options

Table 10, page 44 describes the options available for device program mode and code restore capabilities. The respective GPIO pins are sampled at reset by device and depending on the values seen on these pins goes into the appropriate mode. Code for the GS2200M resides on the internal flash of the module and up to two back-up copies could be stored in flash. If a software designer wants to restore the execution code to one of the backup copy, it can be accomplished by asserting the appropriate GPIO pins as shown in the table below during power up or reset.

Table 10 GS2100M Pin Program and Code Restore

Boot Control	Program Mode (GPIO 27)	Program Select/Previous Restore (GPIO 25)	Interfaces for Program Load
(see Note 1)	0	0	Normal boot
	0	1	Previous Code Restore. Restores the prior code revision by invalidating the present code image. Will NOT invalidate the last remaining image.
	1	0	Program Mode: UART0 @ 115.2Kbaud; nothing on GPIO15-18; SPI0 on SDIO pins. Note: this is the default you get if you don't pull the Program Select pin high.
	1	1	Program Mode using: UART0 @921.6Kbaud; SPI0 on GPIO15-18. Note: GPIO15-18 are only available on GS2000 SoC, and not on modules.

Note:

1. In Run Mode, boot ROM leaves all GPIO pins as input with pull resistor enabled until flash code sets them otherwise. In Program Mode, only the pins required for the Program Mode specified interfaces are set to non-GPIO mode.

Chapter 4 Electrical Characteristics

This chapter describes the GainSpan® GS2200M electrical characteristics.

4.1 Absolute Maximum Ratings

Conditions beyond those cited in Table 11, page 45 may cause permanent damage to the GS2200M, and must be avoided. Sustained operation, beyond the normal operating conditions, may affect the long term reliability of the module.

Table 11 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Storage Temperature	T_{ST}	-55		+125	^{o}C
RTC Power Supply	VRTC	-0.5		4.0	V
I/O Supply Voltage	VDDIO	-0.5		4.0	V
Single Supply Port	VIN_3V3	0.5		4.0	V
OTP Supply	VPP		TBD		V
Signal Pin Voltage[1]	VI	-0.3		Voltage Domain + 0.3	V
Regulator Input Supply	VREG	-0.5		4.0	V

Note:

1. Reference domain voltage is the Voltage Domain. Refer to the section on GGS2200M Module Pins Description. For limitations on state voltage ranges, refer to the section GS2200M Module Pins Description.

4.2 Operating Conditions

Table 12, page 46 lists the operating conditions of the GS2200M module.

Table 12 Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Extended Temperature Range	T_A	-40		+70	^oC
RTC Power Supply	VRTC	1.6	3.3	3.6	V
Single Supply Port GS2200M	VIN_3V3	2.7	3.3	3.6	V
Signal Pin Voltage[1]	VI	0		Voltage Domain	V
VPP[2]	VPP	5.5	5.75	6.0	V
I/O and LDO Supply Voltage	VDDIO, VREG independently	1.7 2.7	1.8 3.3	1.98 3.6	V

Notes:

1. Reference domain voltage is the Voltage Domain. Refer to section GS2200M Module Pins Description.
2. The VPP pin should be left floating when not doing OTP programming operations.

4.3 I/O DC Specifications

4.3.1 I/O Digital Specifications (Tri-State) Pin Types 4mA, 12mA, and 16mA

The specifications for these I/O's are given for voltage ranges: 2.7V to 3.6V.

4.3.1.1 I/O Digital Specifications for VDDIO=2.7V to 3.6V

Table 13, page 47 lists the parameters for I/O digital specification for VDDIO 2.7V to 3.6V for Pin Types 4mA, 12mA, and 16mA.

Table 13 I/O Digital Parameters for VDDIO=2.7V to 3.6V

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Note
I/O Supply Voltage	V_{DDIO}	2.7	3.3	3.6	V	
Input Low Voltage	V_{IL}	-0.3		$0.3*V_{DDIO}$	V	
Input High Voltage	V_{IH}	$0.7*V_{D\ DIO}$		V_{DDIO}	V	
Input Leakage Current	I_L			10	µA	Pull up/down disabled
Tri-State Output Leakage Current	I_{OZ}			10	µA	Pull up/down disabled
Pull-Up Resistor	R_u	34K	51K	100K	Ω	
Pull-Down Resistor	R_d	35K	51K	100K	Ω	
Output Low Voltage	V_{OL}			0.4	V	
Output High Voltage	V_{OH}	$0.8*V_{DDIO}$			V	
Low Level Output Current @ V_{OL} max	I_{OL}	4 12 16			mA	Pin Type 4mA Pint Type 12mA Pint Type 16mA
High Level Output Current @ V_{OH} min	I_{OH}	4 12 16			mA	Pin Type 4mA Pin Type 12mA Pin Type 16mA
Output rise time 10% to 90% load, 30pF	t_{TRLH}	3.1 1.8 1.5	4.2 2.4 2.0	7 4 3.4	ns	Pin Type 4mA Pint Type 12mA Pin Type 16mA
Output fall time 90% to 10% load, 30pF	t_{TFHL}	3.8 1.8 1.5	5.0 2.5 2.1	8 4.2 3.5	ns	Pin Type 4mA Pin Type 12mA Pin Type 16mA

4.3.1.2 I/O Digital Specifications for VDDIO=1.7V to 1.98V

Table 14, page 48 lists the parameters for I/O digital specification for VDDIO 1.7V to 1.98V for Pin Types 4mA, 12mA, and 16mA.

Table 14 I/O Digital Parameters for VDDIO=1.7V to 1.98V

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Note
I/O Supply Voltage	V_{DDIO}	1.7	1.8	1.98	V	
Input Low Voltage	V_{IL}	-0.3		$0.3*V_{DDIO}$	V	
Input High Voltage	V_{IH}	$0.7*V_{DDIO}$		VDDIO	V	
Input Leakage Current	I_L			10	µA	Pull up/down disabled
Tri-State Output Leakage Current	I_{OZ}			10	µA	Pull up/down disabled
Pull-Up Resistor	R_u	66K	114K	211K	Ω	
Pull-Down Resistor	R_d	58K	103K	204K	Ω	
Output Low Voltage	V_{OL}	0		0.45	V	
Output High Voltage	V_{OH}	$0.8*V_{DDIO}$			*V*	
Low Level Output Current @ V_{OL} max	I_{OL}	2.6 8.0 10.8			mA	Pin Type 4mA Pin Type 12mA Pin Type 16mA
High Level Output Current @ V_{OH} min	I_{OH}	1.7 5.0 6.6			mA	Pin Type 4mA Pin Type 12mA Pin Type 16mA
Output rise time 10% to 90% load, 30pF	t_{TRLH}	5.3 2.6 2.1	8.4 4.2 3.4	13.9 7.0 5.8	ns	Pin Type 4mA Pin Type 12mA Pin Type 16mA
Output fall time 90% to 10% load, 30pF	t_{TFHL}	5.29 2.73 2.30	8.1 4.2 3.6	14.0 7.2 6.1	ns	Pin Type 4mA Pin Type 12mA Pin Type 16mA

4.3.2 RTC I/O Specifications

Table 15, page 49 lists the RTC I/O parameters.

Table 15 RTC I/O Parameters

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Note
Supply Voltage	VRTC	1.6		3.6	V	
Input Low Voltage	V_{IL}	-.03		$0.3*V_{RTC}$	V	
Input High Voltage	V_{IH}	$0.7*V_{RTC}$		VRTC+0.3	V	
Input Leakage Current	I_L			0.1	µA	
Pullup Current	I_{PU}		1		µA	
Pulldown Current	I_{PU}		1		µA	
Output Low Voltage	V_{OL}			0.4	V	IL=1mA or 4mA*
Output High Voltage	V_{OH}	VRTC-0.4			V	IL=1mA or 4mA*

*RTC I/O's are software selectable as 1mA (default) or 4mA drive strength.

4.4 Power Consumption

Table 16, page 50 lists the power consumption for the GS2200M. Typical conditions are: VIN_3V3=VDDIO=VRTC=3.3V, VREG=1.8V, Temp=25^{o}C.

Table 16 Typical Power Consumption in Different States

System State	Typical LDO_IN pins current@ 1.8V (see Note 5)	Typical Current Other Supply Pins @ 3.3V	Typical Total System Current @ 3.3V (see Note 4)
Hibernate (only VRTC ON other power OFF, 32KHz OFF) (GS2000-124 only)	-	0.26µA	0.26µA
SStandby (only VRTC ON other power OFF) (GS2000-124 only)	-	4-8µA	4-8µA
Deep Sleep (see Notes 1 and 2)	570µA	40µA	475µA
WLAN Continuous RX (1 Mbps)	128mA	3.5mA	88mA
WLAN Continuous TX (1Mbps, +17dBm)	110mA	225mA	300mA
PS-Poll, DTIM=1, 2mS beacon, Note 3	2.64mA	162µA	2.08mA
PS-Poll, DTIM=1, 2mS beacon, Note 3	3.82mA	198µA	2.85mA
PS-Poll, DTIM=3, 1mS beacon, Note 3	1.44mA	81µA	1.20mA
PS-Poll, DTIM=3, 2mS beacon, Note 3	1.81mA	93µA	1.45mA
PS-Poll, DTIM=10, 1mS beacon, Note 3	522µA	46µA	402µA
PS-Poll, DTIM=10, 2mS beacon, Note 3	654µA	49µA	495µA

Note:

1. It depends on the firmware version.
2. One sigma is +/-200µA @ 1.8V, and +/-140µA in total system @ 3.3V.
3. It is the average current. PS-Poll current is given for both 1mS and 2mS beacon duration. DTIM=1 and DTIM=3 uses the deep sleep state between beacons while DTIM 10 uses the standby (GS2000-124 only).
4. Column 2 and 3 shows the current consumption at SOC pins. The column 4 indicates the total power consumed @ 3.3V by using an external 1.8V switching regulator and a load switch driven by the DC_DC_CNTL pin. Note that the 1.8V switching regulator's output current is greater than the regulator's input current, so the power calculation in the right column is less than the sum of the left two columns.
5. The current consumption is the same even if the LDO_IN pins are powered from 3.3V instead of 1.8 V, the additional power is consumed by the on-chip LDO regulator.

4.5 802.11 Radio Parameters

Table 17, page 51 lists the 802.11 Radio parameters. Test conditions are: VIN_3V3=VDDIO=VRTC=3.3V Temp=25°C.

Table 17 802.11 Radio Parameters - (Typical - Nominal Conditions)

Parameter	Minimum	Typical	Maximum	Unit	Notes
RF Frequency Range	2400		2497	MHz	N/A
Radio bit rate	1		HT20 MCS7	Mbps	N/A
Transmit/Receive Specification for GS2200M (See Note 1)					
Output power (average)		14 11 10 13 13 7 12 10 3		dBm	11b, 1Mbps 11b, 5.5Mbps 11b, 11Mbps 11g, 6Mbps 11g, 18Mbps 11g, 54Mbps 11n, MSC0 11n, MCS3 11n, MSC7
Spectrum Mask				dBr	Meets 802.11 requirement for selected data rates
Receive Sensitivity at antenna port		-90 -84 -86 -71 -86 -67		dBm	11b, 1Mbps 11b, 11Mbps 11g, 6Mbps 11g, 54Mbps 11n, MSC0 11n, MSC7

NOTE: 1. *Transmit/Receive specifications are measured using a conducted test with uFL connector.*

4.6 SAR_ADC Parameters

Table 18, page 52 lists the SAR_ADC parameters. Test conditions are: VIN_3V3=VDDIO=VRTC=3.3V Temp=25^{o}C.

Table 18 SAR_ADC Parameters

Parameter	Minimum	Typical	Maximum	Unit	Notes
ADC Resolution	-	12	-	Bits	
Conversion Speed (F_S)	0.01	-	2	Msps	
Input Voltage Full Scale range	0		1.4	V	Internal Reference
	0		VIN_3V3	V	External Reference
ADC Integral Non-Linearity (INL)	-	-	$\pm$2	LSB	
ADC Differential non-linearity (DNL)	-	-	$\pm$1	LSB	see Note 1
Active Current		800		µA	F_S=2Mbps, Internal reference (Reference Buffer on) 3.3V
		550		µA	F_S=32KHz, Internal reference (Reference Buffer on) 3.3V
		450		µA	F_S=2Mbps, External reference (Reference Buffer off) 3.3V
		180		µA	F_S=32KHz, External reference (Reference Buffer off) 3.3V
ADC Offset Error	-30	-	30	mV	

Table 18 SAR_ADC Parameters (Continued)

Parameter	Minimum	Typical	Maximum	Unit	Notes
ADC Gain Error	-8	-	8	LSB	see Note 2
Error in Internal Reference Voltage without Trim	-5	-	5	%	
Error in Internal Reference Voltage with Trim	-2.5		2.5	%	

Notes:

1. No missing codes.

2. This is the gain of the ADC core measured in External reference mode.

4.7 Sigma Delta ADC Parameters

Table 18, page 52 lists the Sigma Delta ADC parameters. Test conditions are: VIN_3V3=VRTC=3.3V Temp=25°C.

Table 19 ADC Parameters

Parameter	Minimum	Typical	Maximum	Unit	Notes
D/A DC Performance (see Note 1)					
Resolution	-	16	-	Bits	
Full Scale		2.4	0	V	See Note 2
Output common-mode level		VIN_3V3/2			
Gain Error	-	-	±5	%	See Note 2
Offset	-	-	±20	mV	
D/A Dynamic Performance					
Data Rate	32	-	80	KHz	
Clock Frequency	8	-	20	MHz	See Note 3
Signal to Noise Ratio (SNR)		67	-	dB	See Note 4
Total Harmonic Distortions (THD)	-	-74		dB	
Output load	10			KΩ	
Output load			30	pF	
A/D DC Performance (Preamplifier Gain=0db)					
Resolution		16		Bits	
Full Scale		2.0		V	
Input common-mode level		VIN_3V3/2			
Gain Error			±3	%	
Offset			±10	LSB	
A/D Dynamic Performance (Preamplifier Gain=0db)					
Data Rate	32		80	KHz	
Clock Frequency	8		20	MHz	See Note 3
Signal-to-Noise Ratio (SNR)		80		dB	See Note 4
Total Harmonic Distortion (THD)		-85		dB	See Note 4
Input Resistance	100			KΩ	

Chapter 5 Package and Layout Guidelines

This chapter describes the GainSpan® GS2200M package and layout guidelines.

5.1 GS2200M Recommended PCB Footprint and Dimensions

Figure 9, page 56 and Figure 10, page 57 shows the module dimensions. Figure 11, page 58 shows the recommended footprint. The module pins are split into 7 groups, as shown in Figure 10, page 57. For each group the center for one pin is specified in Figure 9, page 56. The other pins are centered based upon the pin pitch for the group, given in Figure 10, page 57.

Figure 9 GS2200M Module Dimensions (in millimeters)

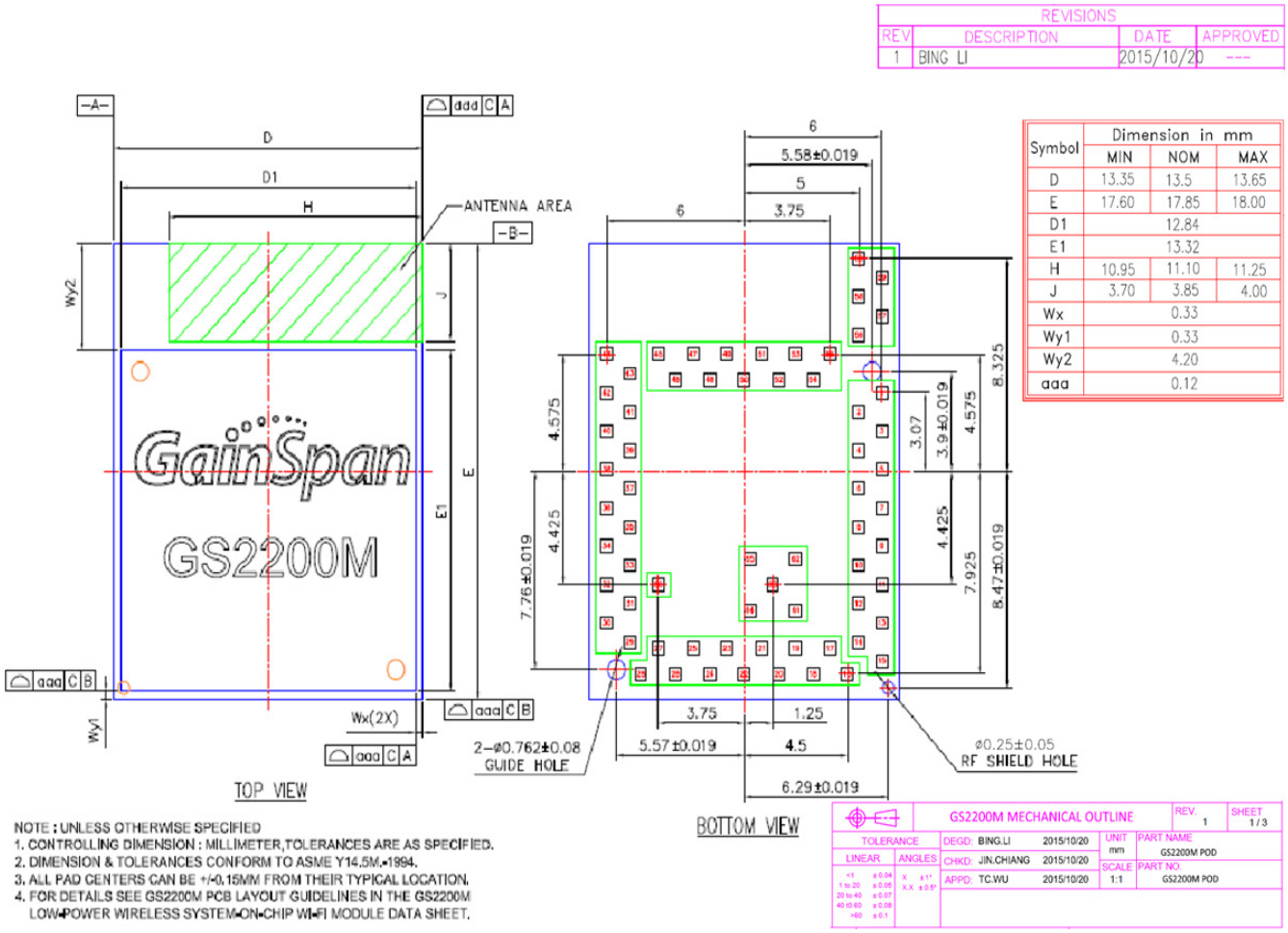
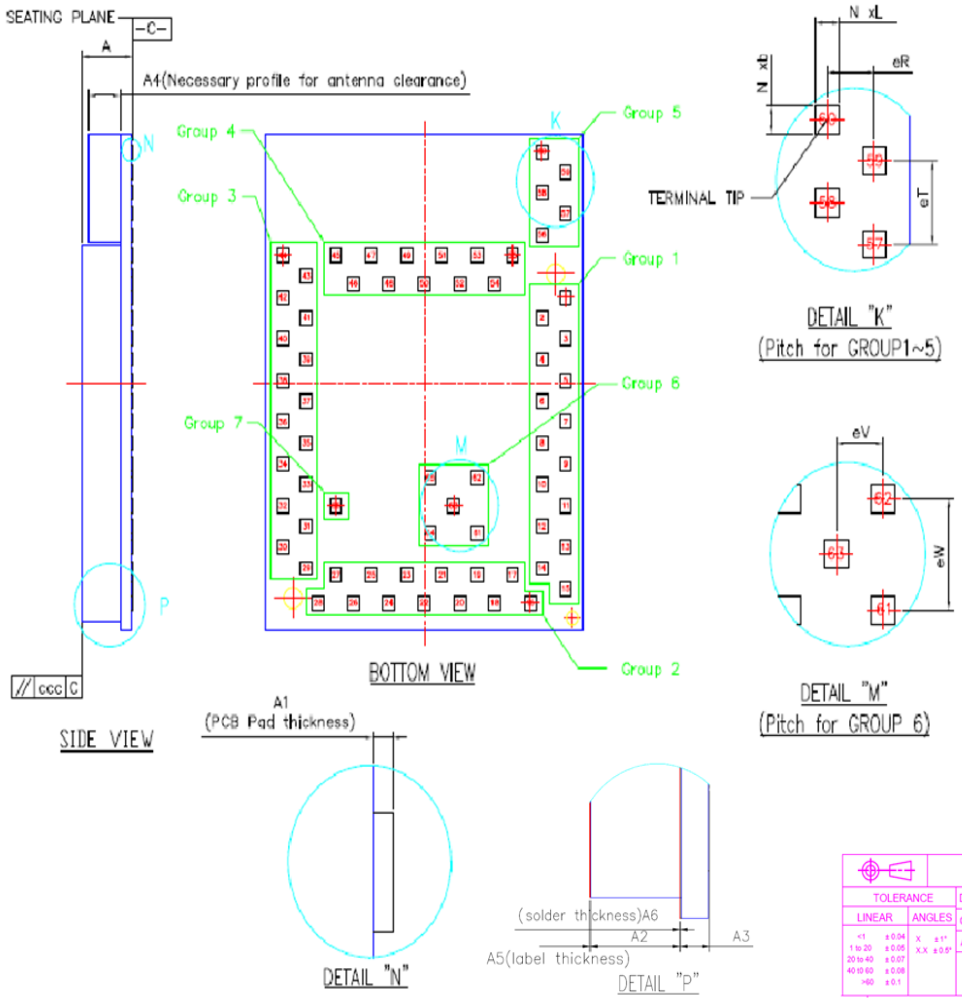


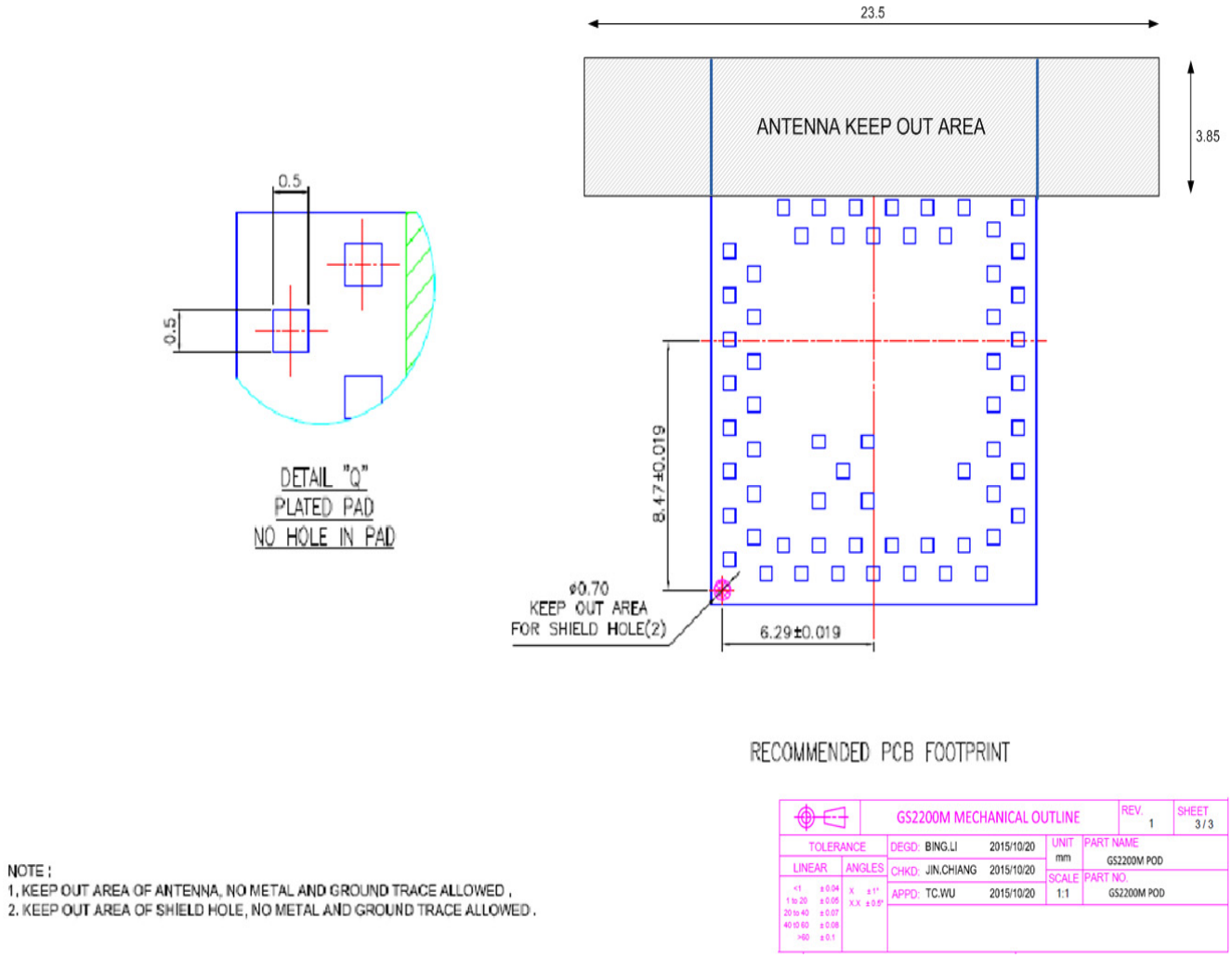
Figure 10 GS2200M Module Dimensions (in millimeters) - (Continued)



Symbol	Dimension in mm		
	MIN	NOM	MAX
A	2.129	2.249	2.369
A1		0.036	
A2	1.46	1.52	1.58
A3	0.529	0.579	0.629
A4		1.35	
A5	0.04	0.05	0.06
A6		0.10	
N		66	
b	0.47	0.5	0.53
L	0.47	0.5	0.53
eT		1.5	
eR		1.0	
eV		1.0	
eW		2.0	
ccc		0.12	

GS2200M MECHANICAL OUTLINE			REV. 1	SHEET 2 / 3
TOLERANCE	DEGD: BING.LI	2015/10/20	UNIT mm	PART NAME GS2200M POD
LINEAR ANGLES	CHKD: JIN.CHIANG	2015/10/20	SCALE 1:1	PART NO. GS2200M POD
	APPD: TC.WU	2015/10/20		

Figure 11 GS2200M Module Recommended PCB Footprint (in millimeters)



Notes:

1. GainSpan recommends that the antenna area have only air on **BOTH** sides. It can be either:
   a. Hung over the edge of the base board. In this case, it is OK for there to be no connection to pads 56-60.
   b. Over a cutout at the edge of the base board. No metal or FR4 under or encircling the antenna.
2. Nothing conductive near antenna (battery, display, wire, etc.).
3. GND plane on **layer 1**, connecting to pads 1-6, 8, 43-55, and 61-66. Do not connect pads 56-60. These pads are in the antenna keep-out area of figure 9, and should be hung over the edge of the customer board or have a cutout under them. The reason for GND to be on layer 1 is for thermal performance. Use thermally relieved pads to the L1 GND plane. Provide GND or at least a very thick connection back to the voltage regulator providing VIN_3V3 power.

4. Use 3 vias any time that GND or VIN_3V3 power changes layers.
5. Isolate PWR/GND from high frequency or high current parts. For example, use a notch in the GND plane between a host uC and the GS2200M.
6. Provide a 4.7uF or greater capacitor at the VIN_3V3 pin. 3 vias on BOTH sides of the capacitor.
7. Keep high speed signals away from the module. Route signals outwards from the module pins on layer 1, not under the module. For other PCB layers, it is OK to route signals under the module if and only if there is GND plane between the signal and the module.
8. The RF shield hole has exposed metal on the bottom of the module. GainSpan recommends that the base board have no metal in this area.
9. Do not use a metallic or metalized plastic for the end product enclosure when using on-board antenna.
10. If the module is enclosed in a plastic case, have reasonable clearance from plastic case to on-board antenna.

5.1.1 Surface Mount Assembly

The reflow profile is shown in Figure 12, page 59. The recommended reflow parameters are summarized in Table 20, page 59.

Figure 12 Reflow Temperature Profile

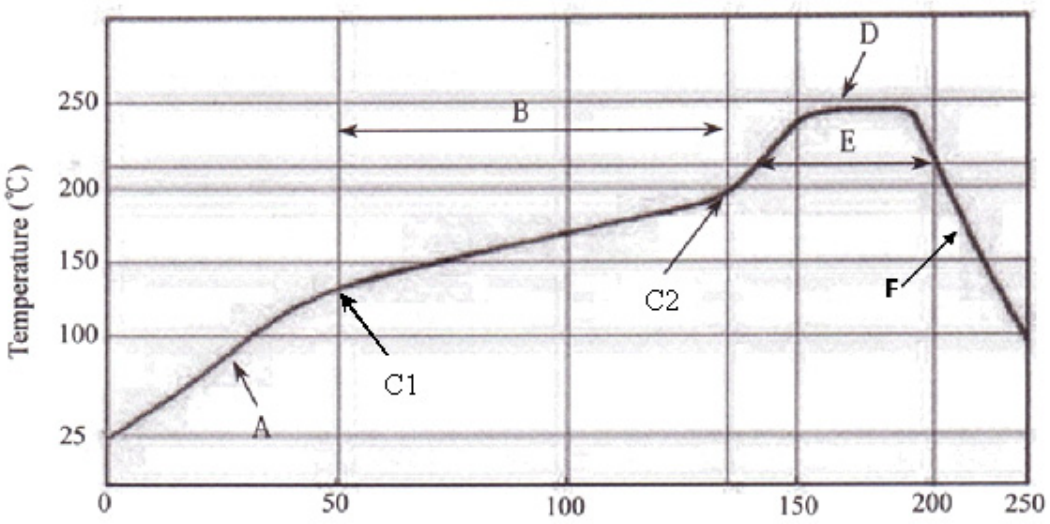


Table 20 Recommended Reflow Parameters

Preheat	
Temperature Ramp up rate for (A)[2]	1.5~3.5 °C/s
Pre-heat time (B)[3]	80 to 130 seconds
Pre-heat starting temperature (C1)	125 to 135 °C

Table 20 Recommended Reflow Parameters (Continued)

Preheat	
Pre-heat ending temperature (C2)	180 to 200 ^{o}C
Heating[5]	
Peak Temperature range (D)	240 to 250 ^{o}C
Melting time[4] that is the time over 220 ^{o}C (E)	50 to 75 seconds
Cool Down Ramp (F)	>2 ^{o}C/s

Notes:

1. Perform adequate test in advance as the reflow temperature profile will vary according to the conditions of the parts and boards, and the specifications of the reflow furnace.
2. Max number of reflow supported are two.
3. Temperature uniformity inside the IR reflow oven must be tightly controlled and multiple thermocouples should be used. An example of possible thermocouple locations is given in Figure 13, page 61. The locations should also include multiple points INSIDE the module RF shield (e.g., TC1, TC5, and TC7 in Figure 13, page 61). The temperature profile of ALL thermocouples must meet the requirements of Table 20, page 59.
4. Pay close attention to “Melting Time over 220^{o}C”. Sufficient time is necessary to completely melt all solder.
5. Be careful about rapid temperature rise in preheat zone as it may cause excessive slumping of the solder paste.
6. If the preheat is insufficient, rather large solder balls tend to be generated. Conversely, if performed excessively, fine balls and large balls will generate in clusters at a time.
7. If the temperature is too low, non-melting tends to be caused in the area with large heat capacity after reflow.
8. Be careful about sudden rise in temperature as it may worsen the slump of solder paste.
9. Be careful about slow cooling as it may cause the positional shift of parts and decline in joining at times.
10. A no clean flux should be used during SMT process.

Note: The modules are shipped in sealed trays with the following conditions (see Figure 14, page 62).

Figure 13 Thermocouple Locations

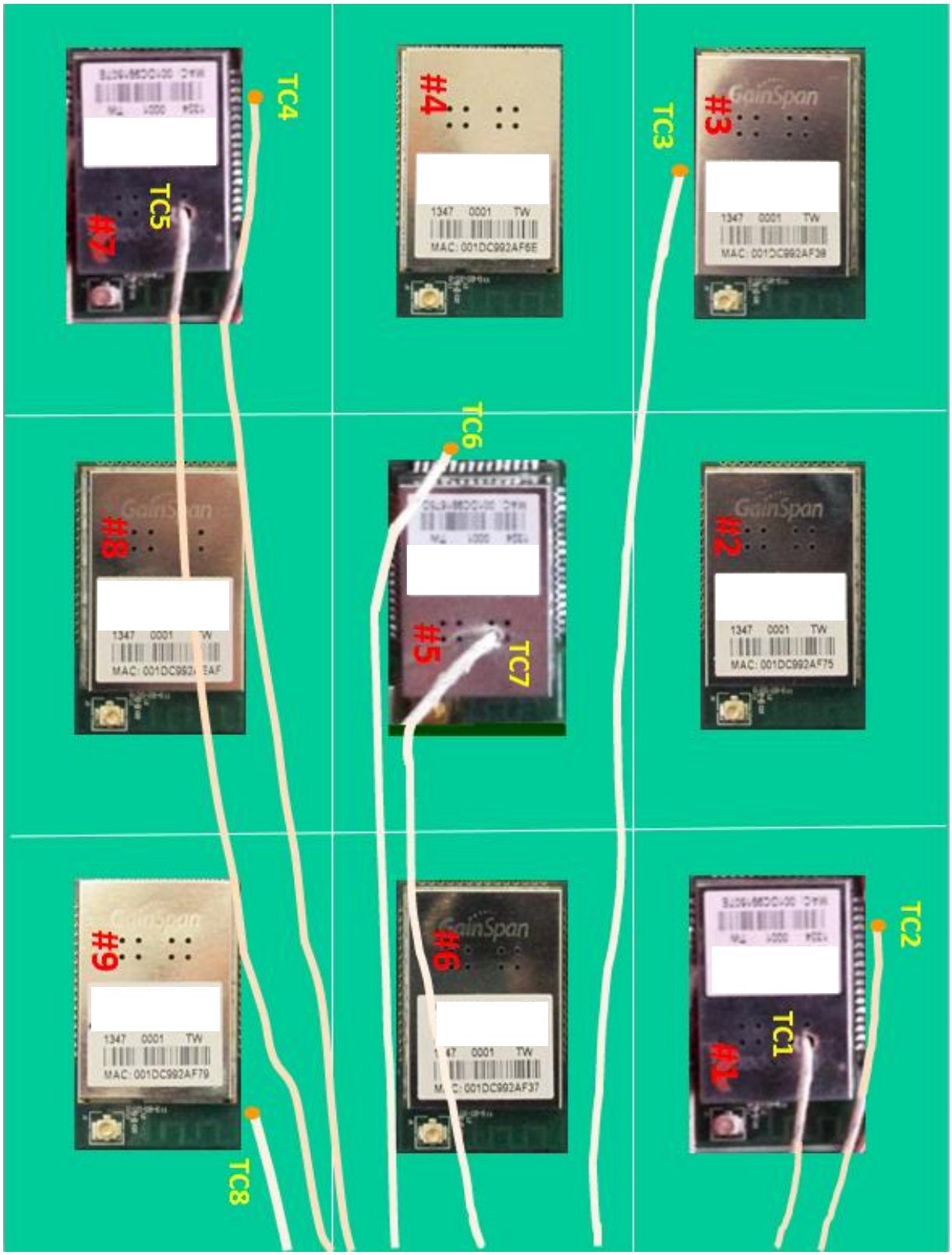
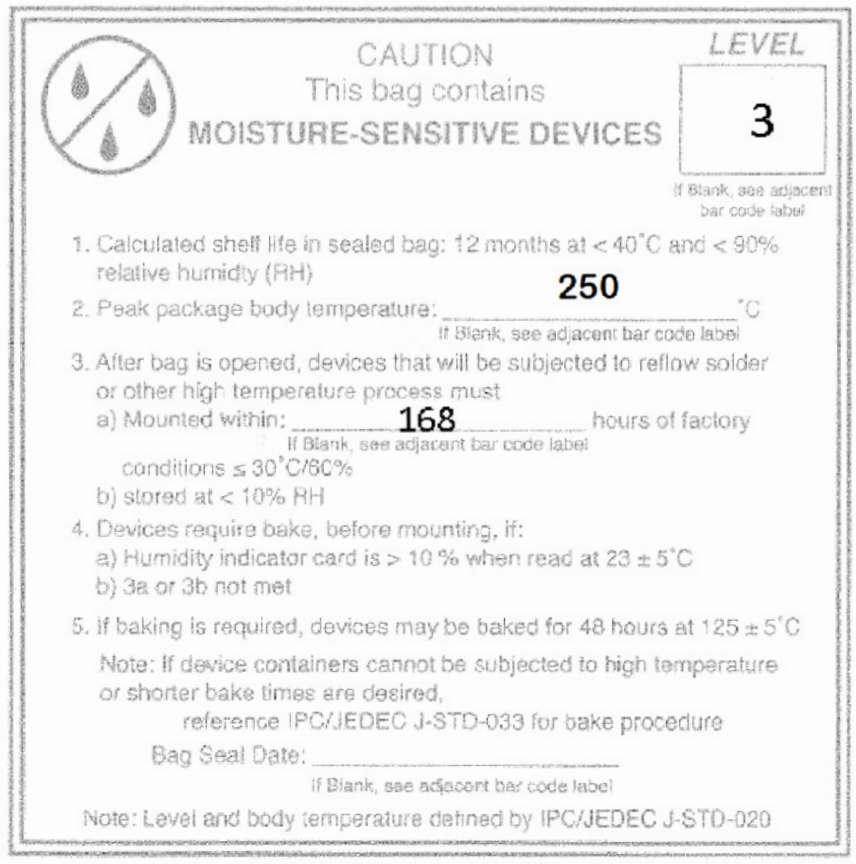


Figure 14 Module Moisture Conditions



SUPPORT INQUIRIES

Link to **www.telit.com** and contact our technical support team for any questions related to technical issues.

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