JF2 SPI-UART-I2C Application Note

80000NT10068A Rev.2-2013-10-31

APPLICABILITY TABLE

PRODUCT
JF2

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Contents

Mod. 0809 2011-07 Rev.2

1. Introduction

1.1. Scope

Scope of this document is to give an overview of communication interfaces available in the GPS module Jupiter JF2.

1.2. Audience

This document is intended for customers aiming to develop applications with JF2.

1.3. Contact Information, Support

For general contact, technical support, to report documentation errors and to order manuals, contact Telit Technical Support Center (TTSC) at:

TS-EMEA@telit.com
TS-NORTHAMERICA@telit.com
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Alternatively, use:

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Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

1.4. Document Organization

This document contains the following chapters (sample):

Chapter 1: "Introduction" provides a scope for this document, target audience, contact and support information, and text conventions.

Chapter 2: "Overview" gives an overview of the serial host communications port of the JF2.

Chapter 3: "Implementation" describes in details the characteristics of the product.

Chapter 4: "UART" describes the UART serial host interface

Chapter 5: "SPI Slave Mode" describes the SPI serial host interface

Chapter 6: "I2C" describes the I2C serial host interface.

Chapter 7: "Document History" details the document history.

1.5. Text Conventions

Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

1.6. Related Documents

- JF2 Product Description, 80403ST10103A
- JF2 Hardware User Guide, 1vv0300985
- JF2 EVK User Guide, 1vv0300987

2.   Overview

At start-up, the JF2 Host port can be configured to have UART, SPI, or I^{2}C data format. This is done by the GPS sensing the state of GPIO6 and GPIO7 pins at start up.

The serial port outputs are 1.8V logic based, while the inputs are 1.8V to 3.6V tolerant.

This document describes the operation of the host serial interfaces on the JF2.

Refer to documentation available under Non-Disclosure Agreement (NDA) on features and functions of the JF2 which have critical reliance on proper operation of the host serial port interfaces:

- NMEA Message Protocol
- OSP Messaging Protocol
- SGEE Downloader
- Host Data storage for SGEE, CGEE, and BE

3.   Implementation

The JF2 supports 3 interface types:

- Slave SPI
- UART
- Multi-master I^2C

3.1.   Port Selection Configuration

A 10kΩ resistor will be needed for pull-ups to 1.8V or pull-downs to ground. Table 1 indicates the state of GPIO7 and GPIO6 during the start up sequence for the three communication modes.

	GPIO7	GPIO6
UART	No Connect: Weak internal pull up	External Pull UP 10kΩ to 1.8V
SPI	Weak internal Pull up (becomes SPI CS)	Weak internal Pull down (becomes SPI CLCK)
I^2C	External Pull Down 10kΩ	No Connect: Weak internal pull down

TABLE 1 PORT SELECTION.

Port type can be changed by OSP command, however, the host must match the JF2 correctly at the same instant. OSP message transport, message integrity, acknowledgement, and sequencing during such a commanded transition is not guaranteed.

Pin Assignments	Quick Name	Interface signal names		
JF2		SPI	UART	I^2C
10	TXA	*SSPI_DO*	TXA	I^2C_CLK
11	RXA	*SSPI_DI*	RXA	I^2C_DIO
23	GPIO6	*SSPI_CLK*	*(Not Used)*	*(Not Used)*
24	GPIO7	*CS_SPI*	*(Not Used)*	*(Not Used)*

TABLE 2 INTERFACE SIGNAL NAMES

3.2. Message Rates

3.2.1. Input to the JF2

Maximum sustained inflow at the rate of command messages should not exceed about 10,000 characters per second. Above 115.2kbps, such as 1228800 bps (122880 characters per second), input flow should be limited to less than 10,000 characters/sec to keep from choking the system. Command processing is a low priority task within the system.

At higher data rates, TELIT recommends using OSP message/ACK protocol to prevent message loss.

Low data rates impact startup and TTFF values in sending configuration commands and patches to ROM-based devices and when using host storage for JF2 data files.

3.2.2. Output from the JF2

Users can control selection and rate of delivery of some output messages through OSP or NMEA configuration commands

Debug messages are controlled as a block and cannot be individually selected.

Some event or alarm messages occur spontaneously and cannot be directly controlled.

You must assess the capacity of the communications link between JF2 and the host. You must select OSP or NMEA messages appropriate to the application and well within the maximum capacity of the communications link. In assessing the capacity required, consider the protocol overheads and maximum size of variable payloads.

In power consumption-critical applications, any time spent creating and sending messages causes both the JF2 and the host to consume power. A low data link speed extends the current consumption of both host and JF2.

3.3. Message Timing

The host serial port driver is ready about 150ms after the baseband has been started with an ON_OFF pulse, at which time an OK to SEND message (NMEA message $PSRF150, OSP Message ID 18) is transmitted.

Commands can be sent continuously but at least one second must be allowed for their processing

Input commands are generally processed within 200ms of receipt. An acknowledgement message is generally available after an OSP command is processed.

3.4.   Message Protocols

Messages must be in the appropriate protocol supported:

- **NMEA** as described in the *NMEA Reference Guide*
- **OSP** as described in the *One Socket Protocol Interface Control Document*

The system does not support concurrent operation of NMEA and OSP on the same serial port.

3.5.   Configuration Setting Cautions

The Host Port Selects are read the first time an ON_OFF is pulsed after an internal RESET or an external NRESET. A subsequent ON_OFF pulse does not cause another reading. To allow a correct reading of the Host Port Selection, it is necessary to maintain the correct levels on GPIO6 and GPIO7 for 100ms after pulsing ON_OFF. Typical usage has the GPIOs input levels set by weak internal pull resistors or strong external pull resistors.

Note
When connected to a host or other interface device, the product designer must assess and control the risk of any external drive or inadvertent leakage into these lines to ensure the correct configuration is selected.

An internal RESET occurs when
- Power is first applied to the JF2
- The external NRESET input is asserted and released.

3.6.   Data Ready Indicator

From software version v4.1.0, GPIO3 can be used as a message-ready indicator to make host interfacing easier in slave SPI operation. If there is no data to transmit, GPIO3 stays low. GPIO3 goes high when data is ready to be sent out, and after completion of all data transmission, it goes low again. It is supported in two modes: SPI slave, and UART with flow control enabled. Note that GPIO3 is also used for antenna sense depending on software.

4.   UART

UART is normally used for GPS data reporting and receiver control.

	JF2 Pin	Pin Config/Definition
GPIO6	23	Pull UP with 10kΩ
GPIO7	24	No connect

TABLE 3 PORT SELECTION UART

The features of the JF2's UART include:

1. Transmit and receive channel contain a 64B FIFO
2. Serial data rates are selectable from 1200baud to 1.8432Mbaud.
3. Programmable fill interrupt for the receiver, based on selecting the fill level alarm for the receiver FIFO. (i.e.) set at when FIFO contains 64 N Bytes.
4. Interrupt available when transmitter is empty.
5. Clock source is DLL/2
6. A timer is provided to generate an interrupt when:

    a. The receiver FIFO is not empty
    b. The receiver FIFO fill level does not exceed the alarm level
    c. There are no received bytes for a programmable number of UART source clock ticks
    d. Signals for frame error, parity error, overrun error, and break interrupt.

JF2	In/Out	Pull	Name	Description, Voltage, Notes
10	O	None	TXA	JF2 output / Host input, 1.8 V
11	I	High	RXA	JF2 input / Host output, 1.8 V

TABLE 4 UART PINOUTS

4.1. Description

At boot up, the software uses different default data rates depending on the protocol selected, in OSP mode it is 115200 baud and in NMEA mode it is 4800 baud. The software can set the program the rate depending on the type of operation, such as FLASH code upload.

4.2. Run-Time Operation

4.2.1. TX/RX Electrical

- "1" (mark) is logic high
- "0" (space) is logic low
- idle line = logic high
- Line-break/open line is continuous logic low. (Continuous break is not allowed on RX during operation and not generated on TX during operation.)

4.2.2. Data frame length

8-bit octets only.

4.2.3. Receive Frame format

1 start bit, 8 data bits with least significant bit (bit 0) to most significant bit (bit 7), 1 stop bit or longer is accepted, and parity is generally not used.

4.2.4. Transmit Frame Format

1 start bit, 8 data bits with least significant bit (bit 0) to most significant bit (bit 7), 2 stop bits followed by next character or idle line. The JF2 UART hardware is preset to output 2 stop bits and this is not changeable by configuration. Designers should treat computations of maximum message output capacity from JF2 with 11-bits per character. This effectively decreases line capacity by about 10% and increases CPU and host ON time for message exchange by about 10% above expected.

Not all possible data rates are supported by every firmware version.

Current UART data rates in kbps are: 4.8, 9.6, 19.2, 38.4, 57.6, 115.2, 230.4, 460.8, 921.6 and 1228.8. Note that the data rate can be higher but has not been tested. Operation at line speeds above 115.2 kbps has not been rigorously tested and verified.

Because UART transmission is asynchronous and sampled by the receiver, both sender and receiver require closely matched bit-rate clocks, and that data bit waveform and timing distortion at the receiver should be limited.

Maximum allowed clock rate difference between JF2 and host is 2.0% overall.
Maximum bit-edge distortion = <5% UI, maximum bit jitter = <5% UI.

[1/data bit rate = Unit Interval or UI]

4.2.5.   Message Rates

Input to the JF2:

The JF2 cannot support sustained, continuous *command* inflow at rates in excess of about 115.2 kbps.

The JF2 can support serial port operation at speeds above 115.2 kbps for *data* download of EE files, ROM patches and loading flash memory.

At high data rates, use of OSP message/ACK protocol is recommended to prevent message loss.

Low data rates will impact the TTFF values expected when using host storage for EE data file interaction. For example, downloading a single EE data block for one satellite in NMEA at 4.8 kbps, will take about ½ second. Refer to CGEE and SGEE documentation for the sizes of various messages and files.

Low data rates will impact the time taken to apply patches to ROM-based devices. Refer the JF2 Patch Manager documentation for the sizes of various messages and files.

Output from the JF2:

Selection and rate of delivery of some output messages can be controlled by OSP or NMEA configuration commands.

The default master message scheduler is based on a 1 Hz timer. A 5 Hz timer is also available for more frequent output of selected messages.

Some messages such as debug messages are enabled en-bloc.

Some event messages are sent on occurrence of an event and are not directly controlled.

Messages associated with request and transfer of EE data between host and the JF2 may not be configurable.

Customer is responsible to assess the capacity of the communications link between JF2 and host and select OSP or NMEA messages appropriate to the application and well within the maximum capacity of the communications link. In assessing the capacity required, all protocol overheads as well as maximum size of variable size payloads must be considered. (For example, NMEA GSV message can range from an empty single message about 20 characters long including header and ender, to three consecutive messages of about 80 characters each).

In power-consumption-critical applications, any time spent in creating and sending messages causes both the JF2 and the host to consume power – a low data link capacity will needlessly extend current consumption of both host and JF2.

4.2.6.   Message Timing

UART driver is ready about 200-400 ms after the baseband has been started with ON_OFF pulse as indicated by transmission of an "OK to SEND" message.

Commands can be sent continuously but at least one second must be allowed for their processing.

Input commands are generally processed within 200 ms of receipt. An acknowledgement message is available after the command is processed.

4.2.7. Message Protocols

Messages must be in the appropriate protocol supported: NMEA as described in the NMEA protocol reference manual as appropriate for the firmware version or OSP as described in the OSP Reference manual as appropriate for the firmware version.

4.2.8. Internal Details

The following internal operation details are provided for information only:

- Internal FIFOs: RX 16 bytes, TX 16 bytes

- Sampling Clock: = ½ CPU clock counted by N to sample data bit mid-point

- Start bit detection: 1>0 edge transition and sample at ½ UI of start bit time

- False start bit detection: After 1>0 edge detection, sample at ½ start bit time must be 0

- Interrupts for RX input FIFO not empty and TX FIFO refill level reached

- UART sampling rate is RTC*3340/2. The resulting error between nominal UART bit clocking rate and actual JF2 bit clocking rate can be determined as:

$$100\% \times \Big(\big((RTC \times 3340 \div 2) \\ \div (Round[RTC \times 3340 \div 2) \div BPSRate_{Nominal}, \quad 0]\big) \\ - BPSRate\_Nominal \Big)$$

  o   where RTC is nominal 32.768000 kHz but may vary by +25 ppm /-200 ppm

Configuration 1

- RX and TX data lines only, No hardware or software flow control

Configuration 2

- RX and TX lines for data transmission

- RTC and CTS for hardware flow control under standard hardware flow control principles

  o   Transmission stops at the end of the current character and restarts when CTS goes high.

- Note that JF2 may lose or garble serial messages if host flow control throttling is too severe. System design assumes unrestricted outflow of serial messages.

4.2.9.   Cautions

When switching the unit to hibernate mode using orderly shutdown with ON_OFF pulse or by OSP/NMEA command message, the JF2 will continue to run until the transmit/output buffers are emptied.

At slow serial port speeds with a high volume of data, time-to-turn-off may be up to one second.

If host flow control prevents output of final messages, the JF2 will not turn off.

5. SPI Slave Mode

This section describes how to configure the serial port for SPI slave mode.

	JF2 Pin	**Pin Definition**
TXA	10	SPI DATA OUT/MISO
RXA	11	SPI DATA IN/ MOSI
GPIO6	23	SPI CLOCK
GPIO7	24	SPI CHIP SELECT

TABLE 5 PIN DEFINITIONS IN SPI

Electrical Interface: CMOS at 1.8 V:

- The maximum clock frequency supported is 6.8MHz.
- The four primary pins are Host SPI serial Input (Master Out, Slave In, or MOSI), Host SPI serial Output (Master In Slave Out, or MISO), Host SPI Select Input, and Host SPI clock Input.
- While Host SPI serial Input and Host SPI clock Input are 3.3 V compatible, if Host SPI serial Input is driven from a source higher than 1.8 V, excess leakage current may flow through the ~80 kΩ internal pull-up resistor
- Host SPI serial Output has maximum 1.8 V logic high output level and may require an external level shifter to interface with a 3.3 V input.
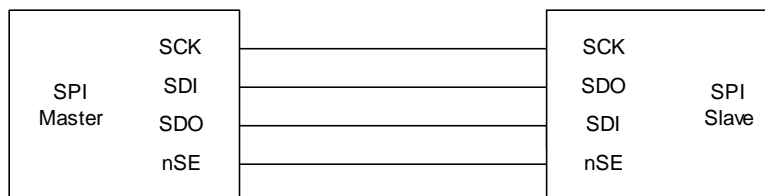

FIGURE 1 SPI MASTER SLAVE CONNECTION

5.1. Description

Once the SPI mode has been selected the GPIO7 and GPIO6 pins change function:

SPI SLAVE MODE ONLY.

JF2	In/Out	Pull	Name	Description, Voltage, Notes
10	O	None	*SSPI_DO*	Host SPI serial Output (MISO), 1.8 V
11	I	None	*SSPI_DI*	Host SPI serial Input((MOSI), 1.8 V
23	I	None	*SSPI_CLK*	Host SPI clock Input, 1.8 V
24	I	High	$\overline{CS\_SPI}$	Host SPI Select Input, 1.8 V, active low

TABLE 6 SPI PINOUTS

5.2. Run Time Operation

5.2.1. Hardware Interface

JF2 operates only as SPI slave. This requires that the host drive the SPI clock and JF2 SPI chip select lines when it wishes to receives messages from the JF2.

5.2.2. Transmission

To begin a communication, the master pulls the JF2 SPI Chip Select input (nCS_SPI) low. The master then generates a clock frequency less than or equal to the maximum frequency the slave device supports. During clock generation, a full duplex transmission occurs:

- the master sends data on its SDO (MOSI) line; the slave reads from its SDI line
- the slave sends data on its SDO (MISO) line; the master reads from its SDI line

5.2.3. Clock polarity and phase

There are four modes of communication between the master and server depending on the clock polarity and clock phase with respect to data.

The CPOL defines the polarity of clock as CPHA does the clock phase. When CPOL is zero, the clock stays low and the status of clock phase is determined by CPHA. If CPHA is zero, data is read on the clock's rising edge and changed on a falling edge. If CPHA is high, data is read on the clock's falling edge and changed on a rising edge. When CPOL is one, it is opposite of when the CPOL is zero. The clock stays high in the idle state. If CPHA is zero,

data is read on clock's falling edge and data is changed on a rising edge. If it is one, data is read on clock's rising edge and data is changed on a falling edge

It is important that the CPOL and CPHA match between the master and slave. These are set in the JF2 by default to CPOL = 0, CPHA = 1, and cannot be changed under normal circumstances. The combinations of polarity and phase are often referred to as modes which are commonly numbered according to the following convention:

Mode	CPOL	CPHA	JF2 Comments
0	0	0	Not supported
1	0	1	Supported
2	1	0	Not supported
3	1	1	Supported

TABLE 7 SPI MODES CONVENTION

Please note that only 2 modes out of four are supported, and to change from default mode 1 to mode 3 requires special software from Telit.

5.2.4.   Operation

SPI mode 1 is the default mode. Maximum SPI clock rate is about 6.8 MHz. Firmware currently supports only the SPI format, not MicroWire. Frame size is 8 bits, with MSB sent first. There are no unique SPI headers; the payload is the same structure as the message. NMEA messages and OSP messages each have their own unique start-of-message, end-of message patterns and message data structures.

Operation is concurrent bi-directional full-duplex and starts when nCS_SPI is asserted and SPICLK is active.

Idle line characters are used when the sender has nothing to send

Receive operations do not require an enable. When the system is first turned on, the master in the host system is able to send a message before software has set up the receive idle pattern filter. The host must poll continuously for the first message indicating that the JF2 is ready.

In general, the JF2 loads an "OK to Send" message to its TX_FIFO to inform the host that operations can begin. The query is typically sent every 500 ms to limit the receive byte volume until idle pattern filters are established.

On JF2 receive side, the host is expected to transmit idle pattern when it is querying the JF2 , unless it has messages to send to the JF2 . This keeps the processing effort low since hardware does not place most idle pattern bytes in the RX FIFO.

Most messaging can be serviced with polling. Since message creation times have about 200 ms of jitter from second-to-second, the host must accommodate and early start of polling

before messages are expected to be ready. Any delay in polling increases the latency between actual position and the time the position is received and processed and displayed by the host.

There is a JF2 GPIO indicator option which may be used as "message waiting" to signal the host to start polling.

When transmitting, the JF2 fills its FIFO with as many queued up messages as can fit in the FIFO. The host is required to poll messages until idle pattern bytes are detected. The JF2 replenishes its TX-FIFO with subsequent pending messages.

5.2.5.   Initiation

In order to communicate properly with SPI device, the protocol on how to communicate must be agreed on. This includes the SPI mode and an idle byte pattern. On power up, the first message to come out of the JF2 is the OK_TO_SEND message. It takes about 100 ms from power up for the SPI drivers to get initialized. The slave has no way of forcing data to the master to indicate it is ready for transmission, but the master can poll the client periodically. Since the specified idle byte pattern is A7B4, the master can transmit this idle pattern into the slave repeatedly. If it receives idle patterns back from the slave, it indicates that the slave currently have nothing to transmit but is ready to communicate.

Note that in some versions of firmware, the JF2 will assert GPIO 3 (currently pin19) high whenever it has data in the transmit FIFO. The host can observe this GPIO line to know when to poll the receiver for data.

5.2.6.   Message Transfer

On the receive side, the host is expected to transmit idle pattern when it is querying the transmit buffer, unless it has commands for the JF2. In this way, the volume of discarded bytes is kept nearly as low as in the UART application because the hardware does not place most idle pattern bytes in the RX FIFO. Most messaging can be serviced with polling. The FIFO threshold can be placed to detect large messages requiring interrupt-driven servicing.

On the transmit side, the intent is to fill the FIFO only when it is disabled and empty. In this condition, the driver software loads as many queued-up messages as can completely fit in the FIFO, then the FIFO is enabled. The host is required to poll messages until it receivers idle pattern bytes. At this point the FIFO is empty and disabled, allowing the driver to again respond to an empty FIFO interrupt and load the FIFO with messages, if any are queued in buffers.

Note that JF2 may lose or garble serial messages if host does not poll often enough to fetch all messages. System design assumes unrestricted outflow of serial messages.

An optional feature in the JF2 allows a predefined GPIO to be used as a "message waiting" indicator to the host. The message waiting indicator is set high by firmware whenever messages are queued to the transmit FIFO and it goes low when there are no bytes left in the FIFO. The "message waiting" indicator is unaffected by idle byte pattern.

5.2.7.   Error Recovery

All channel recovery, message sequencing, and integrity checks are the responsibility of the SPI master.

5.2.8.   SPI Clock

Daisy chain or "cascaded" mode is not supported.

5.2.9.   Messages

For information on message protocols, rates and timing, refer to the UART section above.

5.2.10.   Internal Details

The following internal operation details are provided for information only:

- **TX and RX each have independent 1024 byte FIFO buffers**

- **RX and TX have independent, software-specified two byte idle patterns**

- **TX FIFO is disabled when empty and transmits its idle pattern until re-enabled**

- **RX FIFO detects a software specified number of idle pattern repeats and then disables FIFO input until the idle pattern is broken**

- **FIFO buffers can generate an interrupt at any fill level**

- **SPI detects synchronization errors and can be reset by software**

5.2.11.   Cautions

When the interface is set for SPI mode, the internal framing logic is powered in hibernate mode. Accidental toggling of the SPI clock line while nCS_SPI is enabled will step the framing register requiring software recovery on the host to get back into frame synch

When switching the JF2 to hibernate mode using orderly shutdown with an ON_OFF pulse or by OSP/NMEA command message, the JF2 will continue to run until the SPI transmit/output buffers are emptied.

At slow serial port speeds with a high volume of data, time-to-turn-off may be up to one second.

If host flow stops polling or turns off the SPI clock before the SPI FIFO is empty and idle patterns are sent from JF2 to host, the JF2 will never turn off.

5.3.   Behavior

At startup, the JF2 is in NMEA protocol. Expect the JF2 to output an "OkToSend" message, with a value of "1", to the host when it is alive and in full-power. The master is supplying the clock and can send data bi-directionally. When there is nothing to send, idle bytes are sent out. Figure 2 displays an example behavior of a host with the JF2 at startup.

FIGURE 2 HOST COMMUNICATION WITH JF2

In Figure 2, "a7 b4" is the Idle pattern (no data available to send), and "00 00" or "ff ff" are the null data message. The highlighted portion in Figure 2 is the NMEA message ID 150: OkToSend. Table 8 shows the OkToSend message format.

	Example	Description
Message ID	$PSRF150	PSRF150 protocol header
OkToSend	1	1 = OK to send, 0 = not OK to send
Checksum	*3F	
<CR><LF>		End of message termination

TABLE 8 MID150 OKTOSEND

The highlighted portion of Figure 2 is "24 50 53 52 46 31 35 30 2c 31 2a 33 45 0d 0a". It is decoded as follows:
24 is hex for ASCII $

50 = P

53 = S

52 = R

46 = F

31 = 1

35 = 5

30 = 0

2c = ,

31 = 1

2a = *

33 = 3

45 = E

0d = <CR>

0a = <LF>

Another example of a message is shown in Figure 3.

FIGURE 3 $GPGGA MESSAGE

Part of the NMEA message is "24 47 50 47 47 41 2c 32 33 35 39" This can be decoded as:

24 = $

47 = G

50 = P

47 = G

47 = G

41 = A

2c = ,

32 = 2

33 = 3

35 = 5

39 = 9

.. and so forth.

6. I^{2}C

This section describes how to configure the serial port for I2C mode.

	JF2 Pin	Pin Definition
TXA	10	I^{2}C CLOCK
RXA	11	I^{2}C DATA
GPIO6	23	No connect
GPIO7	24	Pull DOWN with 10kΩ

TABLE 9 I^{2}C PIN DEFINITIONS

Electrical Interface: CMOS at 1.8 V:

- While Data and Clock are 3.3 V compatible, if external pull ups are from a source higher than 1.8 V, then small amounts of current may flow from the 3.3 V source, through the external pull ups, and through the internal pull-ups to the 1.8 V line.
- All device drivers are specified as open drain with external pull-up to allow collision detection and contention resolution.

6.1. Description

JF2	In/Out	Pull	Name	Description, Voltage, Notes
10	BiDir	High*	*I^{2}C_CLK*	Host SPI serial Output, 1.8 V
11	BiDir	High*	*I^{2}C_DIO*	Host SPI serial Input, 1.8 V

TABLE 10 I^{2}C PINOUTS

* Note, for proper operation, external pull-ups are required to ensure proper rise times with stray shunt capacitances from attached loads and traces. These must be pulled up to 1.8V-3.6V supply. The typical resistor value is between 1KΩ and 2.2KΩ.
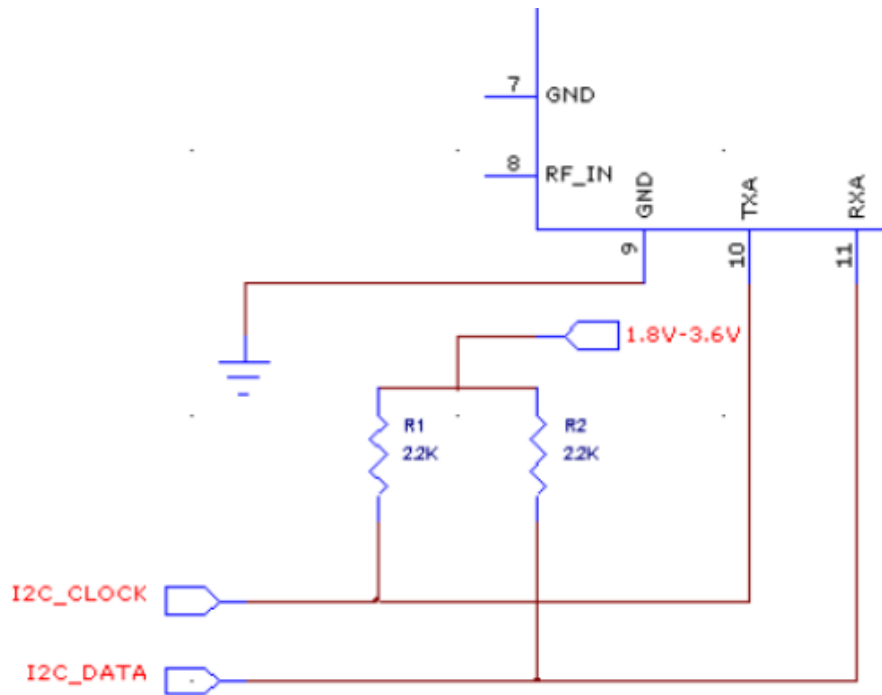
FIGURE 4 REQUIRED PULL-UPS ON I2C

6.2.　　Run-time Operation

The JF2 supports two-wire I^{2}C operation in multi-master mode only, with behavior comparable to UART operation. Refer to industry documents on I^{2}C interfaces and operation.

6.2.1.　Multi-Master Mode:

Multi-master mode requires that the hardware detect and arbitrate between collisions for master status and data direction. Master or slave mode is determined from clock contention: whichever device is generating the clock is master, and all other devices on the bus are slave. In the event of contention time-out, the master device must take control of error detection and retries.   If a device has data to send, it waits for the bus to idle, then asserts itself as master and sends the data.

Thus in a typical application the JF2 periodically asserts itself as bus master and sends messages to the Host. If the Host wants to send a command to JF2, it must assert itself as master when the I2C bus becomes idle and then send the command. If there is a response to the command, the JF2 becomes master again and sends the response.

If both the JF2 and the Host try to assert bus mastership at the same time, the JF2 implements the contention resolution mechanism specified by the I2C standard.

6.2.2.   I^{2}C Addresses

Address format is 7-bit. I^{2}C supports multiple masters and multiple slaves. When the JF2 is the master, it addresses the Host CPU by issuing the address 0x62. When the Host is master and JF2 is slave, the Host addresses the JF2 by issuing the address 0x60. Note that the JF2's I^{2}C master and slave addresses can be changed under firmware control using an OSP input message (MID 178, SID 2).

6.2.3.   Frame Format

I^{2}C-standard 8-bit octets (bytes) are used. Bit order is MSB transmitted first, with the first byte of a transfer containing the 7-bit address and direction bit as per the standard. The direction bit is set to '0' indicating write or send in all transfers involving the JF2. There is no specified maximum limit of bytes per transfer.

6.2.4.   Data Rates

The supported bit clock rates are 100 kbps (standard mode) and 400 kbps (DEFAULT - fast mode). High speed mode is not supported. The data rate can be changed using an OSP input message (MID 178, SID 2).

6.2.5.   Internal Details

The following internal operation details are provided for information only:

Internal FIFOs for RX and TX are 64 bytes.

Bus contention timeout is set to 30 ms and is not changeable

6.2.6.   Messages

For message protocols and timing, refer to the UART section above.

With regard to message rates, the maximum amount of I^{2}C data handling capacity between sender and receiver must be de-rated by protocol overheads and collision density and backoff/retry timing. Refer to the UART section above for other considerations.

6.2.7.   Cautions

Note that JF2 may lose or garble serial messages if contention with other bus masters makes it unable to send all messages. System design assumes unrestricted outflow of serial messages.

When switching the JF2 to hibernate mode using orderly shutdown with ON_OFF pulse or by OSP/NMEA command message, the JF2 will continue to run until the I^{2}C transmit/output buffers are emptied.

At slow I^{2}C serial port speeds with a high volume of data, time-to-turn-off may be up to one second with no throttling from contention.

If multi-master mode contention on the I^{2}C bus prevents JF2 output, the JF2 will take longer to turn off. If the I^{2}C bus is inadvertently seized (another device hold clocks or data line low and never releases) the JF2 will not turn off.

7.　　Document History

Revision	Date	Changes
0	2012-05-01	First issue
1	2012-07-19	Section reformatting, I2C corrections
2	2012-10-31	• Completed Introduction • Updated I2C chapter to reflect only multi-master mode support • Grammatical and formatting corrections for clarity