

## 1VV0301090 Rev.2 – 2013-10-07



## **APPLICABILITY TABLE**

PRODUCT
SE868 V2



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# 1. Introduction

## 1.1. Scope

The SE868-V2 is an 11mm by 11mm integrated GNSS receiver module using SiRFstar V technology. This document expands upon the data sheet(s) to highlight particular areas to allow the hardware engineer to achieve a successful design implementation.

## 1.2. Audience

This document is intended for helping customer in the integration of the Telit SE868 GNSS module.

## 1.3. Contact Information, Support

For general contact, technical support, to report documentation errors and to order manuals, contact Telit Technical Support Center (TTSC) at:

[TS-EMEA@telit.com](mailto:TS-EMEA@telit.com)  
[TS-NORTHAMERICA@telit.com](mailto:TS-NORTHAMERICA@telit.com)  
[TS-LATINAMERICA@telit.com](mailto:TS-LATINAMERICA@telit.com)  
[TS-APAC@telit.com](mailto:TS-APAC@telit.com)

Alternatively, use:

<http://www.telit.com/en/products/technical-support-center/contact.php>

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

<http://www.telit.com>

To register for product news and announcements or for product questions contact Telit Technical Support Center (TTSC).

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.





## 1.4. Document Organization

This document contains the following chapters (sample):

[“Chapter 1: “Introduction”](#) provides a scope for this document, target audience, contact and support information, and text conventions.

[“Chapter 2: “Powering the SE868-V2”](#) gives an overview about power supply.

[“Chapter 3: “Example Implementation”](#) describes the Startup and shutdown

[“Chapter 4: “SE868-V2 ROM features”](#) describes the new ROM features code to ROM version.

[“Chapter 5: “Updating Patch Code”](#) describes updating patch code in SPI Flash

[“Chapter 6: “Main serial interface”](#) describes the serial interfaces.

[“Chapter 7: “RF Front End Design”](#) describes in details the characteristics of the Front end.

[“Chapter 8: “Reference Design”](#) gives an overview about the reference design.

[“Chapter 9: “Firmware configuration”](#) describes the configuration settings.

[“Chapter10:“Operating Conditions and Electrical Specifications”](#) describes electrical Specifications

[“Chapter 11: “Handling and soldering”](#) describes packaging and soldering of the module.

[“Chapter 12: “PCB layout details”](#) describes the mechanical design of the module.

[“Chapter 12: “Document History”](#) describes the history of the present product.

## 1.5. Text Conventions



**Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.**



**Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.**



**Tip or Information – Provides advice and suggestions that may be useful when integrating the module.**

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.



## 1.6. Related Documents

- SE868-V2 Product Description,
- SE868-V2 EVK User Guide,

## 1.7. Upgrading JF2 designs to the SE868-V2

The SE868-V2 is a PIN for PIN compatible replacement or upgrade to the JF2 ROM module. However it is NOT design compatible. A SE868-V2 cannot be dropped into a JF2 design and operate properly. Listed below are differences between the JF2 and the SE868-V2 and the necessary external changes. There are other variations between the products that also prevent them from being drop in replacements, such as variations in software that are not discussed here. Consult Telit support for more information

- The JF2 flash variant used the BOOT pin to program the device. The Boot pin will be a no connect on the SE868-V2 module the same as the JF2 ROM variant.
- The SE868-V2 does not support EEPROM. It uses an internal SPI flash. The Baud rate and protocol will be NEMA 4800 on initial boot and any subsequent ON-OFF cycles unless a software patch is loaded in the Serial SPI Flash.
- The SE868 V2 does not support DRI2C or MEMs devices because the DRI2C port is now used by the internal SPI flash. For this reason, the GPIO0, GPIO1, GPIO3 and GPIO4 lines must not be connected in customer applications, otherwise operation with the SPI flash can fail. The current JF2 EVK will not work properly with an SE868-V2 module unless hardware changes are made. The JF2 antenna detect circuitry uses GPIO2 and GPIO3. The SE868-V2 uses GPIO3 for the internal SPI flash.
- For the SE868-V2 the change in level on GPIO8 no longer affects the functionality of the ON-OFF signal as it did on JF2 modules. The GPIO8 pin is now used for external antenna use select. GPIO8 is read at power up to determine whether the SE868-V2 is to be placed in high gain or low gain mode. Pull low for low gain mode, leave floating or pulled high for high gain mode. Typically pull low if an external LNA or active patch antenna used.
- The SE868 V2 adds a new power pin. For compatibility to the JF2 flash and ROM variants a zero ohm jumper has been added internally so this pin will not need to be powered. However, we recommend it be connected to 1.8V. The previous JF2 variants had this pin as a no-connect. If the customer grounded this pin in their design, it will short the 1.8 volt supply directly to ground.
- The SE868-V2 is a complete GNSS receiver that is capable of using Satellites from the GLONASS constellation. The JF2 module only used



GPS signal with a center frequency of 1575.42 MHz. GLONASS frequency range is approximately 1598-1607 MHz. Appropriate design consideration should be taken when selecting the Antenna and any external LNA.



## 2. Powering the SE868-V2

### 2.1. 1.8V Supply Voltage

Unlike older GNSS receiver modules, the SE868-V2 requires a single always on supply voltage of 1.8 volts. Rather than having a “split” power supply design of main and backup, the SE868-V2 manages all of its power modes internally. The SE868-V2 will normally power up into the lowest power “hibernate” state upon initial application of power. Upon pulsing the ON-OFF signal, the SE868-V2 will transition to the “operate” state. Pulsing the ON-OFF signal a second time will transition the SE868-V2 back into the “hibernate” state.

The current power state of the SE868-V2 can be determined by monitoring the “SYSTEM-ON” signal. A logic low indicates the module is in “hibernate”, whereas logic high indicates the module is in “operate” state.

If the 1.8 volt DC supply is removed from the SE868-V2 (regardless of power state) it will lose current RTC time and will lose the contents of the internal SRAM. To prevent improper startup, once power is removed, keep the power removed for approximately 10 seconds so the internal SRAM contents can clear reliably.

The SE868-V2 monitors the 1.8 volt supply and issues an internal hardware reset if the supply drops below 1.7 volts. This reset protects the memory from accidental writes during a power down condition. The reset forces the SE868-V2 into a low power stand-by state.

To prevent the reset the 1.8 volt supply must be regulated to be within  $\pm 50$  mV of nominal voltage inclusive of load regulation and power supply noise and ripple. Noise and ripple outside of these limits can affect GNSS sensitivity and also risk tripping the internal voltage supervisors, thereby shutting down the SE868-V2 unexpectedly. Regulators with very good load regulation are strongly recommended along with adequate power supply filtering to prevent power supply glitches as the SE868-V2 transitions between power states.

The power supply voltage, noise and ripple must be between 1.75V and 1.85V for all frequencies. To help meet these requirements, a separate LDO for the SE868-V2 is suggested.

### 2.2. Capacitance

Aluminum electrolytic capacitors are not recommended at the input to the SE868-V2 due to their high ESR. Tantalum capacitors are recommended with a minimum value of 10uF in parallel with a 0.1uF ceramic capacitor. Ceramic capacitors alone can be used, but make sure the LDO is stable with such capacitors tied to the output.



## 2.3. Implementing Pseudo Battery Back-up

As mentioned above, the SE868-V2 cannot tolerate removal of the 1.8 volt supply without losing RTC time and SRAM data. The main supply voltage can be switched to a backup supply external to the SE868-V2 provided the receiver is allowed time to enter the hibernate state. This can be accomplished by monitoring the status of the SYSTEM-ON line, which will be low whenever the SE868-V2 is in the hibernate state. At this point, the main supply can be safely switched over to the backup supply provided the 1.8 volt supply stays within specification. Similarly, the switch back to the main supply must occur prior to placing the SE868-V2 into full power mode.

If the product containing the SE868-V2 needs to support abrupt removal of power, then the module will require a cold start reset upon reapplication of power.

## 2.4. Understanding ON-OFF and SYSTEM-ON

ON-OFF: Input control

SYSTEM-ON: Output indicator

The SE868-V2 power is controlled by a state machine. This state machine is clocked by the internal 32 KHz RTC clock, and is controlled by internal signals as well as the ON-OFF and NRESET signals. The SYSTEM-ON signal reflects the power state of the SE868-V2: logic low for hibernate mode, and logic high for full power mode.

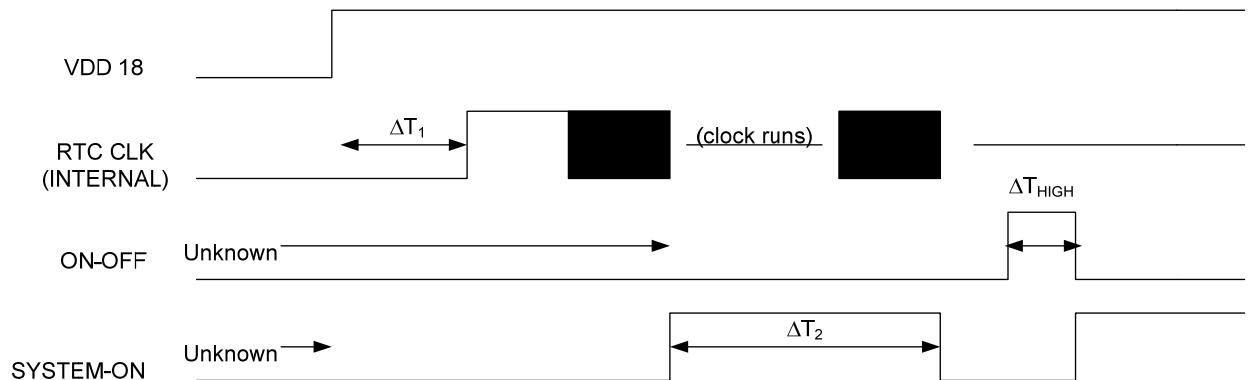
When power is first applied to the SE868-V2, the internal RTC must start up before the state machine can begin operating. ON-OFF signals applied before the state machine is ready for them will be ignored. The SE868-V2 signals the readiness to accept ON-OFF signals by outputting a pulse on the SYSTEM-ON line after power is first applied. This pulse is only output upon application of power, and is not output when the receiver is in hibernate or full power mode.

The ON-OFF signal is normally low. When it transitions high, it should stay high for a time equivalent to a minimum of 3 RTC clock cycles. The signal may then transition low and remain low until the next change in power state is desired.

For self-start operation, the SYSTEM-ON output is connected to the ON-OFF input. The SE868-V2 then goes into full power run state when the supply voltage is first applied. Low power modes trickle-power and micro-power mode will not operate in this condition. The recommended way to shut the receiver down is with a serial command. Pulling power is not recommended without first sending a shutdown command. In order to restart the receiver power will need to be cycled.







**Figure 1 – Initial Application of Main Power**

Timed Parameter	Prior Event/State	Symbol	Min	Typ	Max	Unit
RTC startup time	First power applied	$\Delta T_1$	0	299	1000	ms
FSM Ready pulse	RTC running	$\Delta T_2$		10		$T_{RTC}$
Min ON-OFF high		$\Delta T_{HIGH}$	3			$T_{RTC}$
$T_{RTC}$ is equivalent to one RTC (32.678KHz) clock cycle.						

**Table 1 – Power State Timing**

The host system can determine if the SE868-V2 is “ready” as follows:

- A short pulse on SYSTEM-ON output line indicates to a host that the SE868-V2 is ready and armed to accept an ON-OFF pulse.
- The host can wait a fixed duration. In most cases, the “time-to-ready” interval can be on the order of 300ms. If the system temperature is very low, the RTC startup time may be as long as 5 seconds.
- The host can issue ON-OFF pulses repeatedly every 100ms and monitor for JF-2 SYSTEM-ON output to go HIGH. Note that issuing an ON-OFF pulse once the system is running may cause the firmware to initiate the shutdown process.
- The host can issue ON-OFF repeatedly every one second and wait for serial messages to be output within the one second. Note that issuing an ON-OFF pulse once the system is running may cause the firmware to initiate the shutdown process.



## 2.5. Reset Design Details

The SE868-V2 will generate an internal reset as appropriate. No external reset signal needs to be applied to the SE868-V2.

If an external reset is desired, the signal must be either open collector or open drain without any form of pull up. Do not pull this line high with either a pull up or a driven logic one. When this line is pulled low, the SE868-V2 will immediately drop into hibernate mode with some loss of data.

When the external reset is released, the SE868-V2 will go through its normal power up sequence provided the VCC\_IN supply is within specifications.





### 3. Example Implementations

This section illustrates the implementations that meet the rules for the SE868-V2. Telit recommends assessing the risks when making implementation decisions

#### 3.1. Normal Operation Startup and Shutdown

To start the SE868-V2:

Send a voltage pulse (tolerant to 3.6V) to the ON-OFF input.

To go into the shutdown sequence of the SE868-V2 from full power state :

Send a voltage pulse (tolerant to 3.6V) to the ON-OFF input

Or Issue an NMEA (\$PSRF117) or OSP (MID 205) serial command.



## **4. SE868-V2 ROM Features**

### **4.1. External LNA auto Select**

GPIO 8 is external LNA detect during boot up. If an External LNA is to be used then GPIO8 should be pulled low. When GPIO8 is left floating the internal LNA will be used. The Gain of the external LNA should not exceed the limits detailed in Section 10.1. This is a onetime detect on startup and is not dynamic.

The Tracker Config message (OSP MID178, SID2) can also be used to change the LNA mode, but note that the use of this message is not recommended, because an incorrect parameter could render the SE868-V2 inoperable. Contact Telit technical support if this approach is required in your system.

### **4.2. SPI Flash Support**

The SE868-V2 includes Internal SPI flash providing storage for features such as patches, SGEE, CGEE, broadcast ephemeris data, and data logging. No external SPI or memory connections are required, or supported.



## 5. Updating Patch Code:

The SE868-V2 supports firmware patching. Firmware patches are stored inside the modules the non-volatile SPI FLASH device. At power up, patches are retrieved from SPI FLASH and loaded into patch RAM. Firmware patches are accumulated into patch data files, which in turn are made available with descriptions of their contents and applicability. A patch data file is cumulative in that it includes firmware improvements and enhancements made available in previous patches. It may also include configuration settings that differ from the ROM defaults, as in the default UART baud rate, for example. The desired patch data file must be distributed to the end-user device where it may be accessed by the Host processor.

The Host processor in the end-user device is required to run software that sends patch data from the patch file to the module using OSP Patch Protocol messages over the host serial port. Example source code to assist in the implementation of a patch downloader on the Host processor is available. Note that the module must be operating in full power mode during the patching process. The patch contents are stored in non volatile SPI FLASH memory and loaded into patch RAM on the module, where they remain as long as main power is maintained. This avoids the reloading of patches into patch RAM when the system resumes normal operation from a low power state such as hibernate. At the end of the patching process the module performs an internal reset and restart.



## 6. Main Serial Interface

The SE868-V2 has the capability to operate in serial UART mode, SPI mode or I2C mode depending upon how the SE868-V2 GPIO6 and GPIO7 pins are strapped at power up. Either leave the pin floating, apply a 10K resistor to +1.8V (PU) or apply a 10K resistor to GND (PD).

Mode	GPIO6 (internal pull-down)	GPIO7 (internal pull-up)
UART	PU	Leave floating or PU
I2C	Leave floating or PD	PD
SPI	Leave floating	Leave floating

**Table 2 – Interface Operating Modes**

### 6.1. UART Mode

The GPIO6 pin should be pulled high through a 10K resistor to the 1.8 volt supply. The GPIO7 pin can be left open or pulled to 1.8V. Upon power up, the SE868-V2 will communicate using a standard asynchronous 8 bit protocol with messages appearing on the TX line, and commands and data being entered on the RX line. Note the GPIO6 and GPIO7 lines are read at power up or reset only and are not used afterwards. In particular, no flow control operations are performed.

### 6.2. I2C Mode

The GPIO7 pin should be pulled low through a 10K resistor to GND. The GPIO6 pin can be left open or pulled low. Upon power, the SE868-V2 acts as a master transmitter and a slave receiver. Pull-ups to a 1.8V to 3.6V power supply in the range of 1K to 2.2K are required on the RXA and TXA lines when used in I2C mode. In this mode, the pins are defined below:

Signal Name	I2C Function
RXA	I2C Data (DIO)
TXA	I2C Clock (CLK)

**Table 3 – I2C Pin Assignments**

Bit rates to 400K are achievable. Note the GPIO6 and GPIO7 lines are read at power up or reset only and are not used afterwards.

The operation of the I2C with a master transmit and slave receive mimics a UART operation, where both SE868-V2 and host can independently freely transmit. It is possible to enable the master transmit and slave receive at the same



time, as the I2C bus allows for contention resolution between SE868-V2 and a host vying for the bus.

## 6.3. SPI Mode

If both the GPIO6 and GPIO7 pins are left floating, the SE868-V2 will power up in slave SPI mode, supporting both SPI and Microwire formats. In this mode, the four pins are defined below:

Signal Name	SPI Function
GPIO7	SPI Chip Select (CS#)
GPIO6	SPI Clock (CLK)
RXA	SPI Data In (MOSI)
TXA	SPI Data Out (MISO)

**Table 4 – SPI Mode Pin Assignments**

---

**NOTE:**

Data rates of 6.8 MHz are achievable.

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## 7. RF Front End Design

The SE868-V2 contains an integrated LNA and pre-select SAW filter. This allows the SE868-V2 to work well with a passive GNSS antenna. If the antenna cannot be located near the SE868-V2, then an active antenna (that is, an antenna with a low noise amplifier built in) can be used. The following items will be discussed in turn to assist in designing the “RF front end”.

1. RF signal requirements
2. GNSS antenna polarization
3. GNSS antenna gain
4. System noise floor
5. Active versus passive antenna
6. RF trace losses
7. Implications of the pre-select SAW filter
8. External LNA gain and Noise Figure
9. Powering the external LNA (active antenna)
10. RF interference
11. Shielding

### 7.1. RF Signal Requirements

The SE868-V2 can achieve Cold Start acquisition with a signal level of -146 dBm at its input. This means the SE868-V2 can find the necessary satellites, download the necessary ephemeris data and compute the location within a 2 minute period. In the GNSS signal acquisition process, downloading and decoding the data is the most difficult task, which is why Cold Start acquisition requires a higher signal level than navigation or tracking signal levels. For the purposes of this discussion, autonomous operation is assumed, which makes the Cold Start acquisition level the important design constraint. If assistance data in the form of time or ephemeris aiding is available, then even lower signal levels can be used to compute a navigation solution.

The GPS signal is defined by IS-GPS-200E. This document states that the signal level received by a linearly polarized antenna having 3 dBi gain will be a minimum of -130 dBm when the antenna is in the worst orientation and the satellite is 5 degrees or more above the horizon.

GLONASS signal is defined by GLONASS ICD 2002 Version 5.1. This document states the power level of the received RF signal from GLONASS satellite at the output of a 3dBi linearly polarized antenna is not less than -161 dBW (-131dBm) for L1 sub-band provided that the satellite is observed at an angle 5 degrees or more above the horizon.

In actual practice, the GPS satellites are outputting slightly more power than specified by IS-GPS-200E, and the signal level typically goes higher as the satellites have higher elevation angles.





The SE868-V2 will display a reported C/No 40 dB-Hz with a GPS signal level of -130 dBm into the RF input. This assumes a SEN (system equivalent noise) of the receiver of 4dB. System Equivalent Noise includes the Noise Figure of the receiver plus signal processing or digital noise. For an equivalent GLONASS signal level the GLONASS signal will report a C/No approximately 39 dB-Hz. This is due to the receiver's higher losses (NF) for GLONASS signals and a higher signal processing noise for GLONASS signals.

Each GNSS satellite presents its own signal to the SE868-V2, and best performance is obtained when the signal levels are between -125 dBm and -117 dBm. These received signal levels are determined by

- GPS/GLONASS satellite transmit power
- GPS/GLONASS satellite elevation and azimuth
- Free space path loss
- Extraneous path loss such as rain
- Partial or total path blockage such as foliage or building
- Multipath caused by signal reflection
- GNSS antenna
- Signal path after the GNSS antenna

The first three items in the list above are specified in IS-GPS-200E, online while the GLONASS signal is defined by GLONASS ICD 2002 Version 5.1 readily available from multiple sources

IS-GPS-200E specifies a signal level minimum of -130 dBm will be presented to the receiver when using a linearly polarized antenna with 3 dBi gain.

GLONASS ICD 2002 Version 5 states the the power level of the received RF signal from GLONASS satellite at the output of a 3dBi linearly polarized antenna is not less than -161 dBW for L1 sub-band provided that the satellite is observed at an angle of 5 or more

The GNSS signal is relatively immune to rainfall attenuation and does not really need to be considered.

However, the GNSS signal is heavily influence by attenuation due to foliage, such as tree canopies, etc. as well as outright blockage caused by building, terrain or other items in the line of sight to the specific GNSS satellite. This variable attenuation is highly dependent upon GNSS satellite location. If enough satellites are blocked, say at a lower elevation, or all in a general direction, the geometry of the remaining satellites will result is a lower accuracy of position. The SE868-V2 reports this geometry in the form of PDOP, HDOP and VDOP.

For example, in a vehicular application, the GNSS antenna may be placed embedded into the dashboard or rear package tray of an automobile. The metal roof of the vehicle will cause significant blockage, plus any thermal coating applied to the vehicle glass can attenuate the GNSS signal by as much as 15 dB. Again, both of these factors will affect the performance of the receiver.





Multipath is a phenomena where the signal from a particular satellite is reflected and is received by the GNSS antenna in addition to or in place of the original line of sight signal. The multipath signal has a path length that is longer than the original line of sight path and can either attenuate the original signal, or if received in place of the original signal add additional error is determining a solution because the distance to the particular GNSS satellite is actually longer than expected. It is this phenomena that makes GNSS navigation in urban canyons (narrow roads surround by high rise buildings) so challenging. In general, the reflecting of the GNSS signal causes the polarization to reverse. The implications of this are covered in the next section.

## 7.2. GNSS Antenna Polarization

The GNSS (GPS and GLONASS) signals are broadcast as right hand circularly polarized signal. The best antenna to receive the GNSS signal is a right hand circularly (RHCP) polarized antenna. Remember that IS-GPS-200E and GLONASS ICD 2002 Version 5 specifies the receive power level with a linearly polarized antenna. A linearly polarized antenna will have 3 dB loss as compared to an RHCP antenna assuming the same antenna gain (specified in dBi and dBic respectively).

An RHCP antenna is better at rejecting multipath than a linearly polarized antenna. This is because the reflected signal changes polarization to LHCP, which would be rejected by the RHCP antenna by typically 20 dB or so. If the multipath signal is attenuating the line of sight signal, then the RHCP antenna would show a higher signal level than a linearly polarized antenna because the interfering signal is rejected.

However, in the case where the multipath signal is replacing the line of sight signal, such as in an urban canyon environment, then the number of satellites in view could drop below that needed to determine a 3D solution. This is a case where a bad signal may be better than no signal. The system designer needs to make tradeoffs in their application to determine what the better choice is.

## 7.3. GNSS Antenna Gain

Antenna gain is defined as the extra signal power from the antenna as compared to a theoretical isotropic antenna (equally sensitive in all directions).

For example, a 25mm by 25mm square patch antenna on a reference ground plane (usually 70mm by 70mm) will give an antenna gain at zenith of 5 dBic. A smaller 18mm by 18mm square patch on a reference ground plane (usually 50mm by 50mm) will give an antenna gain at zenith of 2 dBic.

While an antenna vendor will specify a nominal antenna gain (usually at zenith, or directly overhead) they should supply antenna pattern curves specifying gain as a function of elevation, and gain at a fixed elevation as a function of azimuth. Pay careful attention to the requirement to meet these specifications, such as



ground plane required and any external matching components. Failure to follow these requirements could result in very poor antenna performance.

It is important to note that GNSS antenna gain is not the same thing as external LNA gain. Most antenna vendors will specify these numbers separately, but some combine them into a single number. It is important to know both numbers when designing and evaluating the front end of a GNSS receiver.

For example, antenna X has an antenna gain of 5 dBiC at azimuth and an LNA gain of 20 dB for a combined total of 25 dB. Antenna Y has an antenna gain of -5 dBiC at azimuth and an LNA gain of 30 dB for a combined total of 25 dB. However, in the system, antenna X will outperform antenna Y by about 10 dB (refer to Section 9.4 for more details on system noise floor).

An antenna with higher gain will generally outperform an antenna with lower gain. Once the signals are above about -130 dBm for a particular satellite, no improvement in performance would be gained. However, for those satellites that are below approximately -125 dBm, a higher gain antenna would improve the gain and improve the performance of the GNSS receiver. In the case of really weak signals, a good antenna could mean the difference between being able to use a particular satellite signal or not.

## 7.4. System Noise Floor

As mentioned earlier the SE868-V2 will display a reported C/No of 40 dB-Hz with a GPS input signal level of -130 dBm and 39dB-Hz for GLONASS signals. The C/No number means the carrier (or signal) is 40 dB greater than the noise floor measured in a one Hz bandwidth. This is a standard method of measuring GPS receiver performance.

Thermal noise is -174 dBm/Hz at an approximate room temperature. From this we can compute a system noise figure of 4 dB for the SE868-V2. This noise figure consists of the loss of the pre-select SAW filter, the noise figure of the LNA as well as implementation losses within the digital signal processing unit.

If a good quality external LNA is used with the SE868-V2, then the noise figure of that LNA (typically better than 1dB) could reduce the overall system noise figure of the SE868-V2 from 4 dB to around 2-3 dB. Some of the factors in the system noise figure are implementation losses due to quantization and other factors and don't scale with improved front end noise figure.

## 7.5. Active versus Passive Antenna

If the GNSS antenna is placed near the SE868-V2 and the RF traces losses are not excessive (nominally 1 dB), then a passive antenna can be used. This would normally be the lowest cost option and most of the time the simplest to use. However, if the antenna needs to be located away from the SE868-V2 then an active antenna may be required to obtain the best system performance. The active antenna has its own built in low noise amplifier to overcome RF trace or cable losses after the active antenna.



However, an active antenna has a low noise amplifier (LNA) with associated gain and noise figure. In addition, many active antenna have either a pre-select filter, a post-select filter or both.

## 7.6. RF Trace Losses

RF Trace losses are difficult to estimate on a PCB without having the appropriate tables or RF simulation software to estimate what the losses would be. A good rule of thumb would be to keep the RF traces as short as possible, make sure they are 50 ohms impedance and don't contain any sharp bends.

## 7.7. Implications of the Pre-select SAW Filter

The SE868-V2 module contains a SAW filter used in a pre-select configuration with the built in LNA. The RF input of the SE868-V2 ties directly into the SAW filter. Any circuit connected to the input of the SE868-V2 would see complex impedance presented by the SAW filter, particularly out of band, rather than the relatively broad and flat return loss presented by the LNA. Filter devices pass the desired in band signal to the output, resulting in low reflected energy (good return loss), and reject the out of band signal by reflecting it back to the input, resulting in high reflected energy (bad return loss).

If an external amplifier is to be used with the SE868-V2, the overall design should be checked for RF stability to prevent the external amplifier from oscillating. Amplifiers that are unconditionally stable at the output will be fine to use with the SE868-V2.

If an external filter is to be connected directly to the SE868-V2, care needs to be used in making sure neither the external filter nor the internal SAW filter performance is compromised. These components are typically specified to operate into 50 ohms impedance, which is generally true in band, but would not be true out of band. If there is extra gain associated with the external filter, then a 6 dB Pi or T resistive attenuator is suggested to improve the impedance match between the two components.

## 7.8. External LNA Gain and Noise Figure

The SE868-V2 can be used with an external LNA such as what might be found in an active antenna. GPIO 8 is used as for external LNA detect during boot up. If an External LNA is to be used then GPIO8 should be pulled low. When GPIO8 is left floating or pulled high the internal LNA will be used. This is a onetime detect on startup and is not dynamic.

If GPIO8 is left floating or pulled high the external gain (including signal losses past the external LNA) should not exceed 12 dB. Levels higher than that can affect the jamming detection capability of the SE868-V2. If a higher gain LNA is used, either a resistive Pi or T attenuator can be inserted after the LNA to bring the gain down to 12 dB or the SE868-V2 can be switched into a low gain mode by issuing an OSP command to do so.



The external LNA should have a noise figure better than 1 dB. This will give an overall system noise figure of around 2 dB assuming the LNA gain is 14 dB. If higher the low gain mode is selected within the SE868-V2.

The external LNA, if having no pre-select filter, needs to be able to handle signals other than the GNSS signal. These signals are typically at much higher levels. The amplifier needs to stay in the linear region when presented with these other signals. Again, the system designer needs to determine all of the unintended signals and their possible levels that can be presented and make sure the external LNA will not be driven into compression. If this were to happen, the GNSS signal itself would start to be attenuated and the GNSS performance would suffer.

## 7.9. Powering the External LNA (active antenna)

The external LNA needs a source of power. Many of the active antennas accept a 3 volt or 5 volt DC voltage that is impressed upon the RF signal line. This voltage is not supplied by the SE868-V2, but can be easily supplied by the host design. Two approaches can be used. The first is to use an inductor to tie directly to the RF trace. This inductor should be at self resonance at L1 (1.57542 GHz) and should have good Q for low loss. The higher the inductor Q the lower the loss will be. The side of the inductor connecting to the antenna supply voltage should be bypassed to ground with a good quality RF capacitor, again operating at self resonance at the L1 frequency.

The second approach is to use a quarter wave stub in place of the inductor. The length of the stub is designed to be exactly a quarter wavelength, which has the effect of making an RF short at L1 at one end of the stub to appear as an RF open. The RF short is created by the good quality RF capacitor operating at self resonance.

The choice between the two would be determined by:

- RF path loss introduced by either the inductor or quarter wave stub.
  - Cost of the inductor.
  - Space availability for the quarter wave stub.
- Simulations done by Telit show the following:
- Murata LQG15HS27NJ02 Inductor 0.65 dB of additional signal loss
  - Quarter wave stub on FR4 0.59 dB of additional signal loss
  - Coilcraft B09TJLC Inductor (used in ref. design) 0.37 dB of additional signal loss

This additional loss occurs after the LNA so it is generally not significant unless the circuit is being designed to work with either an active or a passive antenna.

## 7.10. RF Interference

RF Interference into the GNSS receiver tends to be the biggest problem when determining why the system performance is not meeting expectations. As



mentioned earlier, the GPS signals are at -130 dBm and lower. If signal higher than this are presented to the receiver it can be overwhelmed. The SE868-V2 can reject up to 8 CW in-band jamming signals, but would still be affected by non-CW signals.

The most common source of interference is digital noise. This is created by the fast rise and fall times and high clock speeds of modern digital circuitry. For example, a popular netbook computer uses an Atom processor clocked at 1.6 GHz. This is only 25 MHz away from the GPS signal, and depending upon temperature of the SAW filter, can be within the passband of the GNSS receiver. Because of the nature of the address and data lines, this would be broadband digital noise at a relatively high level. Such devices are required to adhere to a regulatory standard for emissions such as FCC Part 15 Subpart J Class B or CISPR 22. However, these regulatory emission levels are far higher than the GNSS signals.

## 7.11. Shielding

Shielding the RF circuitry generally is ineffective because the interference is getting into the GNSS antenna itself, the most sensitive portion of the RF path. The antenna cannot be shielded because then it can't receive the GNSS signals.

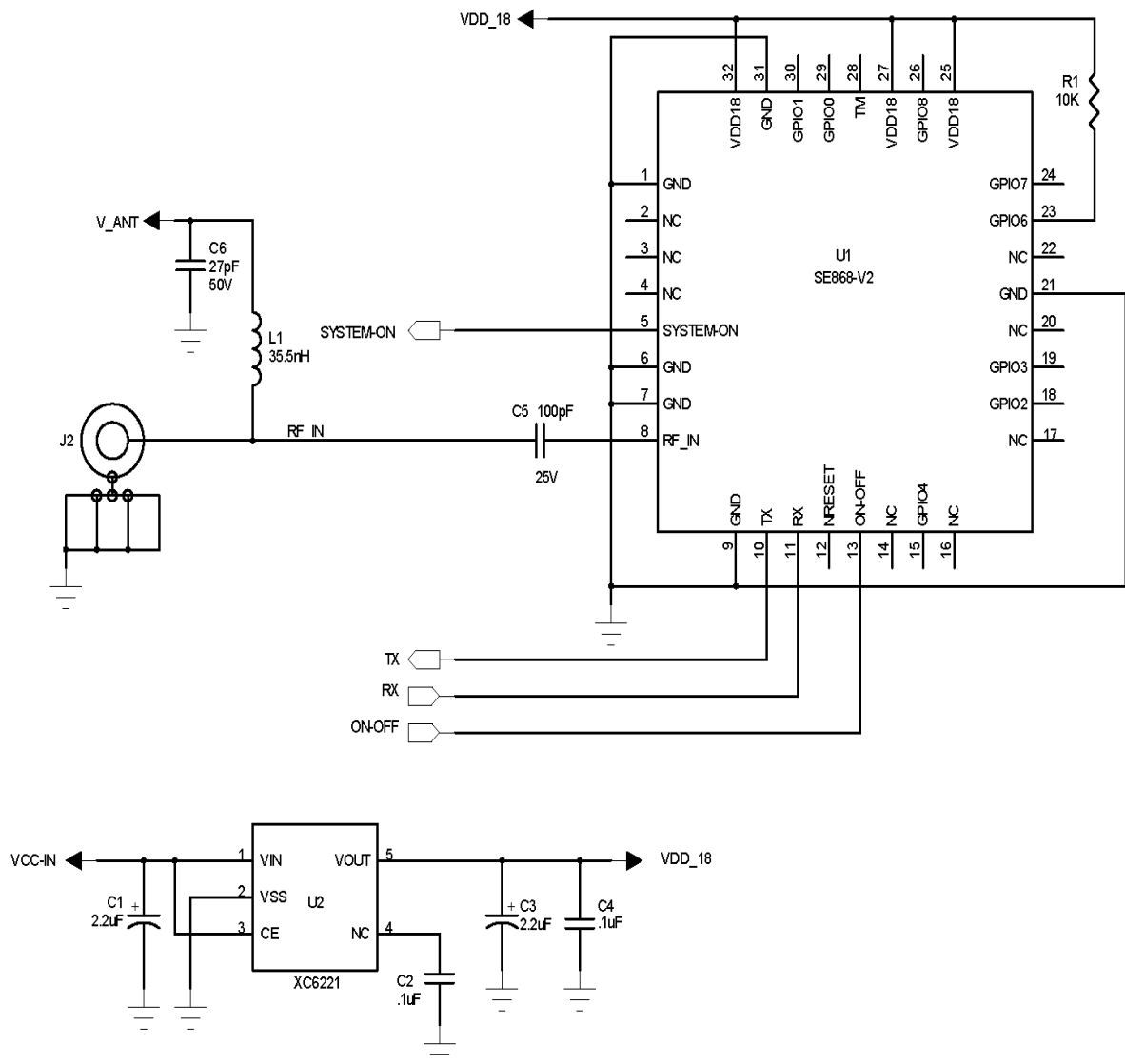
There are two solutions, one is to move the antenna away from the source of interference or the second is to shield the digital interference to prevent it from getting to the antenna.





## 8. Reference Design

The SE868-V2 Reference Design is presented in the figure below.



**Figure 2 – SE868-V2 Reference Design – Active Antenna**

Along with power and ground, the minimum number of signals required to operate the SE868-V2 properly are four digital signals and one RF signal. The RF input can be connected directly to a GNSS antenna. The reference design shows a DC power feed for an active antenna. C5 is used to block the DC voltage from entering the SE868-V2. The inductor L1 is chosen to be self resonant at the GPS frequency, 1.57542 GHz, to minimize loading on the RF trace. Capacitor C6 is chosen to be self resonant at the GPS frequency such that



is looks pretty close to an RF short at that frequency. V\_ANT is the supply voltage for the external active antenna.

TX is the normal digital output and as configured in the reference design, is a serial UART with a default bit rate of 4800 bps, 1 stop bit and 8 data bits. This is a 1.8 volt logic level signal. As is the case with all serial data, the idle state is logic one.

RX is the normal digital input and as configured in the reference design, is a serial UART with a default bit rate of 4800 bps, 1 stop bit and 8 data bits. This is a 1.8 volt logic level signal, but is tolerant to 3.6 volts. As is the case with all serial data, the idle state is logic one. Be careful to tri-state this line if the SE868-V2 is turned off to avoid back-driving the SE868-V2.

SYSTEM-ON is an output indicating the power state of the SE868-V2. If the module is in Hibernate mode the logic level will be zero, and if powered up and running, the logic level will be one. SYSTEM-ON can also be used to control an external LNA. It is HIGH when the receiver is running and needs the LNA turned ON, and LOW when the LNA can be turned off. This is a 1.8 volt logic level.

ON-OFF is an input to control the power state of the SE868-V2. Upon first applying power, the SE868-V2 enters the hibernate state with SYSTEM-ON low. After power is applied a brief pulse from SYSTEM-ON output will indicate the SE868-V2 is ready to accept an ON-OFF pulse. Then ON-OFF can be pulsed high for minimum of 100 microseconds to change the power state. SYSTEM-ON will then go to a logic one.

Resistor R1 as shown pulls GPIO6 high, which determines the input/output configuration of the SE868-V2 to be serial UART I/O.

The power supply shown is a minimal design for the SE868-V2 power requirements. The power supply must have tight voltage regulation under varying line and load conditions to prevent falsely tripping the internal voltage supervisor within the SE868-V2.





## 9. Firmware Configuration

The SE868-V2 can be configured by means of firmware in order to fit better into the overall system. This section describes certain aspects of the receiver that can be configured.

### 9.1. Internal LNA

The SE868-V2 offers two modes of operation, high gain mode and low gain mode, for the internal LNA. The high gain mode is the default mode and provides 16 to 20dB of gain. The low gain mode provides 6 to 10dB of gain.

The SE868-V2 can be used with an external LNA such as what might be found in an active antenna. GPIO 8 is external LNA detect during boot up. If an External LNA is to be used then GPIO8 should be pulled low. When GPIO8 is left floating the internal LNA will be used. This is a onetime detect on startup and is not dynamic.

In general, the high gain mode is intended for use with passive antennas, while the low gain mode is used when there is an external LNA as part of the RF front end (e.g. active antenna). The recommended external LNA gain is 20dB.

The Tracker Config message (OSP MID178, SID2) can also be used to change the LNA mode, but note that the use of this message is not recommended, because an incorrect parameter could render the SE868-V2 inoperable. Contact Telit technical support if this approach is required in your system.

### 9.2. Low Power Modes

The SE868-V2 module can be operated in one of four power management modes; Full Power, TricklePower™, Push-To-Fix™, and Micro Power. The latter three of these modes offer progressively lower power consumption profiles. Depending upon the requirements of the system design regarding frequency of position updates and availability of GNSS signals in the operational environment, the designer can choose a mode that provides the best trade-off of performance versus power consumption.

Each of the power management modes can be commanded using the Power Mode Request Message (MID218), which is available as part of the OSP message set. More details regarding low power operation can be found in the Low Power Operating Modes Application Note.

#### 9.2.1. Full Power

This mode consumes the most average power, but it is the most accurate navigation mode and supports the most dynamic motion scenarios.



### 9.2.2. TricklePower™

This mode is a duty-cycling mode. It provides navigation updates at a fixed rate and retains a high quality of GNSS accuracy and dynamic motion response, but at a lower average power cost as compared to Full Power operation. TricklePower mode produces significant power savings in strong signal conditions.

### 9.2.3. Push-To-Fix

This mode provides for even lower power consumption than TricklePower. It is intended for applications that require infrequent position reports. The position is reported periodically by the receiver (once every 30 minutes by default) and also when requested. To request a position update, a pulse is asserted on the ON-OFF pin.

## 9.3. Host Serial Interface

As mentioned above in Section 7, the host serial interface can be configured as a UART, I2C or SPI port by strapping one or both pins GPIO 6 and GPIO 7 to certain levels at power up. The data rate for I2C is fixed at 400 kbps. The slave SPI supports a maximum clock input rate of 6.8 MHz. The UART can operate at baud rates of 4800, 9600, 19200, 38400, 57600, 115200, 230400 and 460800 bps.

## 9.4. NMEA Protocol Considerations

The lower UART baud rates are typically used for NMEA protocol. Note should be taken however of the bandwidth limitation at 4800 baud. By default, the SE868-V2 module communicates using NMEA at 4800 baud, with the periodic output messages limited to the GGA, GSA and RMC messages at once per second and the GSV message once every five seconds. At 9600 baud or higher, additional output messages may be enabled.

If the SE868-V2 is operated in TricklePower mode, a baud rate of at least 38400 is recommended. This reduces the time required for data output and allows the receiver to drop into the lowest power state for a longer average time.

Use the Set Serial Port (PSRF100) NMEA command to change the baud rate. This command can also be used to switch the protocol to OSP as described in the next section. Use the Query/Rate Control (PSRF103) to enable and disable output messages and set their output rates.

## 9.5. OSP Considerations

The higher baud rates are used for OSP. OSP offers a richer set of commands and more types of data output than does NMEA. Use the Set Serial Port (PSRF100) NMEA command to switch the protocol from NMEA to OSP. The minimum recommended baud rate for OSP is 38400, provided that debug data messages are not enabled. If data debug messages are enabled, the minimum baud rate is 115200 in order to prevent data from being dropped. The protocol



can be switched back to NMEA using the Switch to NMEA Protocol command (Message ID 129).



## 9.6. Motion Dynamics

### 9.6.1. Static Navigation

Static navigation, also called position pinning, is a mechanism that it is used by the receiver to freeze, or pin, the position when the velocity falls below a threshold indicating that the receiver is stationary. The heading is also frozen, and the velocity is reported as 0. The solution is then unpinned when the velocity increases above a threshold or when the computed position is a set distance from the pinned position, indicating that the receiver is in motion again. Note that these velocity and distance thresholds cannot be changed.

By default static navigation is disabled. It can be enabled by sending a Static Navigation message (Message ID 143) with the static navigation flag set to 1. This feature is useful for applications in which very low dynamics are not expected, the classic example being an automotive application.

### 9.6.2. Velocity Dead-Reckoning

Velocity dead-reckoning refers to the use of the last known velocity to propagate the navigation solution when there are insufficient measurements to calculate an updated solution. It serves to mitigate the effects of blocked satellite signals by continuing to provide a position output. Note that the receiver outputs status information which indicates whether a solution is being maintained using dead-reckoning.

By default the receiver operates in dead-reckoning mode for up to 15 seconds before invalidating the position. This timeout value is considered to be appropriate for most applications. It can be changed using the Mode Control message (Message ID 136). Valid timeout values are in a range from zero, which disables dead-reckoning, to two minutes.

## 9.7. Advanced Features

### 9.7.1. CW Jamming Detection

The SE868-V2 module detects, tracks, and removes narrow-band interfering signals (jammers) without the need for external components or tuning. It monitors a frequency band that is  $\pm 4$  MHz from the L1 frequency for jammers. Any number of jammers that occur outside of a  $\pm 1$  MHz center band are removed by the SE868-V2 with a 2 MHz band pass filter. Up to eight jammers inside this center band are removed using a notch filter.

Data regarding detected jammers is output using OSP messages. Message ID 92, Sub ID 1, reports up to eight of the most recently detected interferers. This feature is useful both in the design stage and during the production stage for uncovering issues related to unexpected jamming.



### 9.7.2. SBAS

The SE868-V2 receiver is capable of using Satellite-Based Augmentation System (SBAS) satellites as a source of both differential corrections and satellite range measurements. These systems (WAAS, EGNOS, MSAS) use geostationary satellites to transmit regional differential corrections via a GNSS-compatible signal. The use of SBAS corrections can improve typical position accuracy to 3m or less in open-sky applications.

Note that only an SBAS can be used as source of differential corrections. Other sources such as data from RTCM beacons are not supported.

By default the SE868-V2 does not attempt to acquire SBAS satellites. This can be changed by sending in a DGPS Source command (MID 133) and specifying the source of DGPS corrections as SBAS. When the receiver acquires SBAS satellites, it will demodulate and use corrections data from the satellite signal.

The receiver can be configured to compute SBAS satellite range measurements and use them in the navigation solution. This can be enabled through a control bit in the OSP Mode Control command (MID 136). See the OSP Manual for details.

### 9.7.3. 2-D Acquisition

By default, the SE868-V2 will compute a 2-D solution when possible when performing initial acquisition. In a 2-D solution, the receiver assumes a value for altitude and uses it to estimate the horizontal position. Under warm and hot start conditions, the receiver uses the last known value of altitude, which is a good assumption in most situations. However under cold start conditions, the last position is unknown, and the receiver assumes a value of 0. In situations where the true altitude is significantly higher than that, the horizontal position estimate will be noticeably impacted. To accommodate applications for which these situations are a concern, a version of SE868-V2 firmware is offered that requires a calculated altitude, i.e. a 3-D navigational solution, in order for the receiver to first enter navigation.



## 10. Operating Conditions and Electrical Specifications

Symbol	Parameter	Min	Typ	Max	Unit
<b>T</b>	Operating Temperature	-40	-	+85	°C
<b>VDD_18</b>	Supply voltage input	1.75	1.8	1.85	V
<b>VDD<sub>AC</sub></b>	Supply voltage ripple ,AC coupled	–	–	54	mV(rms) f=0-3Mhz
<b>VDD<sub>AC</sub></b>	Supply voltage ripple , AC coupled	–	–	15	mV (rms) f>3Mhz

**Table 5 – Recommended Operating Conditions**

Symbol	Parameter	Min	Typ	Max	Unit
<b>Current Usage</b>					
<b>I<sub>dd(max)</sub></b>	Maximum In rush current			84	mA
<b>I<sub>DD(peak)</sub></b>	Supply current, peak acq. GPS only	-	43		mA
<b>I<sub>DD(Acq)</sub></b>	Supply current, peak acq. GPS and GLONASS		54		
<b>I<sub>DD(ave)</sub></b>	Supply current average, tracking GPS only		38		ma
<b>I<sub>DD(ave)</sub></b>	Supply current average, tracking, GPS and GLONASS	-	45	-	mA
<b>I<sub>DD(Hib)</sub></b>	Supply current, hibernate state	-	53	-	µA
<b>I<sub>DD(ATP)</sub></b>	Track: TricklePower (100/1) Strong signals	-	9.5		mA
<b>Standard I/O</b>					
<b>V<sub>OL</sub></b>	Low level output voltage, I <sub>OL</sub> 2mA	-	-	0.4	V
<b>V<sub>OH</sub></b>	High level output voltage, I <sub>OH</sub> 2mA	0.75*VDD	-	-	V
<b>V<sub>IL</sub></b>	Low level input voltage	-0.3	-	0.45	V
<b>V<sub>IH</sub></b>	High level input voltage, IOH 2mA	0.7*VDD	-	3.6	V





<b>R<sub>PU</sub></b>	Internal pull-up resistor equivalent	50	86	157	kΩ
<b>R<sub>PD</sub></b>	Internal pull-down resistor equivalent	51	91	180	kΩ
<b>L<sub>I</sub></b>	Input leakage at V <sub>I</sub> =1.8V or 0V	-10	-	10	μA
<b>L<sub>O</sub></b>	Tristate output leakage at V <sub>O</sub> =1.8V or 0V	-10	-	10	μA
<b>C<sub>I</sub></b>	Input capacitance, digital output	-	8	-	pF

**Table 6 – DC electrical Characteristics**

Parameter	Symbol	Rating	Units
<b>RF Input Voltage</b>	All RF inputs	1.5	V
<b>RF Input Power</b>	All RF inputs	10	dBm
<b>ESD Voltage CDM JESD22-C101E</b>	All Pins	+/- 1100	V
<b>ESD Voltage HDM JEDEC JS-001-2012</b>	All Pins	+/-500	V
<b>1.8V Main Supply Voltage</b>	VDD_18	2.2	V
<b>I/O Pin Voltage</b>	All digital inputs	3.60	V
<b>Storage Temperature</b>		150	°C

**Table 7 – Absolute Maximum Ratings**





## 11. Handling and soldering

### 11.1. Moisture Sensitivity

The SE868-V2 module has a moisture sensitivity level rating of 3 as defined by IPC/JEDEC J-STD-020. This rating is assigned due to some of the components used within the SE868-V2.

The SE868-V2 is supplied in trays or tape and reel and is hermetically sealed with desiccant and humidity indicator card. The SE868-V2 parts must be placed and reflowed within 168 hours of first opening the hermetic seal provided the factory conditions are less than 30°C and less than 60% and the humidity indicator card indicates less than 10% relative humidity.

If the package has been opened or the humidity indicator card indicates above 10%, then the parts will need to be baked prior to reflow. The parts may be baked at  $+125^{\circ}\text{C} \pm 5^{\circ}\text{C}$  for 48 hours. However, the trays, nor the tape and reel can withstand that temperature. Lower temperature baking is feasible if the humidity level is low and time is available. Please see IPC/JEDEC J-STD-033 for additional information.

Additional information can be found on the MSL tag affixed to the outside of the hermetical seal bag.


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**NOTE:**

JEDEC standards are available for free from the JEDEC website  
<http://www.jedec.org>.

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	<p><b>CAUTION</b></p> <p>This bag contains <b>MOISTURE-SENSITIVE DEVICES</b></p>	<p>LEVEL</p> <div style="border: 2px solid black; padding: 5px; display: inline-block; font-size: 24px; font-weight: bold;">3</div> <p style="font-size: 8px;">If Blank, see adjacent bar code label</p>
<ol style="list-style-type: none"> <li>1. Calculated shelf life in sealed bag: 12 months at <math>&lt; 40^{\circ}\text{C}</math> and <math>&lt; 90\%</math> relative humidity (RH)</li> <li>2. Peak package body temperature: _____ <math>^{\circ}\text{C}</math>  <div style="text-align: right; font-size: 8px;">If Blank, see adjacent bar code label</div> </li> <li>3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must               <ol style="list-style-type: none"> <li>a) Mounted within: <u>168</u> hours of factory  <div style="text-align: right; font-size: 8px;">If Blank, see adjacent bar code label</div> </li> <li>conditions <math>\leq 30^{\circ}\text{C}/60\%</math></li> <li>b) stored at <math>&lt;10\%</math> RH</li> </ol> </li> <li>4. Devices require bake, before mounting, if:               <ol style="list-style-type: none"> <li>a) Humidity Indicator Card is <math>&gt; 10\%</math> when read at <math>23 \pm 5^{\circ}\text{C}</math></li> <li>b) 3a or 3b not met.</li> </ol> </li> <li>5. If baking is required, devices may be baked for 48 hours at <math>125 \pm 5^{\circ}\text{C}</math>  <div style="text-align: center; font-size: 8px;">Note: If device containers cannot be subjected to high temperature or shorter bake times are desired, reference IPC/JEDEC J-STD-033 for bake procedure</div> </li> </ol>		
<p>Bag Seal Date: _____  <div style="text-align: right; font-size: 8px;">If Blank, see adjacent bar code label</div> </p> <p style="font-size: 8px;">Note: Level and body temperature defined by IPC/JEDEC J-STD-020</p>		

**Figure 3- Label for Moisture Sensitive Devices**

## 11.2. ESD

The SE868-V2 is an electrostatic discharge sensitive device and should be handled in accordance with JESD625-A requirements for Handling Electrostatic Discharge Sensitive (ESDS) Devices. Although the SE868-V2 is a module, the expecting handling of the SE868-V2 during assembly and test is identical to that of a semiconductor device.

**Note:** JEDEC standards are available for free from the JEDEC website <http://www.jedec.org>.

## 11.3. Reflow

The SE868-V2 is compatible with lead free soldering processes as defined in IPC/JEDEC J-STD-020. The reflow profile must not exceed the profile given IPC/JEDEC J-STD-020 Table 5-2, "Classification Reflow Profiles". Although IPC/JEDEC J-STD-020 allows for three reflows, the assembly process for the SE868-V2 uses one of those profiles. Thus the SE868-V2 is limited to two reflows.



**Note:** JEDEC standards are available for free from the JEDEC website  
<http://www.jedec.org>.

When re-flowing a dual-sided SMT board, it is important to reflow the side containing the SE868-V2 module last. This prevents heavier components within the SE868-V2 becoming dislodged if the solder reaches liquidus temperature while the module is inverted.

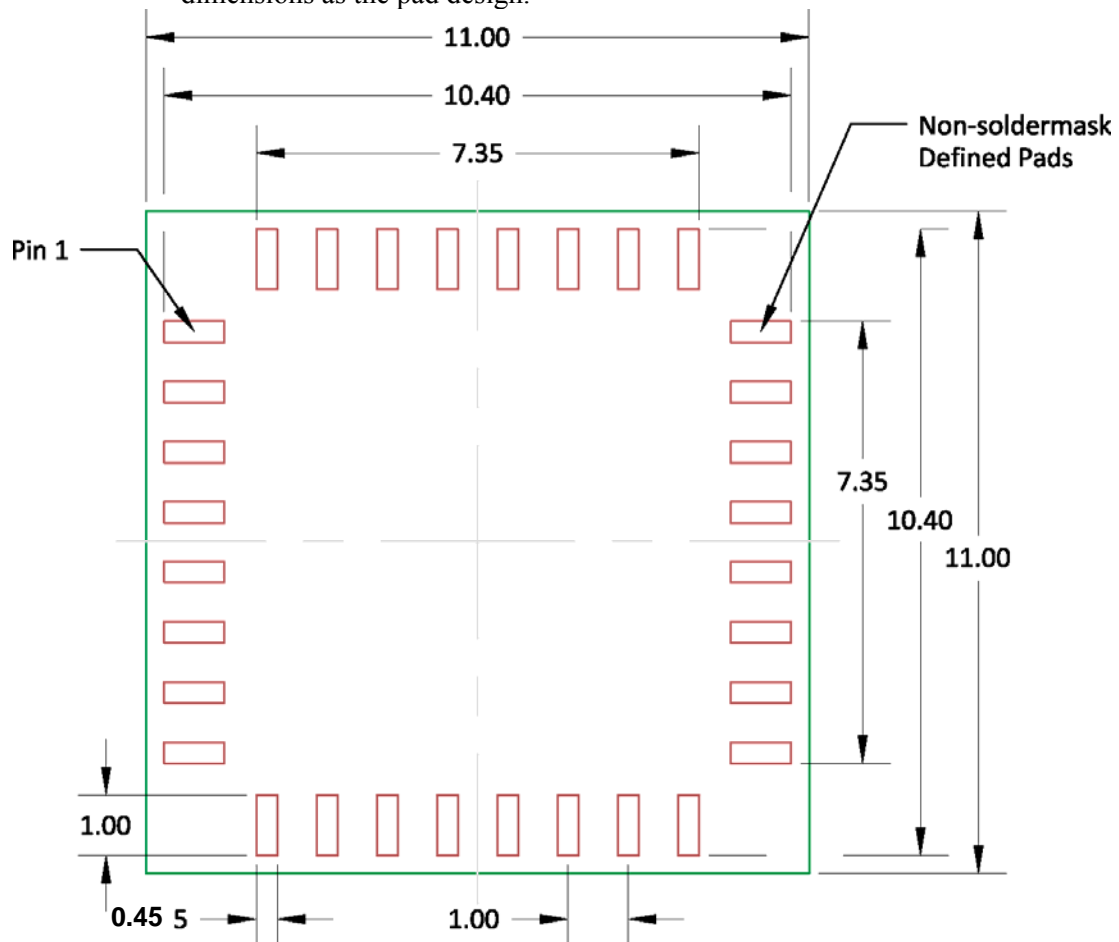
## 11.4. Assembly Issues

Due to the piezo-electric components within the SE868-V2 the component should be placed close to the end of the assembly process to minimize shock to the module. During board singulation, pay careful attention to unwanted vibrations and resonances introduced into the board assembly by the board router.



## 12. PCB Layout Details

The PCB footprint on the receiving board should match the SE868-V2 pad design shown below. The solder mask opening is generally determined by the component geometry of other parts on the board and can be followed here. Standard industry practice is to use a paste mask stencil opening the same dimensions as the pad design.



All Dimensions are in mm.

Viewed from Top

**Figure 4 – SE868-V2 Pad Design**



## 13. Document History

Revision	Date	Changes
1	2013-09-04	First issue
2	2013-10-07	Section 1.7.5 edited for clarity, Section 2.4 edited for content. Header corrected. Document history corrected.

