LE866 PSM Application Note

80471NT11483A Rev. 2 – 2017-06-06

TELIT TECHNICAL DOCUMENTATION

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APPLICABILITY TABLE

PRODUCTS

- LE866-SV1
- LE866A1-KK
- LE866A1-NA
- LE866A1-JS

CONTENTS

1. INTRODUCTION

1.1. Scope

The LE866 includes unique advanced features in order to support the PSM according to 3GPP Rel-12.

The aim of this document is the description of the suggested Application design to use this functionality.

1.2. Audience

This document is intended for Telit customers, who are integrators, about to implement their applications using our LE866 modules.

1.3. Contact Information, Support

For general contact, technical support services, technical questions and report documentation errors contact Telit Technical Support at:

- TS-EMEA@telit.com
- TS-AMERICAS@telit.com
- TS-APAC@telit.com

Alternatively, use:

http://www.telit.com/support

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

http://www.telit.com

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

1.4. Text Conventions

Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

1.5. Related Documents

- LE866 HW User Guide, 1VV0301210
- LE866 AT Commands Reference Guide, 80471ST10691A
- Telit EVK2 User Guide, 1vv0300704

2. OVERVIEW

The aim of this document is the description of some hardware solutions useful for developing a product with the Telit LE866 module.

In this document all the basic functions of a mobile phone will be taken into account; for each one of them a proper hardware solution will be suggested and eventually the wrong solutions and common errors to be avoided will be evidenced. Obviously this document cannot embrace the whole hardware solutions and products that may be designed. The wrong solutions to be avoided shall be considered as mandatory, while the suggested hardware configurations shall not be considered mandatory, instead the information given shall be used as a guide and a starting point for properly developing your product with the Telit LE866 module. For further hardware details that may not be explained in this document refer to the Telit LE866 Product Description document where all the hardware information is reported.

NOTICE:

EN) The integration of the LTE **LE866** cellular module within user application shall be done according to the design rules described in this manual.

(IT) L'integrazione del modulo cellulare LTE **LE866** all'interno dell'applicazione dell'utente dovrà rispettare le indicazioni progettuali descritte in questo manuale.

(DE) Die Integration des **LE866** LTE Mobilfunk-Moduls in ein Gerät muß gemäß der in diesem Dokument beschriebenen Kunstruktionsregeln erfolgen.

(SL) Integracija LTE **LE866** modula v uporabniški aplikaciji bo morala upoštevati projektna navodila, opisana v tem priročniku.

(SP) La utilización del modulo LTE **LE866** debe ser conforme a los usos para los cuales ha sido deseñado descritos en este manual del usuario.

(FR) L'intégration du module cellulaire LTE **LE866** dans l'application de l'utilisateur sera faite selon les règles de conception décrites dans ce manuel.

(HE) האינטגרטור מתבקש ליישם את ההנחיות המפורטות במסמך זה בתהליך האינטגרציה של המודם הסלולרי עם המוצר. **LE866**

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3. PSM DESCRIPTION

The Power Saving Mode (PSM) in 3GPP Rel12 allows the Module to skip idle mode tasks for a longer time period while still maintaining the NAS context.

This feature permits to reduce the overall power consumption when there is no required data activity with the network for a long time.

This saves the power also related to the Paging activity.

The PSM reduces the signaling load between the LE866 and the network on NAS level (24.301 Rel.12 chapter 5.3.11) compared to a standard attach/detach procedure.

Within the attach/RAU/TAU procedure the UE indicates that it supports PSM.

The network confirms PSM usage by sending a value for a timer (T3324) in the confirmation message.

The timer T3324 specifies an active period after the RAU/TAU procedure the UE has to follow the normal idle mode procedures (paging reception, measurements,..).

After timer T3324 elapses the Module enters PSM state, i.e. it disables all AS/NAS activities until the next periodic RAU/TAU update.

A second Timer (T3412) is defining the duration of the PSM.

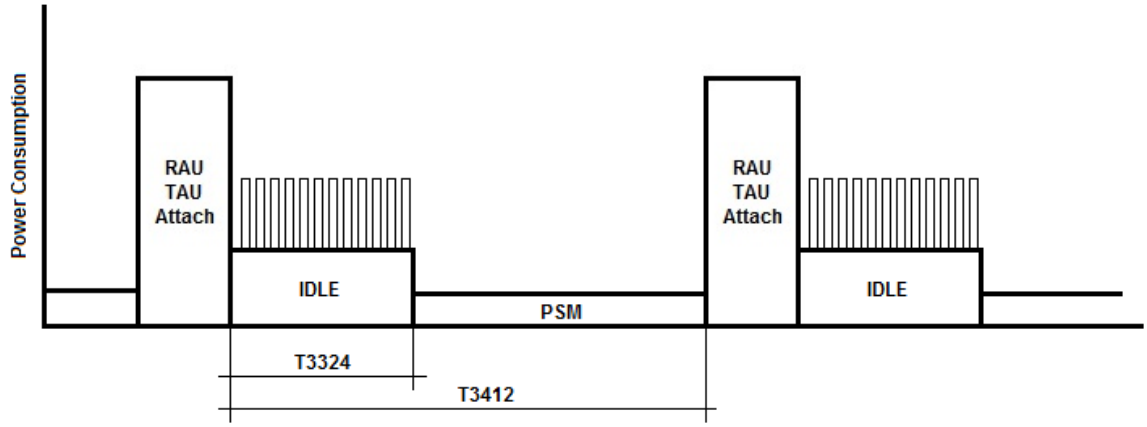
During this period the Module is NOT reachable by the network, i.e. it cannot be paged and stops access stratum activities.

Before the inactivity period the complete NAS context needs to be stored and reused when accessing the network again.

The Module can leave the PSM mode at any point in time when there is MO data or when periodic TAU timer expires.

The PSM is only intended for those Modules that can tolerate a high MT Call latency.

The 3GPP standard does not imply whether or to which extend the PSM does reduce the power of the Module. Only the signaling reduction (i.e. Not doing a reattach but just a RAU/TAU procedure) is defined.



4. PINS ALLOCATION

4.1. PIN list for PSM Mode

Pin	Signal	I/O	Function	Type	Comment
PSM Control Lines					
D3	PSM_WAKE	I	Wake Up from PSM Mode	Analog	
E8	PSM_STATUS	O	PSM Status	CMOS 1.8V	
F8	PSM_ENA_OUT	O	PSM Enable for external LDOs	CMOS 1.8V	
SIM card interface					
C7	SIMVCC	-	External SIM signal – Power supply for the SIM	1.8V Only	
B7	SIMRST	O	External SIM signal – Reset	CMOS 1.8	
A7	SIMCLK	O	External SIM signal – Clock	CMOS 1.8	
A6	SIMIO	I/O	External SIM signal – Data I/O	CMOS 1.8	
D8	VDDIO_IN	I	IO bus Supply input	Power	
RF SECTION					
G2	MAIN_ANT	I/O	LTE Main Antenna (50 ohm)	RF	
C0	DIV_ANT	I	LTE RX Diversity Antenna (50 ohm)	RF	
Miscellaneous Functions					
G4	RESET*	I	Reset Input	VBATT	Pull up to VBATT (10Kohm)
G6	VAUX PWRMON	O	1.8V stabilized output Power ON monitor	Power	

Power Supply				
E2	VBATT	-	Main power supply (Baseband)	Power
E0	VBATT_PA	-	Main power supply (Radio PA)	Power
E1	VBATT_PA	-	Main power supply (Radio PA)	Power
B0	GND	-	Ground	Power
D0	GND	-	Ground	Power
F0	GND	-	Ground	Power
G0	GND	-	Ground	Power
D1	GND	-	Ground	Power
F1	GND	-	Ground	Power
G1	GND	-	Ground	Power
D2	GND	-	Ground	Power
F2	GND	-	Ground	Power
C3	GND	-	Ground	Power
E3	GND	-	Ground	Power
F3	GND	-	Ground	Power
G3	GND	-	Ground	Power
F6	GND	-	Ground	Power
A8	GND	-	Ground	Power
G8	GND	-	Ground	Power
A11	GND	-	Ground	Power
G11	GND	-	Ground	Power

4.2. LGA Pads Layout

TOP VIEW

	A	B	C	D	E	F	G	
0	RESERVED	GND	DIV ANT	GND	VBATT_PA	GND	GND	
1	C105/RTS	C106/CTS	TX AUX	GND	VBATT_PA	GND	GND	
2	C108/DTR	C109/DCD	RX AUX	GND	VBATT	GND	MAIN ANT	
3	C107/DSR	C125/RING	GND	PSM_WAKE	GND	GND	GND	
4	C103/TXD	GPIO_06	GPIO_07	RESERVED	DAC_OUT	ADC_IN1	RESET*	
5	C104/RXD	GPIO_05	GPIO_01	GPIO_04	USB_D+	RESERVED	RESERVED	
6	SIMIO	RESERVED	GPIO_02	GPIO_03	USB_D-	GND	VAUX/PWR MON	
7	SIMCLK	SIMRST	SIMVCC	RESERVED	RESERVED	RESERVED	RESERVED	
8	GND	RESERVED	RESERVED	VDDIO_IN	PSM_STAT US	PSM_ENA_ OUT	GND	
9	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	
10	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	
11	GND	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	GND	

4.3. PSM SIGNALS DETAIL

4.3.1. PSM_WAKE

PSM_WAKE is the only pin that can wake the system from the PSM Mode.

It is normally Low and should be set to High to wake up the module.

NOTE:

The pin requires to add a pull down resistor on the application.

4.3.2. PSM_STATUS

PSM_STATUS is a GPIO controlled by SW that is low during the PSM mode and high during regular operation. This pin is used for the LE866/Host Controller protocol when entering/exiting PSM state.

4.3.3. PSM_ENA_OUT

PSM_ENA_OUT is low during normal operation and open drain during the PSM state. It may be used to enable/disable the unnecessary supplies to the different system components when entering exiting the PSM state.

4.3.4. RESET*

RESET* disables the entire integrated power management and is used as a power reset.

4.3.5. VDDIO_IN

VDDIO_IN is the Digital IO supply Input pin.

4.4. Logic Levels Specification

ABSOLUTE MAXIMUM RATINGS:

Parameter	Min	Max
Input level on any digital pin (CMOS 1.8) with respect to ground	-0.3V	VDDIO_IN +0.3V
Input level on any digital pin (CMOS 1.8) with respect to ground when VDDIO is not supplied	-0.3V	0.3V

OPERATING RANGE - INTERFACE LEVELS (1.8V CMOS):

Parameter	Min	Max
Input high level	1.55V	1.9V
Input low level	0V	0.35V
Output high level	1.35V	1.8V
Output low level	0V	0.8V

WARNING:

If VDDIO_IN line is not powered (i.e. during the sleep states in PSM=2 when supplied by VAUX, during transition phases BOOT, RESET etc. and when the module is unsupplied) it is important to avoid back powering the digital pins. Exceeding the absolute maximum ratings could damage permanently the module.

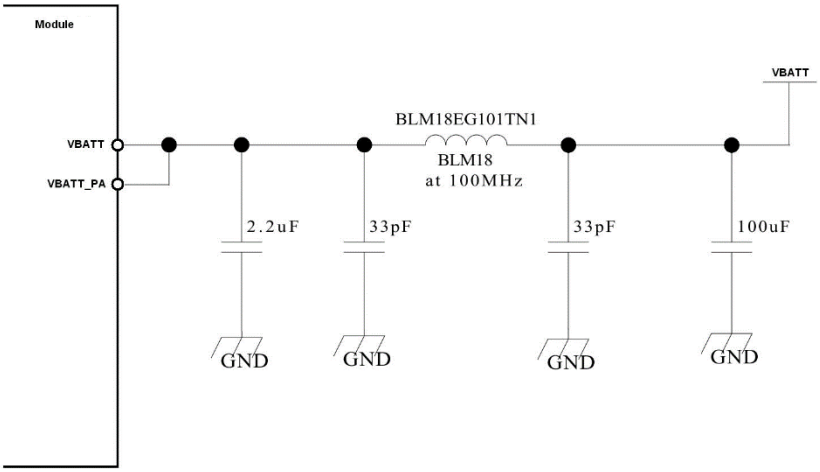
4.5. General Design Rules

The principal guidelines for the PSM Design embrace three different design steps:

- the Power supply
- the Digital IOs supply and control
- the SIM Interface latches.

4.5.1. Power Supply Guidelines

The below figure shows the recommended circuit:



For additional details please refer to the LE866 HW User Guide

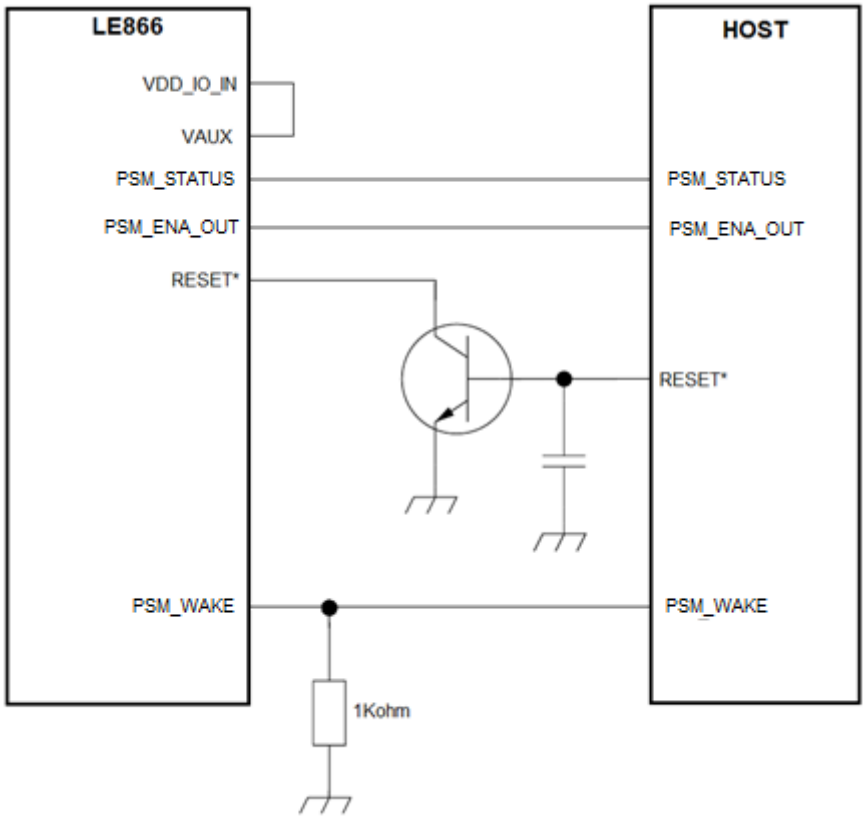
4.5.2. Digital IOs Supply Guidelines

The Digital IO section requires to be supplied applying a 1.8V power supply to the VDDIO_IN input.

In a normal Application design, this is done connecting the VDDIO_IN to the VAUX/PWRMON line.

Using this supply line we have two effects:

- When in PSM=2 the VAUX is switched off so the Host has to ensure to avoid applying any high logic level to the IOs that could damage the module.
- VAUX has a quiescent current of ~40uA and if it is kept alive also VSIM is kept alive (total of ~80uA)

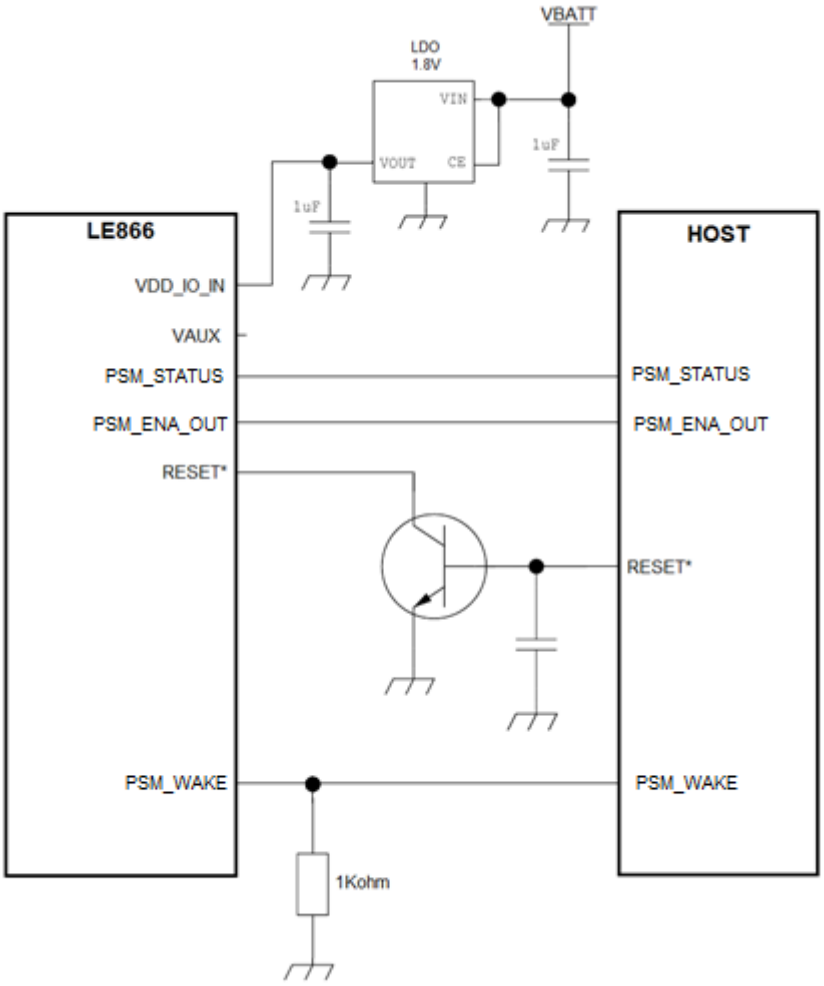


During the PSM modes the host should ignore the value of the signals coming from the LE866 (as all pins are turned to High Z if VDD_IO_IN is available or to non defined state if VDDIO_IN is shut off)

In systems that cannot ensure that no voltage will be applied to the LE866 IOs during PSM status, the VDDIO_IN line should be kept supplied.

The LE866 lowest power consumption can be achieved powering the VDDIO_IN externally (allowing all other LE866 power supplies to be disabled).

This could be done using for example an LDO with a low quiescent current (i.e. TOREX XC6504A181NR-G)

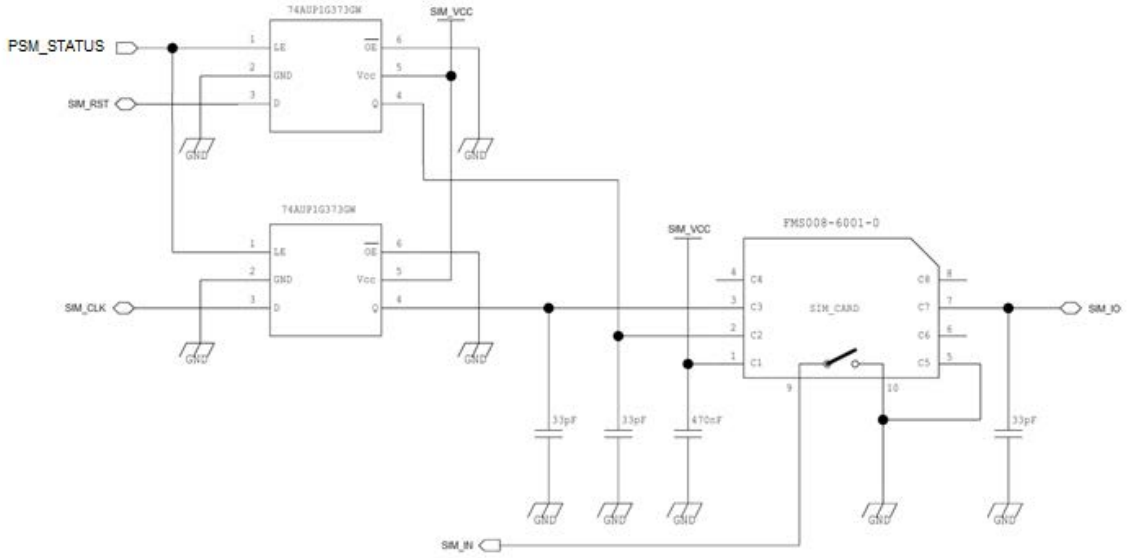


Another alternative is to add logic such as a buffer on the required signals, using the PSM_STATUS line as the output enable control Low=PSM, High=Not PSM.

4.5.3. SIM Lines control

In order to ensure the 3GPP Rel.12 compliance when using the SIM in PSM states it is suggested to use two latches on the SIM_RST and SIM_CLK lines.

The two latches are enabled by the PSM_STATUS line.



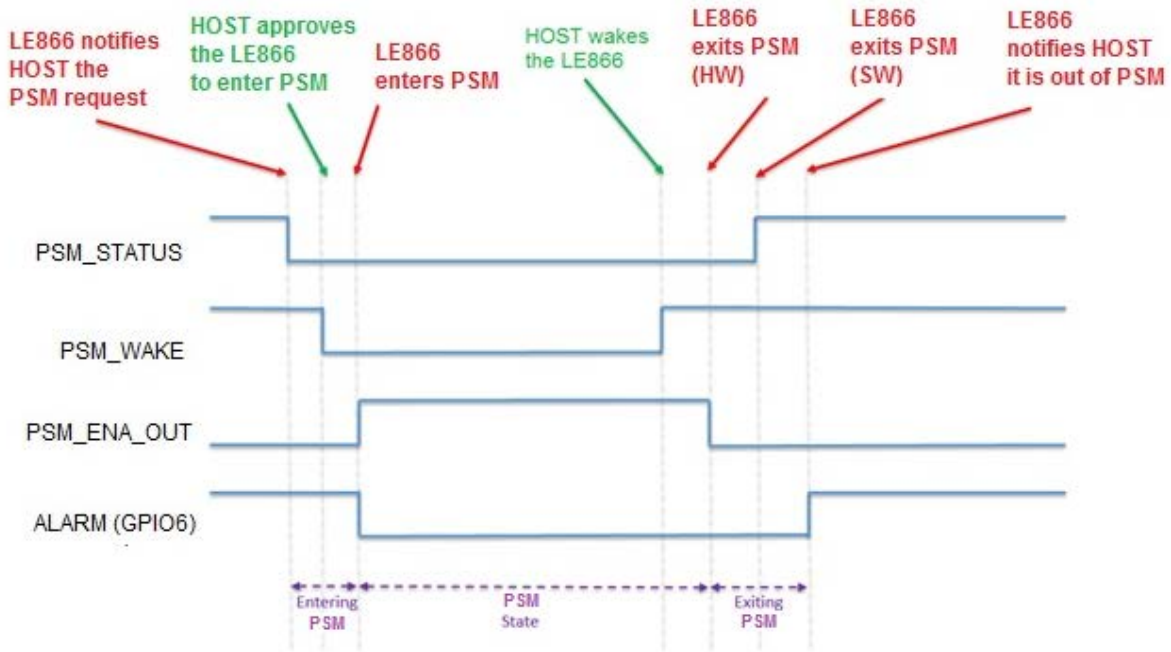
4.6. Enter and Exit from PSM States

Since the LE866 outputs become inputs\non-defined during the PSM states, the module and the host should follow a specific protocol to ensure the proper system operation:

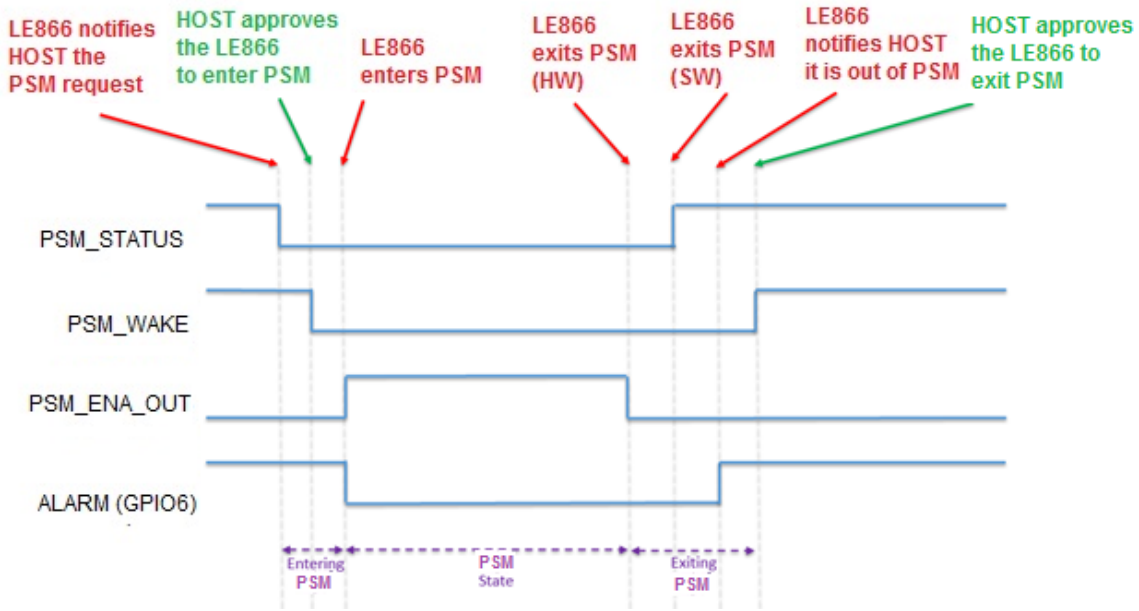
- LE866 notifies the host before going into a PSM state by setting PSM_STATUS low
- Host makes proper preparations and notifies the LE866 he is allowed to enter the PSM state by setting the PSM_WAKE low (this could be avoided if a pull down resistor is added to the PSM_WAKE line)
- LE866 enters in PSM state
- If required, the host can wake the LE866 at any time by setting the PSM_WAKE line high.
- LE866 notifies the host when it is out of the PSM states by setting PSM_STATUS high
- Host keeps the PSM_WAKE line high to ensure the module does not enter the PSM states without proper coordination and permission from the host.

If required on specific applications or by specific hosts, it is possible to add dedicated external logic to toggle the PSM_WAKE pin high, when there is an event on the preferred pin/interface (for example on the UART RTS)

The following diagram shows the process of PSM enter/exit due to Host request:



The following diagram shows the process of PSM enter/exit due to RTC request:



5. GLOSSARY AND ACRONYMS

	Description
TTSC	Telit Technical Support Centre
USB	Universal Serial Bus
HS	High Speed
DTE	Data Terminal Equipment
LTE	Long Term Evolution
PSM	Power Saving Mode according to 3GPP Rel.12
AS	Access Stratum
NAS	Non-Access Stratum
RAU	Routing Area Update
TAU	Tracking Area Update
HSIC	High Speed Inter Chip
SIM	Subscriber Identification Module
SPI	Serial Peripheral Interface
ADC	Analog – Digital Converter
DAC	Digital – Analog Converter
I/O	Input Output
GPIO	General Purpose Input Output
CMOS	Complementary Metal – Oxide Semiconductor
CLK	Clock
MRDY	Master Ready
SRDY	Slave Ready
CS	Chip Select
RTC	Real Time Clock
PCB	Printed Circuit Board
ESR	Equivalent Series Resistance
VSWR	Voltage Standing Wave Radio
VNA	Vector Network Analyzer

6. DOCUMENT HISTORY

Revision	Date	Changes
0	2016-07-26	Preliminary Version
1	2016-12-22	Updated 1.4, 4.3, 4.4, 4.5.2
2	2017-06-06	2017 Template Applied

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