LE922A6
Hardware User Guide

1vv0301271 Rev.5 - 2017-04-12

Making machines talk.

APPLICABILITY TABLE

PRODUCT
LE922A6-A1
LE922A6-E1
LE922A6-E2 (P/N MKT3990251535)

APPLICABILITY TABLE 1

SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

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Contents

1. Introduction

1.1. Scope

The aim of this document is to present possible and recommended hardware solutions useful for developing a product with the Telit LE922A6 module. All the features and solutions detailed are applicable to all LE922A6 where "LE922A6" refers to the modules listed in the applicability table.

If a specific feature is applicable to a specific product, it will be clearly highlighted.

NOTICE:

The description text "LE922A6" refers to all modules listed in the APPLICABILITY TABLE 1.

1.2. Audience

This document is intended for Telit customers, especially system integrators, about to implement their applications using Telit LE922A6 module.

1.3. Contact Information, Support

For general contact, technical support, to report documentation errors and to order manuals, contact Telit's Technical Support Center (TTSC) at:

TS-EMEA@telit.com
TS-NORTHAMERICA@telit.com
TS-LATINAMERICA@telit.com
TS-APAC@telit.com

Alternatively, use:

http://www.telit.com/en/products/technical-support-center/contact.php

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

http://www.telit.com

To register for product news and announcements or for product questions contact Telit's Technical Support Center (TTSC).

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

1.4. Document Organization

This document contains the following chapters:

Chapter 1: "Introduction" provides a scope for this document, target audience, contact and support information, and text conventions.

Chapter 2: "General Product Description" gives an overview of the features of the product.

Chapter 3: "LE922A6 Module Connections" deals with the pin out configuration and layout.

Chapter 4: "Hardware Commands" instructs how to control the module via hardware

Chapter 5: "Power Supply" deals with supply and consumption.

Chapter 6: "Antenna" The antenna connection and board layout design are the most important parts in the full product design

Chapter 7: "Logic Level specifications" Specific values adopted in the implementation of logic levels for this module.

Chapter 8: "USB Port"

Chapter 9: "Serial Ports"

Chapter 10: "Peripheral Ports"

Chapter 11: "Audio Section Overview"

Chapter 12: "General Purpose I/O" How the general purpose I/O pads can be configured.

Chapter 13 "DAC and ADC Section" Deals with these two kind of analog converters.

Chapter 14: "Mounting the module on your board"

Chapter 15: "Application Guides"

Chapter 16: "Packing System"

Chapter 17: "Safety Recommendations"

Chapter 18: "Document History"

1.5. Text Conventions

Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

1.6. Related Documents

- LE922A6 AT command reference guide,
- Telit EVK2 User Guide, 1vv0300704
- SIM integration design guide, 8000NT10001a

2. General Product Description

2.1. Overview

The aim of this document is to present possible and recommended hardware solutions useful for developing a product with the Telit LE922A6 module.

In this document all the basic functions of a wireless module will be taken into account; for each one of them a valid hardware solution will be suggested and usually incorrect solutions and common errors to be avoided will be highlighted. Obviously this document cannot embrace every hardware solution or every product that may be designed. Obviously avoiding invalid solutions must be considered as mandatory. Whereas the suggested hardware configurations need not be considered mandatory, the information given should be used as a guide and a starting point for properly developing your product with the Telit LE922A6 module.

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NOTICE:

The integration of the WCDMA/HSPA+/LTE LE922A6 cellular module within user application must be done according to the design rules described in this manual.

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2.2. Operating Frequency

The operating frequencies in WCDMA and LTE modes are conformed to the 3GPP specifications.

The table below shows a summary of all possible region variants within the LE922A6, with the supported band sets in each variant and with the supported band pairs for 2DL carrier aggregation.

Region Variant	LTE FDD	LTE TDD	HSPA+	LTE Carrier Aggregation
LE922A6-A1	B1, B3, B7, B28	B40	B1, B8	1+7, 1+28, 3+3, 3+7, 3+28, 3+40, 7+7, 28+7, 40+40
LE922A6-E1	B3, B7, B20	-	-	3+3, 3+7, 3+20, 7+7, 7+20
LE922A6-E2	B3, B7, B8, B20, B28. B32	-	-	3+3, 3+7, 3+8, 3+20, 3+28, 7+7, 7+8, 7+20, 7+28, 20+32

Mode	Freq. TX (MHz)	Freq. RX (MHz)	Channels	TX - RX offset
WCDMA 2100 – B1	1920 ~ 1980	2110 ~ 2170	Tx: 9612 ~ 9888 Rx: 10562 ~ 10838	190MHz
WCDMA 900 – B8	880 ~ 915	925 ~ 960	Tx: 2712 ~ 2863 Rx: 2937 ~ 3088	45MHz
LTE 2100 – B1	1920 ~ 1980	2110 ~ 2170	Tx: 18000 ~ 18599 Rx: 0 ~ 599	190MHz
LTE 1800 – B3	1710 ~ 1785	1805 ~ 1880	Tx: 19200 ~ 19949 Rx: 1200 ~ 1949	95MHz
LTE 2600 – B7	2500 ~ 2570	2620 ~ 2690	Tx: 20750 ~ 21449 Rx: 2750 ~ 3449	120MHz
LTE 900 – B8	880 ~ 915	925 ~ 960	Tx: 21450 ~ 21799 Rx: 3450 ~ 3799	45MHz
LTE 800 – B20	832 ~ 862	791 ~ 821	Tx: 24150 ~ 24449 Rx: 6150 ~ 6449	-41MHz
LTE 700 – B28	703 ~ 748	758 ~ 803	Tx : 27210 ~ 27659 Rx : 9210 ~ 9659	55MHz
LTE 1500 – B32	Downlink only	1452 ~ 1496	Rx : 9920 ~ 10359	-
LTE TDD 2300 – B40	2300 ~ 2400	2300 ~ 2400	Tx: 38650 ~ 39650 Rx: 38650 ~ 39650	0MHz

2.3. LE922A6 Mechanical Dimensions

The Telit LE922A6 module overall dimensions are:

- Length: 34 mm, +/- 0.15 mm Tolerance
- Width: 40 mm, +/- 0.15 mm Tolerance
- Thickness: 2.9 mm, +/- 0.15 mm Tolerance

2.4. Weight

The module weight of LE922A6 is about 9 gram.

2.5. Rx Sensitivity and Maximum Tx Power

LE922A6 Rx sensitivity and Maximum Tx power levels are as follow:

Region Variant	Mode	Typical Rx Sensitivity * / ** (LTE BW = 10MHz)	Typical Tx Max Power ** (LTE BW = 10MHz, 1RB)
LE922A6-A1	**LTE 2100 – B1**	-98.0 dBm	23.0 dBm
	LTE 1800 – B3	-99.0 dBm	23.0 dBm
	LTE 2600 – B7	-99.0 dBm	23.0 dBm
	LTE 700 – B28	-99.0 dBm	23.0 dBm
	LTE TDD 2300 – B40	-99.0 dBm	23.0 dBm
	WCDMA 2100 – B1	-108.5 dBm	23.0 dBm
	WCDMA 900 – B8	-108.5 dBm	23.0 dBm
LE922A6-E1	**LTE 1800 – B3**	-99.0 dBm	23.0 dBm
	LTE 2600 – B7	-99.0 dBm	23.0 dBm

	LTE 800 – B20	-99.0 dBm	23.0 dBm
LE922A6-E2	**LTE 1800 – B3**	TBD	TBD
	LTE 2600 – B7	TBD	TBD
	LTE 900 – B8	TBD	TBD
	LTE 800 – B20	TBD	TBD
	LTE 700 – B28	TBD	TBD
	LTE 1500 – B32	TBD	Downlink only

* LTE Rx Sensitivity shall be verified by using both (all) antenna ports simultaneously.
** 3.8 Voltage / Room temperature

2.6. Environmental requirements

2.6.1. Temperature range

Operating Temperature Range	–20°C ~ +55°C : This range is defined by 3GPP (the global standard for wireless mobile communication). Telit guarantees its modules to comply with all the 3GPP requirements and to have full functionality of the module with in this range. –40°C ~ +85°C: Telit guarantees full functionality within this range as well. However, there may possibly be some performance deviations in this extended range relative to 3GPP requirements, which means: some RF parameters may deviate from 3GPP specification in the order of few dB. For example: receiver sensitivity or maximum output power may be slightly degraded. Even so, all the functionalities like call connection, SMS , USB communication, UART activation etc. will be maintained, and the effect of such degradations will not lead to malfunction.
Storage and non-operating Temperature Range	–40°C ~ +85°C

2.6.2. RoHS compliance

As a part of Telit corporate policy of environmental protection, the LE922A6 complies with the RoHS (Restriction of Hazardous Substances) directive of the European Union (EU directive 2011/65/EU).

3. LE922A6 Module Connections

3.1. PIN-OUT

PAD	Signal	I/O	Function	Type	COMMENT
USB HS 2.0 Communication Port					
D19	USB_D+	I/O	USB differential Data(+)		
F19	USB_D-	I/O	USB differential Data(-)		
A18	USB_VBUS	AI	Power sense for the internal USB transceiver		
USB SS 3.0 Communication Port					
C20	USB_SS_RX_P	I	USB super-speed receive (+)		
E20	USB_SS_RX_M	I	USB super-speed receive (-)		
G20	USB_SS_TX_P	O	USB super-speed transmit (+)		
J20	USB_SS_TX_M	O	USB super-speed transmit (-)		
Asynchronous UART – Prog. / data +HW Flow Control					
AH19	C103/TXD	I	Serial data input (TXD) from DTE	1.8V	
AF19	C104/RXD	O	Serial data output to DTE	1.8V	
AC18	C108/DTR	I	Input for Data terminal ready signal (DTR) from DTE	1.8V	
AA18	C105/RTS	I	Input for Request to send signal (RTS) from DTE	1.8V	
AK19	C106/CTS	O	Output for Clear to send signal (CTS) to DTE	1.8V	
AE18	C109/DCD	O	Output for Data carrier detect signal (DCD) to DTE	1.8V	
AG18	C107/DSR	O	Output for Data set ready signal (DSR) to DTE	1.8V	
AJ18	C125/RING	O	Output for Ring indicator signal (RI) to DTE	1.8V	
Asynchronous Auxiliary UART					
AB19	TXD_AUX	O	Auxiliary UART (TX Data to DTE)	1.8V	
AD19	RXD_AUX	I	Auxiliary UART (RX Data from DTE)	1.8V	
SPI – Serial Peripheral Interface					
P19	SPI_CLK	O	SPI Clock output	1.8V	
M19	SPI_MISO	I	SPI data Master Input Slave output	1.8V	
K19	SPI_MOSI	O	SPI data Master Output Slave input	1.8V	
N18	SPI_CS	O	SPI Chip select output	1.8V	
SIM Card Interface 1					
A10	SIMCLK1	O	External SIM signal – Clock	1.8/2.85V	
B11	SIMRST1	O	External SIM signal – Reset	1.8/2.85V	
B9	SIMIO1	I/O	External SIM signal - Data I/O	1.8/2.85V	
B7	SIMIN1	I	External SIM signal - Presence (active low)	1.8V	
A8	SIMVCC1	-	External SIM signal – Power supply for the SIM	1.8/2.85V	
Digital Voice interface (DVI)					
D11	DVI_WA0	O	Digital Voice interface (WA0 master output)	1.8V	

PAD	Signal	I/O	Function	Type	COMMENT
C8	DVI_RX	I	Digital Voice interface (RX)	1.8V	
D9	DVI_TX	O	Digital Voice interface (TX)	1.8V	
C10	DVI_CLK	O	Digital Voice interface (CLK master output)	1.8V	
C12	AUDIO_REF_CLK	O	Audio Reference clock for an external codec		
I2C interface					
C14	I2C_SCL	I/O	I2C clock	1.8V	
D13	I2C_SDA	I/O	I2C Data	1.8V	
Digital I/O					
F9	GPIO_01	I/O	GPIO_01	1.8V	I2C alternate
E10	GPIO_02	I/O	GPIO_02	1.8V	I2C alternate
F11	GPIO_03	I/O	GPIO_03	1.8V	I2C alternate
E12	GPIO_04	I/O	GPIO_04	1.8V	I2C alternate
F13	GPIO_05	I/O	GPIO_05	1.8V	I2C alternate
E14	GPIO_06	I/O	GPIO_06 / DAC_OUT	1.8V	I2C alternate
R18	GPIO_07	I/O	GPIO_07	1.8V	I2C alternate
S19	GPIO_08	I/O	GPIO_08	1.8V	I2C alternate
U19	GPIO_09	I/O	GPIO_09	1.8V	I2C alternate
W19	GPIO_10	I/O	GPIO_10	1.8V	I2C alternate
RF Section					
AD1	ANT 1	I/O	UMTS/LTE Primary Antenna 1 (50 Ohm)	RF	
AM1	ANT 2	I/O	UMTS/LTE Primary Antenna 2 (50 Ohm)	RF	
AU9	ANT_DIV 1	I	UMTS/LTE Antenna Diversity Input 1 (50 Ohm)	RF	
AU13	ANT_DIV 2	I	UMTS/LTE Antenna Diversity Input 2 (50 Ohm)	RF	
Miscellaneous Function					
AS1	ON_OFF_N	I	Power ON/OFF Input		Active Low
AN12	SHDN_N	I	Unconditional Shut down Input		Active Low
AN8	RESET_N	I	Reset Input		Active Low
P17	VAUX/PWRMON	O	Supply Output for External Accessories / Power ON Monitor	1.8V	
D5	ADC_IN1	AI	Analog/Digital Converter Input 1	Analog	
E6	ADC_IN2	AI	Analog/Digital Converter Input 2	Analog	
F7	ADC_IN3	AI	Analog/Digital Converter Input 3	Analog	
AU3	STAT_LED	O	Status Indicator LED	1.8V	
AN10	SW_RDY	O	Indicates that the boot sequence completed successfully	1.8V	
Power Supply					
AP17	VBATT	-	Main Power Supply (Digital Section)	Power	
AP19	VBATT	-	Main Power Supply (Digital Section)	Power	
AR18	VBATT	-	Main Power Supply (Digital Section)	Power	
AR20	VBATT	-	Main Power Supply (Digital Section)	Power	
AS17	VBATT_PA	-	Main Power Supply (RF Transmit Power Section)	Power	

PAD	Signal	I/O	Function	Type	COMMENT
AS19	VBATT_PA	-	Main Power Supply (RF Transmit Power Section)	Power	
AT18	VBATT_PA	-	Main Power Supply (RF Transmit Power Section)	Power	
AU17	VBATT_PA	-	Main Power Supply (RF Transmit Power Section)	Power	
AU19	VBATT_PA	-	Main Power Supply (RF Transmit Power Section)	Power	
AT20	VBATT_PA	-	Main Power Supply (RF Transmit Power Section)	Power	
A0	GND	-	Ground		
A6	GND	-	Ground		
A12	GND	-	Ground		
A20	GND	-	Ground		
B13	GND	-	Ground		
B15	GND	-	Ground		
B17	GND	-	Ground		
C4	GND	-	Ground		
C6	GND	-	Ground		
D3	GND	-	Ground		
D7	GND	-	Ground		
E18	GND	-	Ground		
F1	GND	-	Ground		
G18	GND	-	Ground		
H19	GND	-	Ground		
L20	GND	-	Ground		
M1	GND	-	Ground		
N0	GND		Ground		
N2	GND		Ground		
N20	GND	-	Ground		
P1	GND	-	Ground		
P3	GND	-	Ground		
R0	GND	-	Ground		
R2	GND	-	Ground		
T0	GND	-	Ground		
T2	GND	-	Ground		
T8	GND		Ground		
T10	GND	-	Ground		
T12	GND	-	Ground		
T18	GND	-	Ground		
U1	GND	-	Ground		
U9	GND	-	Ground		
U11	GND	-	Ground		
V0	GND	-	Ground		
V8	GND	-	Ground		
V10	GND	-	Ground		

PAD	Signal	I/O	Function	Type	COMMENT
V12	GND	-	Ground		
V18	GND	-	Ground		
W1	GND	-	Ground		
W9	GND	-	Ground		
W11	GND	-	Ground		
X0	GND	-	Ground		
X2	GND	-	Ground		
X8	GND	-	Ground		
X10	GND	-	Ground		
X12	GND	-	Ground		
X18	GND	-	Ground		
Y1	GND	-	Ground		
Y9	GND	-	Ground		
Y11	GND	-	Ground		
Y19	GND	-	Ground		
AA0	GND	-	Ground		
AA2	GND	-	Ground		
AA8	GND	-	Ground		
AA10	GND	-	Ground		
AA12	GND	-	Ground		
AB1	GND	-	Ground		
AC0	GND	-	Ground		
AC2	GND	-	Ground		
AE0	GND	-	Ground		
AE2	GND	-	Ground		
AF1	GND	-	Ground		
AG0	GND	-	Ground		
AG2	GND	-	Ground		
AH1	GND	-	Ground		
AJ0	GND	-	Ground		
AJ2	GND	-	Ground		
AK1	GND	-	Ground		
AK17	GND	-	Ground		
AL0	GND	-	Ground		
AL2	GND	-	Ground		
AL18	GND	-	Ground		
AM17	GND	-	Ground		
AM19	GND	-	Ground		
AN0	GND	-	Ground		
AN2	GND	-	Ground		
AN16	GND	-	Ground		

PAD	Signal	I/O	Function	Type	COMMENT
AN18	GND	-	Ground		
AP3	GND	-	Ground		
AP5	GND	-	Ground		
AP7	GND	-	Ground		
AP9	GND	-	Ground		
AP11	GND	-	Ground		
AP13	GND	-	Ground		
AP15	GND	-	Ground		
AR0	GND	-	Ground		
AR2	GND	-	Ground		
AR4	GND	-	Ground		
AR6	GND	-	Ground		
AR8	GND	-	Ground		
AR10	GND	-	Ground		
AR12	GND	-	Ground		
AR14	GND	-	Ground		
AR16	GND	-	Ground		
AS5	GND	-	Ground		
AS7	GND	-	Ground		
AS9	GND	-	Ground		
AS11	GND	-	Ground		
AS13	GND	-	Ground		
AS15	GND	-	Ground		
AT4	GND	-	Ground		
AT6	GND	-	Ground		
AT8	GND	-	Ground		
AT10	GND	-	Ground		
AT12	GND	-	Ground		
AT14	GND	-	Ground		
AT16	GND	-	Ground		
AU1	GND	-	Ground		
AU5	GND	-	Ground		
AU7	GND	-	Ground		
AU11	GND	-	Ground		
AU15	GND	-	Ground		
AV0	GND	-	Ground		
AV8	GND	-	Ground		
AV10	GND	-	Ground		
AV12	GND	-	Ground		
AV14	GND	-	Ground		
AV16	GND	-	Ground		

PAD	Signal	I/O	Function	Type	COMMENT
AV18	GND	-	Ground		
AV20	GND	-	Ground		
ZZ1	GND	-	Ground		
ZZ19	GND	-	Ground		
Reserved					
A2	Reserved	-	Reserved		
A4	Reserved	-	Reserved		
A14	Reserved	-	Reserved		
A16	Reserved	-	Reserved		
B1	Reserved	-	Reserved		
B3	Reserved	-	Reserved		
B5	Reserved	-	Reserved		
B19	Reserved	-	Reserved		
C0	Reserved	-	Reserved		
C2	Reserved	-	Reserved		
C16	Reserved	-	Reserved		
C18	Reserved	-	Reserved		
D1	Reserved	-	Reserved		
D15	Reserved	-	Reserved		
D17	Reserved	-	Reserved		
E0	Reserved	-	Reserved		
E2	Reserved	-	Reserved		
E4	Reserved	-	Reserved		
E8	Reserved	-	Reserved		
E16	Reserved	-	Reserved		
F3	Reserved	-	Reserved		
F5	Reserved	-	Reserved		
F15	Reserved	-	Reserved		
F17	Reserved	-	Reserved		
G0	Reserved	-	Reserved		
G2	Reserved	-	Reserved		
G4	Reserved	-	Reserved		
G6	Reserved	-	Reserved		
G8	Reserved	-	Reserved		
G10	Reserved	-	Reserved		
G12	Reserved	-	Reserved		
G14	Reserved	-	Reserved		
G16	Reserved	-	Reserved		
H1	Reserved	-	Reserved		
H3	Reserved	-	Reserved		
H17	Reserved	-	Reserved		

PAD	Signal	I/O	Function	Type	COMMENT
J0	Reserved	-	Reserved		
J2	Reserved	-	Reserved		
J4	Reserved	-	Reserved		
J16	Reserved	-	Reserved		
J18	Reserved	-	Reserved		
K1	Reserved	-	Reserved		
K3	Reserved	-	Reserved		
K17	Reserved	-	Reserved		
L0	Reserved	-	Reserved		
L2	Reserved	-	Reserved		
L4	Reserved	-	Reserved		
L16	Reserved	-	Reserved		
L18	Reserved	-	Reserved		
M3	Reserved	-	Reserved		
M17	Reserved	-	Reserved		
N4	Reserved	-	Reserved		
N16	Reserved	-	Reserved		
R4	Reserved	-	Reserved		
R16	Reserved	-	Reserved		
R20	Reserved	-	Reserved		
S1	Reserved	-	Reserved		
S3	Reserved	-	Reserved		
S17	Reserved	-	Reserved		
T4	Reserved	-	Reserved		
T16	Reserved	-	Reserved		
T20	Reserved	-	Reserved		
U3	Reserved	-	Reserved		
U17	Reserved	-	Reserved		
V2	Reserved	-	Reserved		
V4	Reserved	-	Reserved		
V16	Reserved	-	Reserved		
V20	Reserved	-	Reserved		
W3	Reserved	-	Reserved		
W17	Reserved	-	Reserved		
X4	Reserved	-	Reserved		
X16	Reserved	-	Reserved		
X20	Reserved	-	Reserved		
Y3	Reserved	-	Reserved		
Y17	Reserved	-	Reserved		
AA4	Reserved	-	Reserved		
AA16	Reserved	-	Reserved		

PAD	Signal	I/O	Function	Type	COMMENT
AA20	Reserved	-	Reserved		
AB3	Reserved	-	Reserved		
AB17	Reserved	-	Reserved		
AC4	Reserved	-	Reserved		
AC16	Reserved	-	Reserved		
AC20	Reserved	-	Reserved		
AD3	Reserved	-	Reserved		
AD17	Reserved	-	Reserved		
AE4	Reserved	-	Reserved		
AE16	Reserved	-	Reserved		
AE20	Reserved	-	Reserved		
AF3	Reserved	-	Reserved		
AF17	Reserved	-	Reserved		
AG4	Reserved	-	Reserved		
AG16	Reserved	-	Reserved		
AG20	Reserved	-	Reserved		
AH3	Reserved	-	Reserved		
AH17	Reserved	-	Reserved		
AJ4	Reserved	-	Reserved		
AJ16	Reserved	-	Reserved		
AJ20	Reserved	-	Reserved		
AK3	Reserved	-	Reserved		
AL4	Reserved	-	Reserved		
AL16	Reserved	-	Reserved		
AL20	Reserved	-	Reserved		
AM3	Reserved	-	Reserved		
AM5	Reserved	-	Reserved		
AM7	Reserved	-	Reserved		
AM9	Reserved	-	Reserved		
AM11	Reserved	-	Reserved		
AM13	Reserved	-	Reserved		
AM15	Reserved	-	Reserved		
AN4	Reserved	-	Reserved		
AN6	Reserved	-	Reserved		
AN14	Reserved	-	Reserved		
AN20	Reserved	-	Reserved		
AP1	Reserved	-	Reserved		
AS3	Reserved	-	Reserved		
AT0	Reserved	-	Reserved		
AT2	Reserved	-	Reserved		
AV2	Reserved	-	Reserved		

PAD	Signal	I/O	Function	Type	COMMENT
AV4	Reserved	-	Reserved		
AV6	Reserved	-	Reserved		
ZZ3	Reserved	-	Reserved		
ZZ5	Reserved	-	Reserved		
ZZ7	Reserved	-	Reserved		
ZZ9	Reserved	-	Reserved		
ZZ11	Reserved	-	Reserved		
ZZ13	Reserved	-	Reserved		
ZZ15	Reserved	-	Reserved		
ZZ17	Reserved	-	Reserved		

NOTE:

When the UART signals are used as the communication port between the Host and the Modem:

- DTR pin must be connected in order to enter LE922A6's power saving mode.
- RI pin must be connected in order to wake the host when a call is coming during sleep mode of host.
- RTS must be connected to GND (on the module side) if flow control is not used

In case that the UART port is not used, all UART signals may be left disconnected

NOTE:

RESERVED pins must not be connected to any circuits in an application board.

NOTE:

If not used, almost all pins must be left disconnected. The only exceptions are the following:

The table below specifies the LE922A6 signals that must be connected even if not used by end application:

PAD	Signal	Notes
AP17,AP19,AR18,AR20,AS17,AS19,AT18,AU17,AU19,AT20	VBATT & VBATT_PA	
A0,A6,A12,A20,B13,B15,B17,C4,C6,D3,D7,E18,F1,G18,H19,L20,M1,N0,N2,N20,P1,P3,R0,R2,T0,T2,T8,T10,T12,T18,U1,U9,U11,V0,V8,V10,V12,V18,W1,W9,W11,X0,X2,X8,X10,X12,X18,Y1,Y9,Y11,Y19,AA0,AA2,AA8,AA10,AA12,AB1,AC0,AC2,AE0,AE2,AF1,AG0,AG2,AH1,AJ0,AJ2,AK1,AK17,AL0,AL2,AL18,AM17,AM19,AN0,AN2,AN16,AN18,AP3,AP5,AP7,AP9,AP11,AP13,AP15,AR0,AR2,AR4,AR6,AR8,AR10,AR12,AR14,AR16,AS5,AS7,AS9,AS11,AS13,AS15,AT4,AT6,AT8,AT10,AT12,AT14,AT16,AU1,AU5,AU7,AU11,AU15,AV0,AV8,AV10,AV12,AV14,AV16,AV18,AV20,ZZ1,ZZ19	GND	
AS1	ON/OFF*	
AN8	RESET_N	If not used should be connected to a Test Point
AN12	SHDN_N	If not used should be connected to a Test Point
D19	USB_D+	If not used should be connected to a Test Point or an USB connector
F19	USB_D-	If not used should be connected to a Test Point or an USB connector
A18	USB_VBUS	If not used should be connected to a Test Point or an USB connector
C20	USB_SS_RX_P	If not used should be connected to a Test Point or an USB connector
E20	USB_SS_RX_M	If not used should be connected to a Test Point or an USB connector
G20	USB_SS_TX_P	If not used should be connected to a Test Point or an USB connector
J20	USB_SS_TX_M	If not used should be connected to a Test Point or an USB connector
AH19	C103/TXD	If not used should be connected to a Test Point
AF19	C104/RXD	If not used should be connected to a Test Point
AA18	C105/RTS	If the flow control is not used it should be connected to GND
AK19	C106/CTS	If not used should be connected to a Test Point
AB19	TXD_AUX	If not used must be connected to a Test Point
AD19	RXD_AUX	If not used must be connected to a Test Point
AD1,AM1	Primary Antenna	If not used should be connected to a 50ohm termination
AU9,AU13	Secondary Antenna	If not used should be connected to

		a 50ohm termination
E4,F3,H3,J2,K3,L2,AN14	For Analysis	Recommend be connected to Test Points for Analysis

3.1.1. LE922A6 LGA Pads Layout

LE922A6 316 pads

Top View

NOTE:

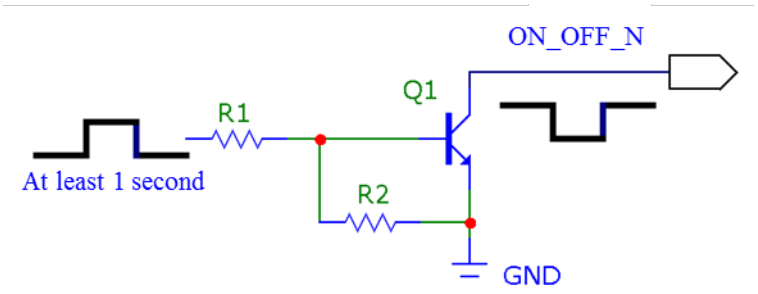
The pin defined as RES must be considered RESERVED and not connected to any pin in the application. The related area on the application must be kept empty.

4. Hardware Commands

4.1. Turning ON the LE922A6

To turn on LE922A6 the pad ON_OFF_N must be asserted low for at least 1 second and then released.

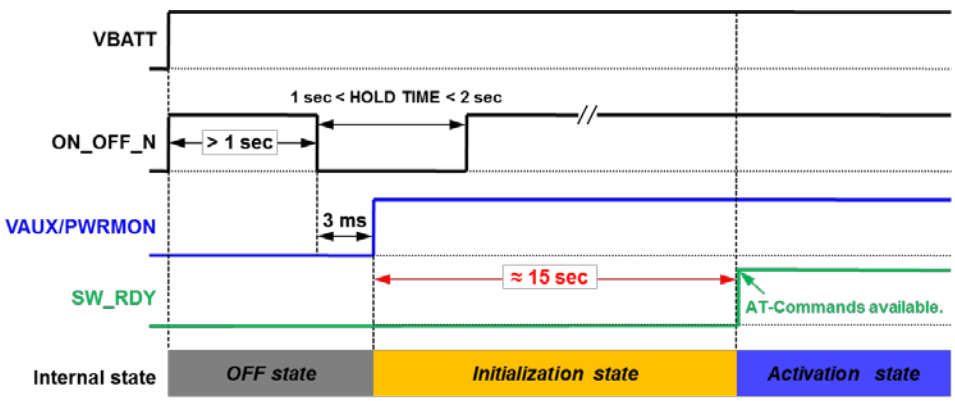
A simple circuit to power on the module is illustrated below:



4.2. Initialization and Activation state

Upon turning on LE922A6 module, The LE922A6 is not activated yet because the boot sequence of LE922A6 is still going on internally. It takes about 15 seconds to complete the initializing the module internally.

For this reason, it is useless to try to access LE922A6 during the Initialization state, as shown below. To reach full stability, The LE922A6 becomes operational (in the activation state) after the SW_RDY goes high.



During the *Initialization state*, any kind of AT-command is not available. DTE must wait for the *Activation state (SW_RDY High)* prior to communicating with LE922A6.

NOTE:

To check if the LE922A6 has powered on, the hardware line VAUX/PWRMON must be monitored. When VAUX/PWRMON goes high, the module has powered on.

NOTE:

Do not use any pull up resistor on the ON_OFF_N line, it is internally pulled up. Using pull up resistor may cause latch-up problems on the LE922A6 power regulator and improper powering on/off of the module. The line ON_OFF_N must be connected only in an open collector configuration.

NOTE:

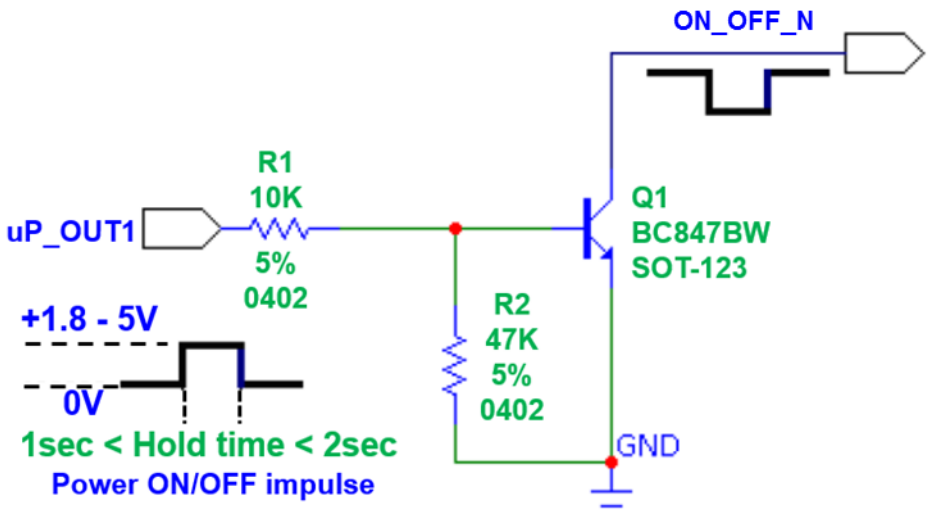
In this document all the lines are inverted. Active low signals are labeled with a name that ends with "_N" or with a bar over the name.

NOTE:

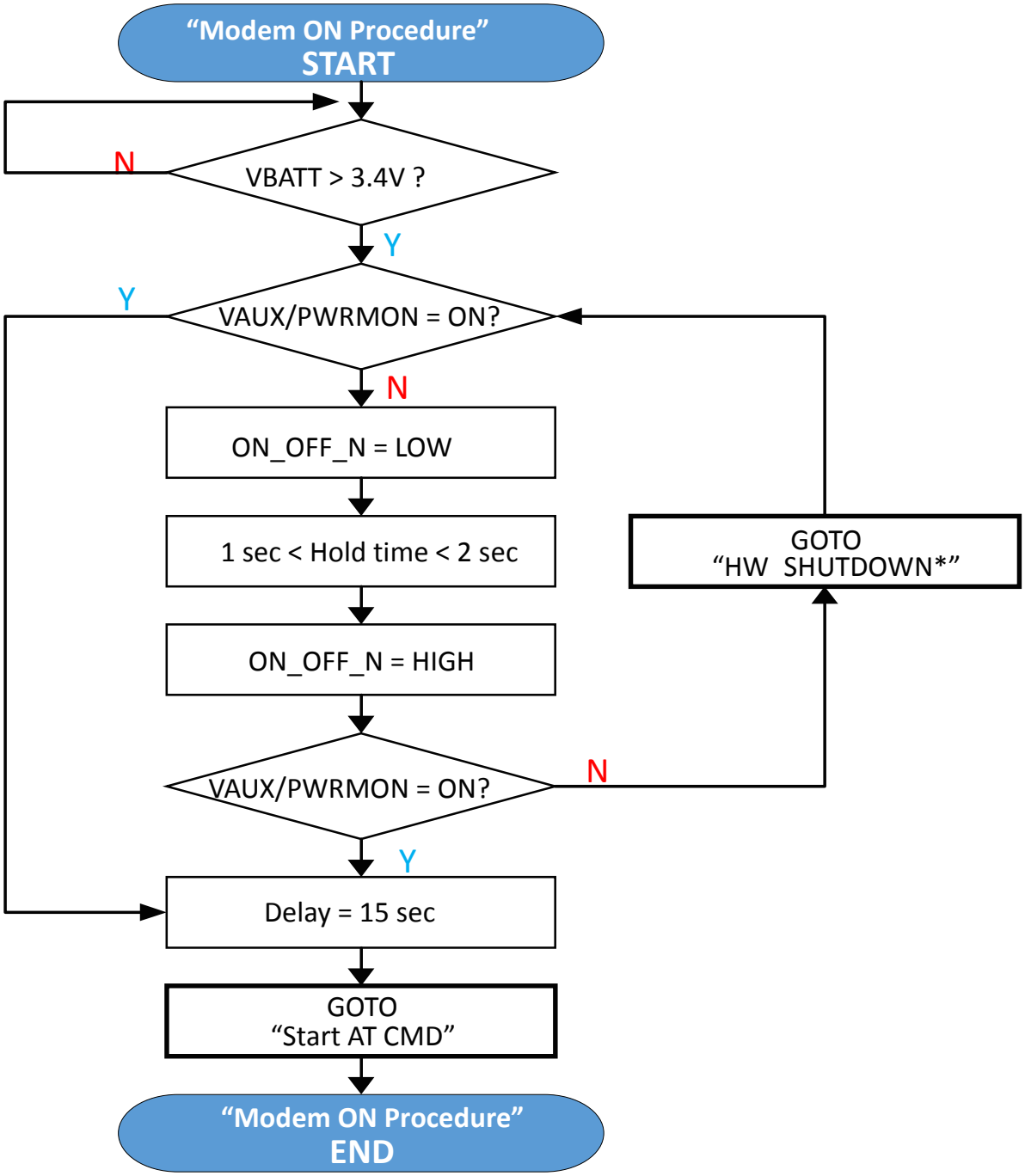
In order to avoid a back-powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the module when it is powered OFF or during an ON/OFF transition.

For example:

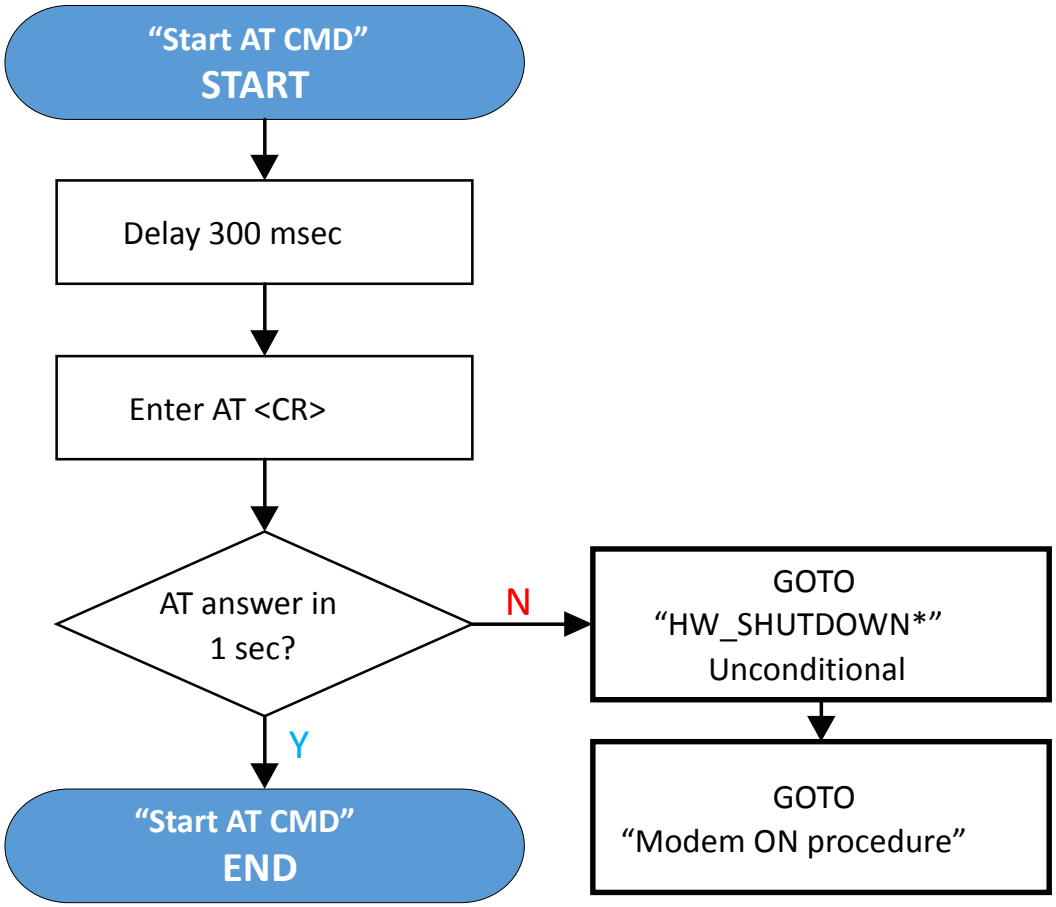
1- Let us assume you need to drive the ON_OFF_N pad with a totem pole output of a +1.8/5 V microcontroller (uP_OUT1):



A flow chart the proper turn on procedure is displayed below:



A flow chart showing the AT commands managing procedure is displayed below:



4.3. RESET and SHUTDOWN the LE922A6

Turning off the device can be done by either of four ways:

- by Software command
- by Hardware shutdown
- by Hardware Unconditional Restart
- by Hardware Unconditional shutdown

When the device is shut down by software command or by hardware shutdown, it issues to the network a detach request, informing the network that the device will not be reachable any more.

TIP:

To check if the device has powered off, hardware line VAUX/PWRMON must be monitored. When VAUX/PWRMON goes low it can be concluded that the device has powered off.

NOTE:

In order to avoid a back-powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the module when it is powered OFF or during an ON/OFF transition.

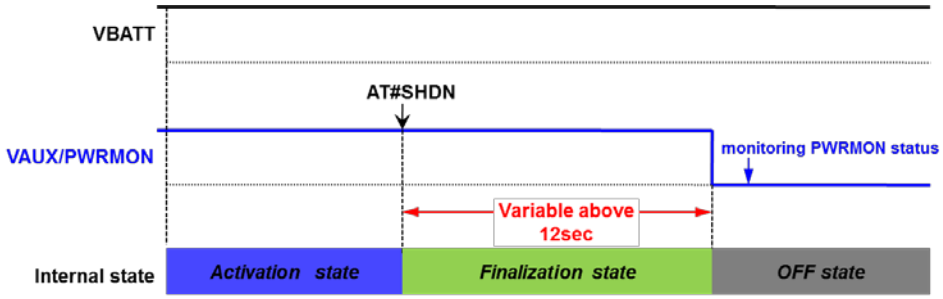
4.3.1. Shutdown by Software Command

LE922A6 can be shut down by a software command.

When a shutdown command is sent, LE922A6 goes into the finalization state and finally will shut down VAUX/PWRMON at the end of this state.

The duration of the finalization state can differ according to the situation in which the LE922A6 is, so a value cannot be defined.

Normally it will take more than 12 seconds since sending a shutdown command till reaching a complete shut down; DTE should monitor the status of VAUX/PWRMON to observe the actual power off.



TIP:

To check whether the device has powered off, hardware line VAUX/PWRMON must be monitored. When VAUX/PWRMON goes low, the device has powered off.

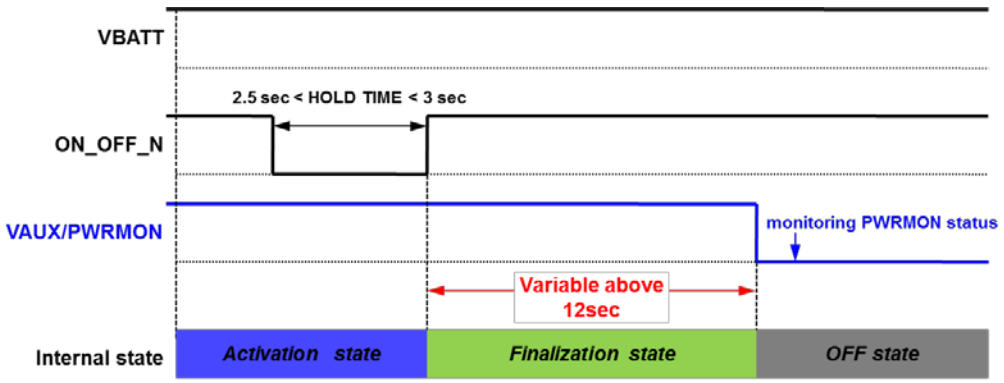
4.3.2. Hardware Shutdown

To turn OFF LE922A6 the pad ON_OFF_N must be asserted low for at least 2 seconds and then released. The same circuitry and timing for the power on must be used.

When the hold time of ON_OFF_N is above 2.5 seconds, LE922A6 goes into the finalization state and finally will shut down VAUX/PWRMON at the end of this state.

The period of the finalization state can differ according to the situation in which the LE922A6 is, so it cannot be fixed definitely.

. Normally it will take more than 12 seconds since sending a shutdown command till reaching a complete shut down; DTE should monitor the status of VAUX/PWRMON to see observe the actual power off.



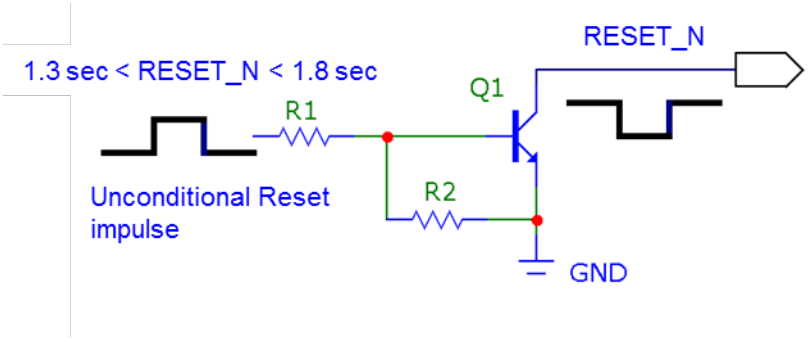
TIP:

To check whether the device has powered off, hardware line VAUX/PWRMON must be monitored. When VAUX/PWRMON goes low, the device has powered off.

4.3.3. Hardware Unconditional Restart (RESET)

To unconditionally restart LE922A6 the pad RESET_N must be tied low for a in the range between 1300 - 1800 milliseconds and then released.

A simple circuit for doing this is shown below:



NOTE:

Do not use any pull up resistor on the RESET_N line or any totem pole digital output. Using pull up resistor may cause latch-up problems on the LE922A6 power regulator and improper functioning of the module. The line RESET_N must be connected only in open collector configuration.

NOTE:

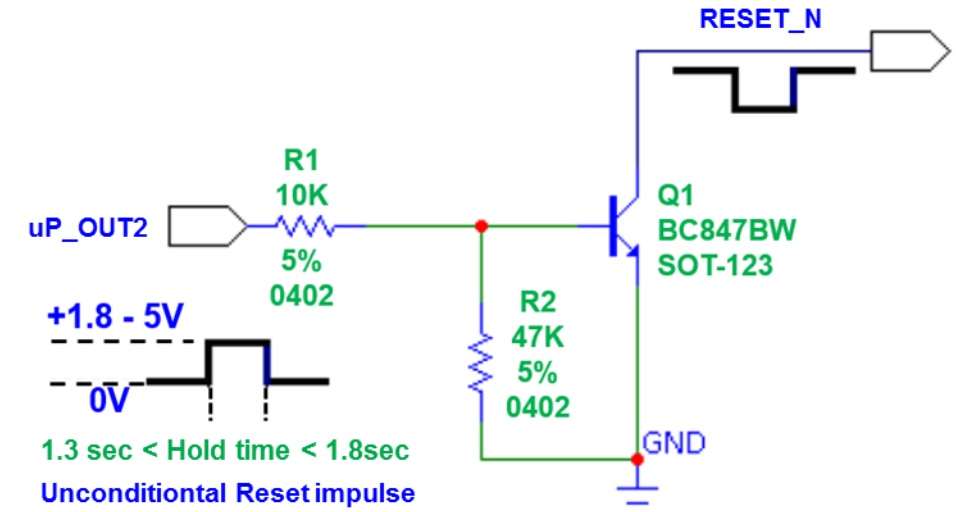
Asserting RESET_N low for period longer than 2000 milliseconds will cause the module to shut down.

TIP:

The unconditional hardware Restart must always be implemented on the boards and the software must use it only as an emergency exit procedure, and **not** as a normal power-off operation

For example:

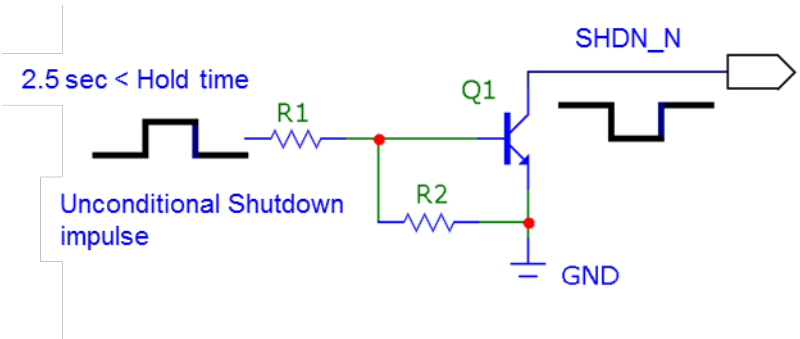
Let us assume that you need to drive the RESET_N pad with a totem pole output of a +1.8/5 V microcontroller (uP_OUT2):



4.3.4. Hardware Unconditional Shutdown

To unconditionally Shutdown LE922A6, the pad SHDN_N must be tied low for at least 2.5 seconds and then released.

A simple circuit for doing this is shown below:



To check whether the device has powered off, hardware line VAUX/PWRMON must be monitored. When VAUX/PWRMON goes low, the device has powered off.

NOTE:

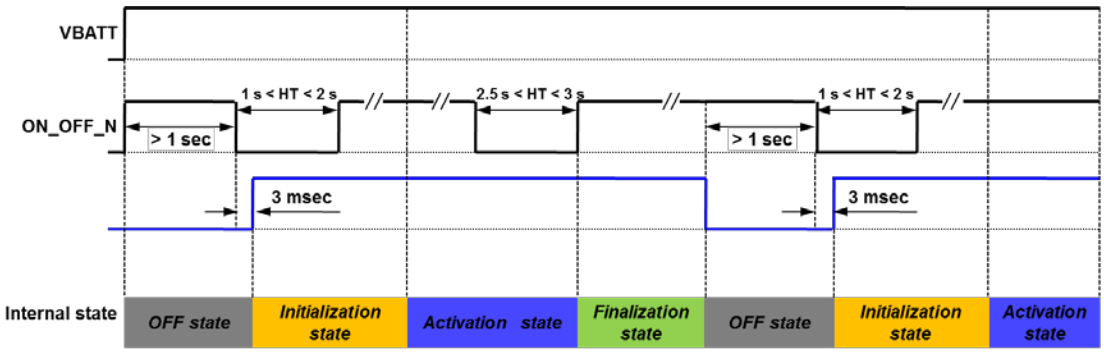
Do not use any pull up resistor on the SHDN_N line or any totem pole digital output. Using pull up resistor may cause latch-up problems on the LE922A6 power regulator and improper functioning of the module. The line SHDN_N must be connected only in open collector configuration.

NOTE:

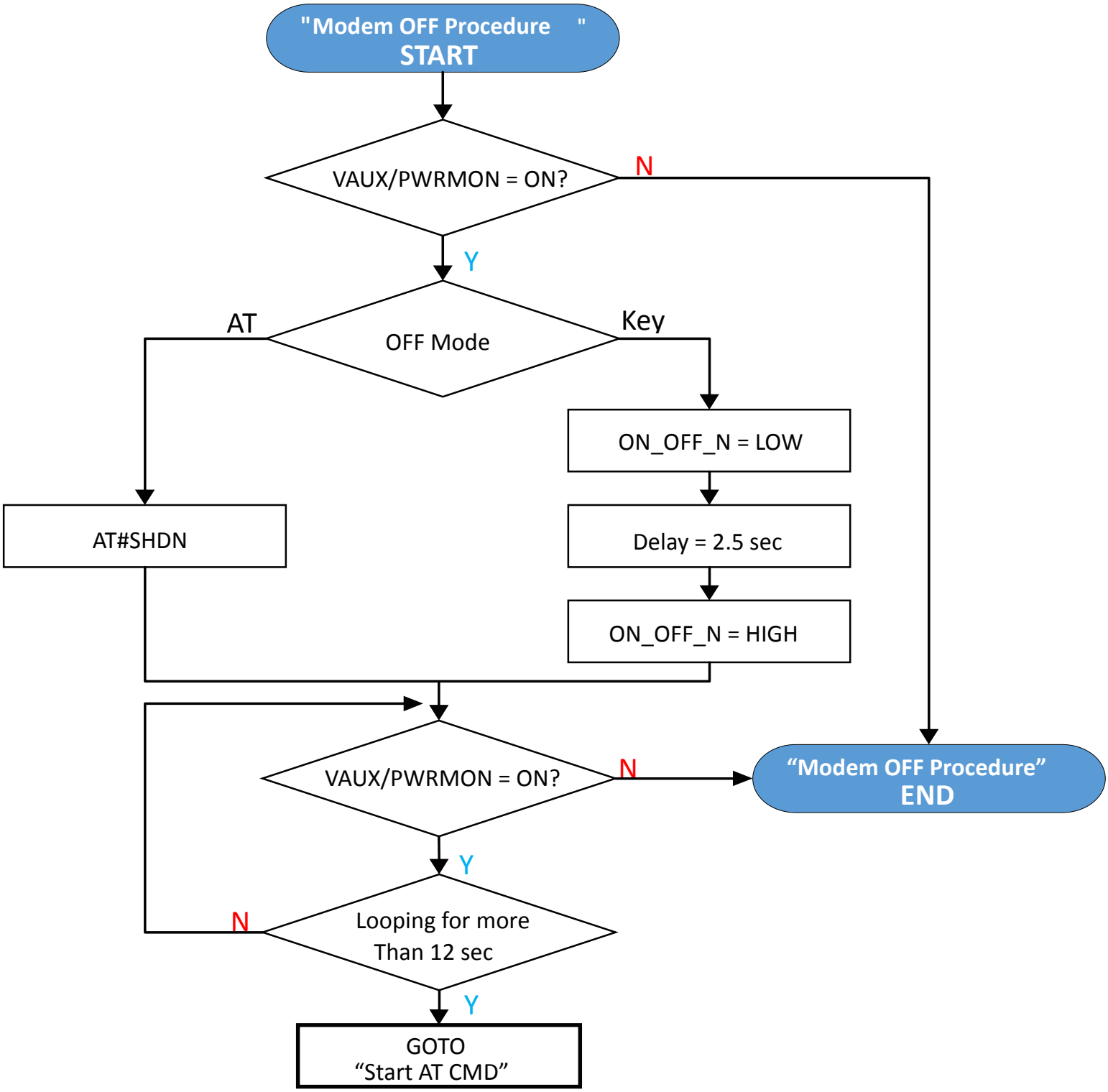
The unconditional hardware SHDN_N must always be implemented on the boards. The software must use it as an **emergency exit** procedure only, and **not** as a normal power-off operation.

4.4. Summary of Turning ON and OFF the module

The chart below describes the overall sequences for Turning ON and OFF.



The following flow chart shows the proper turn off procedure:



4.5. Fast power down

The procedure to power off LE922A6 described in Chapter 4.3 normally takes more than 12 second to de-attach network and make LE922A6 internal filesystem properly closed.

The Fast Power Down feature permits to reduce the current consumption and the time-to-power off to minimum values.

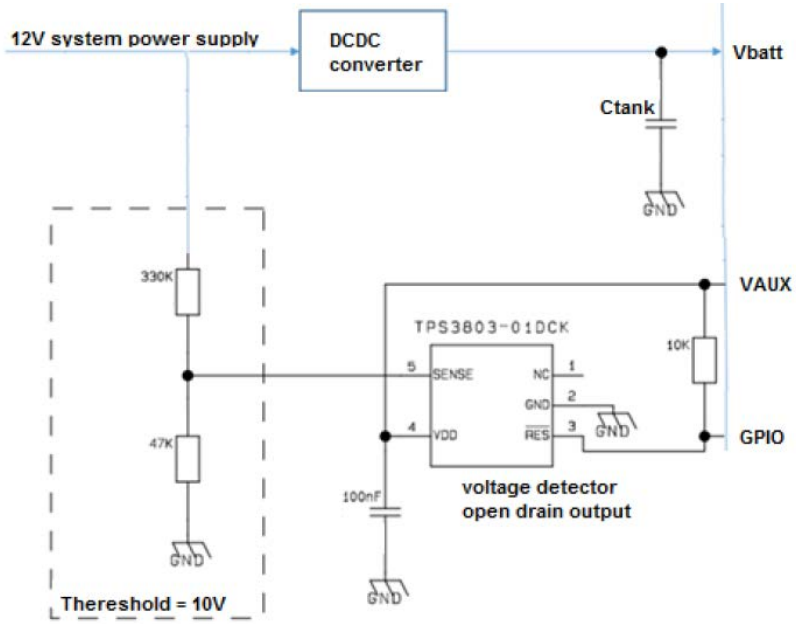
NOTE:

Refer to LE922A6 series AT command reference guide (Fast power down - #FASTSHDN) in order to set up detailed AT command.

4.5.1. Fast Shut Down by Hardware

The module provides an input to give to the FW of the module advance notice that the power source is failing and allow it to prepare for the power failure.

The Fast Power Down can be triggered by configuration of any GPIO. HIGH level to LOW level transition of GPIO forces the fast power down procedure

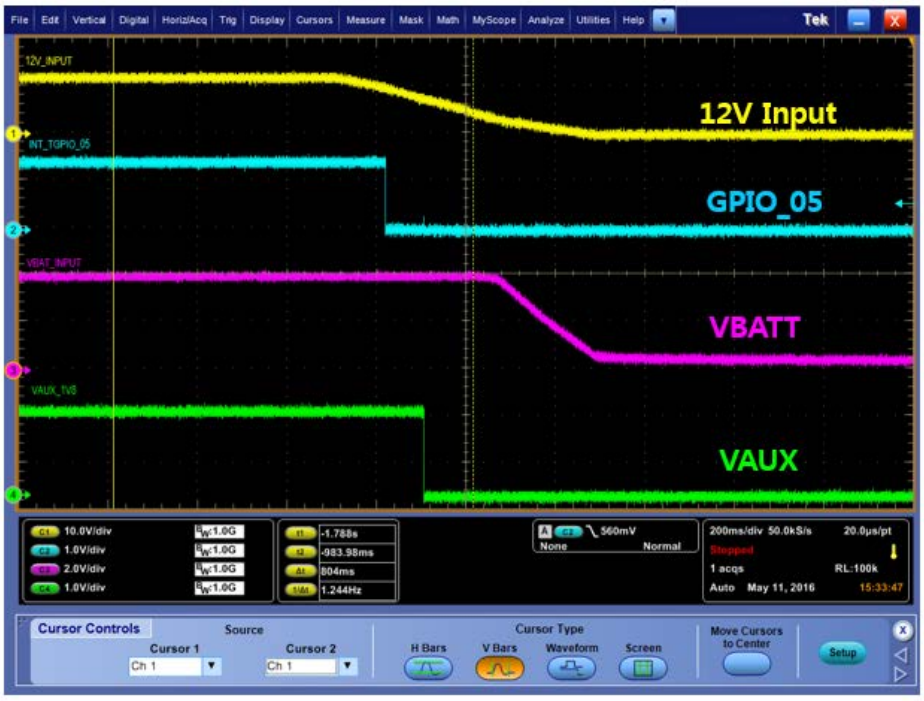


NOTE:

Consider voltage drop under max current conditions when defining the voltage detector threshold in order to avoid unwanted shutdown.

NOTE:

Consider voltage drop under max current conditions when defining the voltage detector threshold in order to avoid unwanted shutdown.



Typical timings are reported in the plot above when testing the example circuit with Ctank=82mF. The capacitor is rated with the following formula:

$$C = I \frac{\Delta t}{\Delta V}$$

Where 820mA is a maximum current consumption during fast shut down procedure, 100ms is the typical time to execute the shutdown and 1V is the minimum voltage margin from threshold of LE922A6 hardware reset.

The Ctank value should be optimized depending on the detection voltage and load current that LE922A6 consumes

NOTE:

Make the same plot during system verification to check timings and voltage levels.

WARNING:

Ctank associated with low ESR requires current limiting feature in DCDC converter to avoid side effect of inrush current.

4.5.2. Fast Shut Down by Software

The Fast Power Down can be triggered directly by AT command.

5. Power Supply

The power supply circuitry and board layout are very important parts of the full product design, with critical impact on the overall product performance. Reading carefully the requirements and the guidelines that follow for making a good and proper design.

5.1. Power Supply Requirements

The LE922A6 power requirements are:

Power Supply	
Nominal Supply Voltage	3.8V
Max Supply Voltage	4.2V
Supply Voltage Range	3.4V– 4.2V

LE922A6 current consumption ***			
Mode		**Average(mA)**	**Mode Description**
SWITCHED OFF			Module supplied but switched Off
Switched Off		30uA	
IDLE mode			Standby mode; no call in progress
AT+CFUN=1	WCDMA	20.0mA	Normal mode; full functionality of the module
	LTE	20.0mA	
AT+CFUN=4		17mA	Disabled TX and RX; modules is not registered on the network
	WCDMA	2.4mA	DRx6
		2.0mA	DRx7
		1.8mA	DRx8
		1.5mA	DRx9
	LTE	6.2mA	Paging cycle #32 frames (0.32 sec DRx cycle)
		3.6mA	Paging cycle #64 frames (0.64 sec DRx cycle)
		2.5mA	Paging cycle #128 frames (1.28 sec DRx cycle)
		2.0mA	Paging cycle #256 frames (2.56 sec DRx cycle)
Operative mode (LTE)			
LTE (0dBm)		140mA	LTE data call channel BW 5MHz,RB=1, TX = 0dBm)
LTE (23dBm)		740mA	LTE data call (channel BW 5MHz,RB=1, TX = 23dBm)
Operative mode (WCDMA)			
WCDMA Voice		670mA	WCDMA voice call (TX = 23dBm)
WCDMA HSDPA (0dBm)		120mA	WCDMA data call (Cat 6/9, TX = 0dBm, Max Throughput)
WCDMA HSDPA (23dBm)		610mA	WCDMA data call (Cat 6/9, TX = 23dBm, Max Throughput)

LE922A6 current consumption to CAT6 Throughput data ***			
Mode	Tx Power	Average(mA)	Mode Description
LTE	0dBm	390mA	2 DL CA 300/50 Mbps , 20 MHz + 20MHz BW
		290mA	2 DL CA 150/25 Mbps , 10 MHz + 10MHz BW
		250mA	150/50 Mbps , 20 MHz BW
	20dBm	780mA	2 DL CA 300/50 Mbps , 20 MHz + 20MHz BW
		700mA	2 DL CA 150/25 Mbps , 10 MHz + 10MHz BW
		650mA	150/50 Mbps , 20 MHz BW
	Max power (21dBm)**	820mA	2 DL CA 300/50 Mbps , 20 MHz + 20MHz BW
		720mA	2 DL CA 150/25 Mbps , 10 MHz + 10MHz BW
		670mA	150/50 Mbps , 20 MHz BW

* Worst/best case depends on network configuration and is not under module control.
** Applied MPR –2dB 16-QAM full RB
*** 3.8 Voltage / Room temperature

TIP:

Differences in measurement technique, equipment, or temperature can cause variations in current consumption measurements

TIP:

The electrical design for the Power supply must be made in a way ensuring that it will be capable of a peak current output of at least 2A.

5.2. General Design Rules

The principal guidelines for the Power Supply Design embrace three different design steps:

- electrical design
- thermal design
- PCB layout

5.2.1. Electrical Design Guidelines

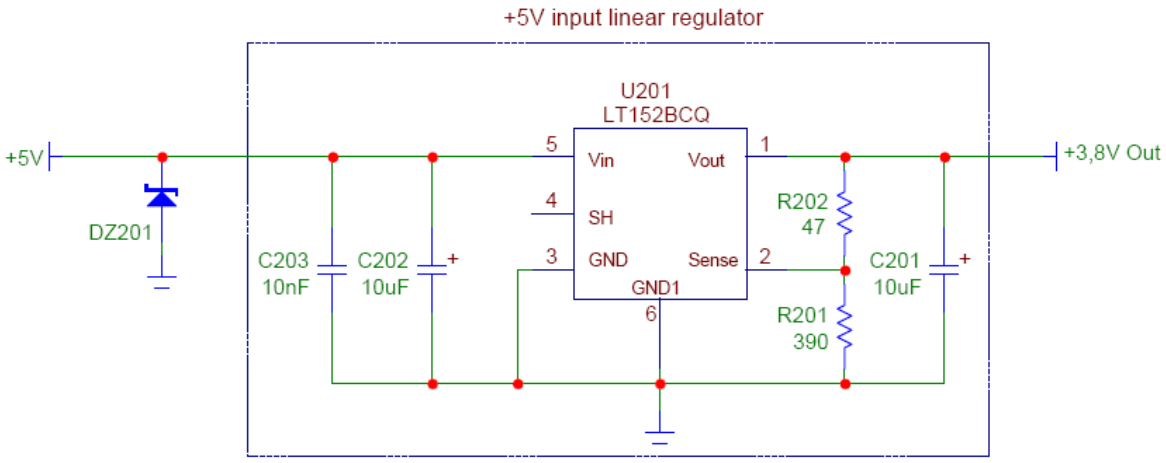
The electrical design of the power supply depends strongly on the power source where this power is drained. We will distinguish them into three categories:

- +5V input (typically PC internal regulator output)
- +12V input (typically automotive)
- Battery

5.2.1.1. + 5V Input Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, hence there is not a big difference between the input source and the desired output and a linear regulator can be used. A switching power supply will not be suitable because of the low drop-out requirements.
- When using a linear regulator, a proper heat sink must be provided in order to dissipate the power generated.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks close to LE922A6, a 100µF tantalum capacitor is usually suitable.
- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- A protection diode must be inserted close to the power input, in order to protect LE922A6 from power polarity inversion.

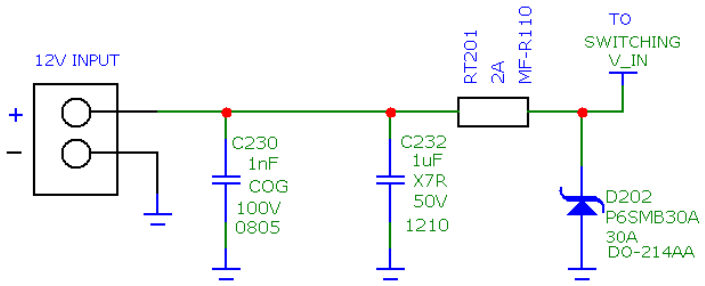
An example of linear regulator with 5V input is:

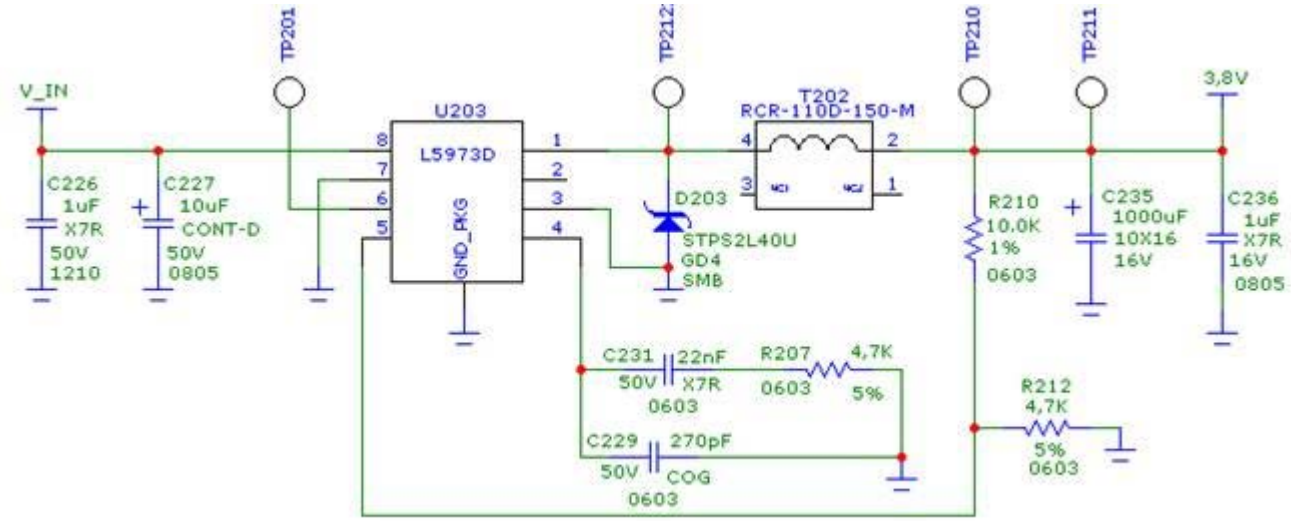


5.2.1.2. + 12V Input Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, hence due to the big difference between the input source and the desired output, a linear regulator is unsuitable and must not be used. A switching power supply will be preferable because of its better efficiency especially with the 2A peak current load represented by LE922A6.
- When using a switching regulator, a 500 kHz or more switching frequency regulator is preferable because of its smaller inductor size and its faster transient response. This allows the regulator to respond quickly to the current peaks absorption.
- In any case, the frequency and switching design selection is related to the application to be developed due to the fact the switching frequency could also generate EMC interference.
- For car batteries (lead-acid accumulators) the input voltage can rise up to 15.8V and this must be kept in mind when choosing components: all components in the power supply must withstand this voltage.
- A bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks. A 100µF tantalum capacitor is usually suitable.
- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- For automotive applications a spike protection diode must be inserted close to the power input, in order to clean the supply of spikes.
- A protection diode must be inserted close to the power input, in order to protect LE922A6 from power polarity inversion. This can be the same diode as for spike protection.

An example of switching regulator with 12V input is shown in the below schematic (it is split in 2 parts):





Switching regulator

5.2.1.3. Battery Source Power Supply Design Guidelines

- The desired nominal output for the power supply is 3.8V and the maximum allowed voltage is 4.2V, hence a single 3.7V Li-Ion cell battery type is suited for supplying the power to the Telit LE922A6 module. The three cells Ni/Cd or Ni/MH 3.6 V Nom. battery types or 4V PB types must not be used directly since their maximum voltage can rise over the absolute maximum voltage for LE922A6 damage it.

NOTE:

Do not use any Ni-Cd, Ni-MH, and Pb battery types directly connected with LE922A6. Their use can lead to overvoltage on LE922A6 and damage it. Use only Li-Ion battery types.

- A bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks; a 100µF tantalum capacitor is usually suitable.
- Make sure the low ESR capacitor (usually a tantalum one) is rated at least 10V.
- A protection diode must be inserted close to the power input, in order to protect LE922A6 from power polarity inversion. Otherwise the battery connector must be done in a way to avoid polarity inversions when connecting the battery.
- The battery capacity must be at least 500mAh in order to withstand the current peaks of 2A; the suggested capacity is from 500mAh to 1000mAh.

5.2.2. Thermal Design Guidelines

The thermal design for the power supply heat sink must be done with the following specifications:

- Average current consumption during LTE 2 DL Max throughput @PWR level max in LE922A6 : 820 mA

NOTE:

The average consumption during transmissions depends on the power level at which the device is requested to transmit via the network. The average current consumption hence varies significantly.

In the LTE mode, since LE922A6 emits RF signals continuously during transmission, you must pay special attention how to dissipate the heat generated.

The current consumption will be up to about 820 mA in 2DL Max throughput in LTE continuously at the maximum TX output power 21 dBm. Thus you must arrange on the PCB used to mount LE922A6 that the area under LE922A6 is as large as possible. You must mount LE922A6 on the large ground area of your application board and make many ground vias to dissipate the heat.

5.2.3. Power Supply PCB Layout Guidelines

As seen in the electrical design guidelines, the power supply must have a low ESR capacitor on the output to cut the current peaks and a protection diode on the input to protect the supply from spikes and polarity inversion. The placement of these components is crucial for the correct operation of the circuitry. A misplaced component can be useless or can even decrease the power supply performances.

- The bypass low ESR capacitor must be placed close to the Telit LE922A6 power input pads, or in the case the power supply is a switching type, it can be placed close to the inductor to cut the ripple as long as the PCB trace from the capacitor to LE922A6 is wide enough to ensure a drop-less connection even during the 2A current peaks.
- The protection diode must be placed close to the input connector where the power source is drained.
- The PCB traces from the input connector to the power regulator IC must be wide enough to ensure no voltage drops occur during the 2A current peaks. Note that this is not done to save power loss but especially to avoid the voltage drops on the power line at the current peaks frequency of 216 Hz that will reflect on all the components connected to that supply (also introducing the noise floor at the burst base frequency.) For this reason while a voltage drop of 300-400 mV may be acceptable from the power loss point of view, the same voltage drop may not be acceptable from the noise point of view. If your application does not have audio

interface but only uses the data feature of the Telit LE922A6, then this noise is not so disturbing and power supply layout design can be more forgiving.

- The PCB traces to LE922A6 and the bypass capacitor must be wide enough to ensure no significant voltage drops occur when the 2A current peaks are absorbed. This is needed for the same above-mentioned reasons. Try to keep this trace as short as possible.
- The PCB traces connecting the switching output to the inductor and the switching diode must be kept as short as possible by placing the inductor and the diode very close to the power switching IC (only for switching power supply). This is done in order to reduce the radiated field (noise) at the switching frequency (usually 100-500 kHz).
- The use of a good common ground plane is suggested.
- The placement of the power supply on the board must be done in a way to guarantee that the high current return paths in the ground plane are not overlapping any noise sensitive circuitry such as the microphone amplifier/buffer or earphone amplifier.
- The power supply input cables must be kept separate from noise sensitive lines such as microphone/earphone cables.

6. Antenna(s)

The antenna connection and board layout design are the most important parts in the full product design and they strongly reflect on the product's overall performance. Read carefully and follow the requirements and the guidelines for a good and proper design.

6.1. WCDMA/LTE Antenna Requirements

The antenna for a Telit LE922A6 device must fulfill the following requirements:

WCDMA/ LTE Antenna Requirements	
Frequency range	Depending on frequency band(s) provided by the network operator, the customer must use the most suitable antenna for that/those band(s)
Gain	Gain < 3dBi
Impedance	50 Ohm
Input power	> 24dBm Average power in WCDMA & LTE
VSWR absolute max	<= 10:1
VSWR recommended	<= 2:1

When using the Telit LE922A6, since there's no antenna connector on the module, the antenna must be connected to the LE922A6 antenna pad (AD1 & AM1) by means of a transmission line implemented on the PCB.

In the case that the antenna is not directly connected to the antenna pad of the LE922A6, then a PCB line is required in order to connect with it or with its connector.

The table below shows a primary antenna pad of the LE922A6.

Primary Antenna Pad	AD1	AM1
LE922A6-A1	LTE B1, B3, B28 / WCDMA B1, B8	LTE B7, B40
LE922A6-E1	LTE B3, B20	LTE B7
LE922A6-E2	LTE B8, B20, B28	LTE B3, B7, B32

6.2. WCDMA/LTE Antenna – PCB line Guidelines

- Make sure that the transmission line's characteristic impedance is 50ohm.
- Keep the line on the PCB as short as possible since the antenna line loss should be less than around 0.3dB.

- Line geometry should have uniform characteristics, constant cross section, avoid meanders and abrupt curves.
- Any suitable geometry/structure can be used for implementing the printed transmission line affecting the antenna.
- If a Ground plane is required in the line geometry, that plane must be continuous and sufficiently extended so the geometry can be as similar as possible to the related canonical model.
- Keep, if possible, at least one layer of the PCB used only for the Ground plane; if possible, use this layer as reference Ground plane for the transmission line.
- It is wise to surround (on both sides) the PCB transmission line with Ground. Avoid having other signal tracks facing directly the antenna line track.
- Avoid crossing any un-shielded transmission line footprint with other tracks on different layers.
- The Ground surrounding the antenna line on the PCB must be strictly connected to the main Ground plane by means of via-holes (once per 2mm at least) placed close to the ground edges facing the line track.
- Place EM-noisy devices as far as possible from LE922A6 antenna line.
- Keep the antenna line far away from the LE922A6 power supply lines.
- If EM-noisy devices are present on the PCB hosting the LE922A6 such as fast switching ICs, take care to shield them with a metal frame cover.
- If EM-noisy devices are not present around the line, using geometries like Micro strip or Grounded Coplanar Waveguide is preferred since they typically ensure less attenuation compared to a Strip line having the same length.

This transmission line shall fulfill the following requirements:

Antenna Line on PCB Requirements	
Characteristic Impedance	50Ohm
Max Attenuation	0.3dB
Coupling with other signals shall be avoided	
Cold End (Ground Plane) of antenna shall be equipotential to the LE922A6 ground pads	

Furthermore if the device is developed for the US and/or Canada market, it must comply with the FCC and/or IC approval requirements:

This device is to be used only for mobile and fixed application. The antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter. End-Users must be provided with transmitter operation conditions for satisfying RF exposure compliance. OEM integrators must ensure that the end user has no manual instructions to remove or install the LE922A6 module. Antennas used for this OEM module must not exceed 3dBi gain for mobile and fixed operating configurations.

6.3. WCDMA/LTE Antenna – Installation Guidelines

- Install the antenna in a location with access to the network radio signal.
- The antenna must be installed such that it provides a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter;
- The antenna must not be installed inside metal cases;
- The antenna must also be installed according to the antenna manufacturer's instructions.

6.4. Secondary Antenna Requirements

This product includes an input for a second RX antenna to improve the radio sensitivity. The function is called Secondary Antenna.

WCDMA/ LTE Antenna Requirements	
Frequency range	Depending on frequency band(s) provided by the network operator, the customer shall use the most suitable antenna for that/those band(s)
Impedance	50 Ohm
VSWR recommended	<= 2:1

When using the Telit LE922A6, since there is no antenna connector on the module, the antenna must be connected to the LE922A6 antenna pad (AU9 & AU13) by means of a transmission line implemented on the PCB.

In the case that the antenna is not directly connected at the antenna pad of the LE922A6 then a PCB line is required in order to connect with it or with its connector.

The table below shows a secondary antenna pad of the LE922A6.

Secondary Antenna Pad	AU9	AU13
LE922A6-A1	LTE B1, B3, B28 / WCDMA B1, B8	LTE B7, B40
LE922A6-E1	LTE B3, B20	LTE B7
LE922A6-E2	LTE B8, B20, B28	LTE B3, B7, B32

The second Rx antenna should not be located in close vicinity of the main antenna. In order to improve Secondary antenna Gain and Isolation and to reduce mutual interaction, the two antennas should be located at the maximum reciprocal distance possible, taking into

consideration the available space within the application. For the same reason, the Rx antenna should also be cross-polarized with respect to the main antenna.

Isolation between main antenna and Rx antenna must be at least 10 dB in all uplink frequency bands.

Envelope Correlation Coefficient (ECC) value should be as close as possible to zero, for best secondary antenna performance. ECC values below 0.5 on all frequency bands are recommended.

7. Logic Level Specifications

Where not specifically stated, all the interface circuits operate at 1.8V CMOS logic levels.

The following table shows the logic level specifications used in the Telit LE922A6 interface circuits:

NOTE:

Do not connect LE922A6's digital logic signal directly to OEM's digital logic signal with a level higher than 2.7V for 1.8V CMOS signals.

For 1.8V CMOS signals:

Absolute Maximum Ratings - Not Functional

Parameter	LE922A6	
	Min	Max
Input level on any digital pin when on	-0.3V	+2.3V
Input voltage on analog pins when on	-0.3V	+2.3 V

Operating Range - Interface levels (1.8V CMOS)

Level	LE922A6	
	Min	Max
Input high level	1.26V	2.1V
Input low level	-0.3V	0.36V
Output high level	1.44V	1.8V
Output low level	0V	0.4V

8. USB Port

The LE922A6 module includes a Universal Serial Bus (USB) transceiver, which operates at USB high-speed (480Mbits/sec). It can also operate with USB full-speed (12Mbits/sec) hosts

It is compliant with the USB 2.0 specification and can be used control and data transfers as well as for diagnostic monitoring and firmware update. In fact firmware update by the host is only possible via USB and not possible via UART. The reason is that Telit consider it impractical to transfer firmware binaries exceeding 100Mb via UART.

The USB port on the Telit LE922A6 is typically the main interface between the module and OEM hardware.

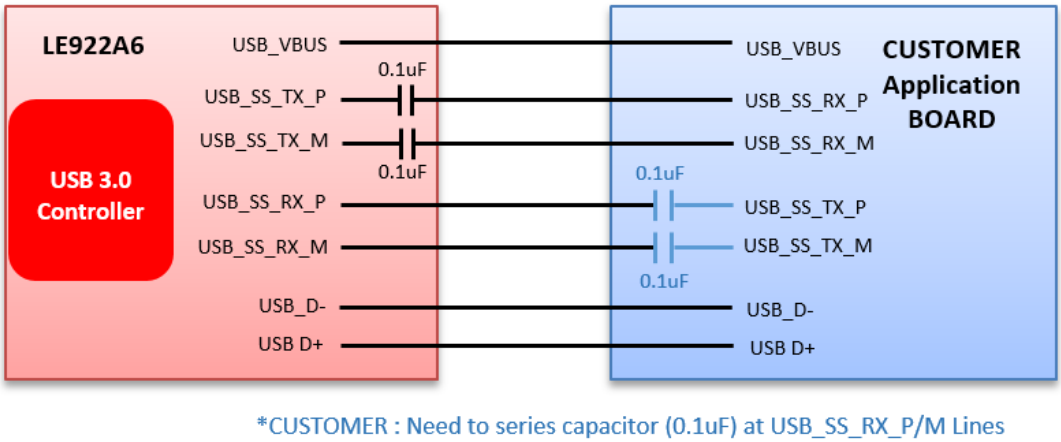
The USB_DPLUS and USB_DMINUS signals have a clock rate of 480MHz. The signal traces should be routed carefully. Trace lengths, number of vias and capacitive loading should be minimized, additional ESD protection must be carefully evaluated. The impedance value should be as close as possible to 90 Ohms differential.

In addition, the LE922A6 supports USB3.0.

But, the LE922A6 does not supports both USB 2.0 and USB 3.0 at the same time.

For AC coupling, USB 3.0 needs series capacitors on the TX lines in both directions. In order to interface USB3.0 with an application board of customer, a customer must install series capacitors (0.1uF) on USB_SS_RX_P/M lines of the LE922A6. The series capacitors (0.1uF) of USB_SS_TX_P/M lines are already applied to the inside LE922A6.

The USB 3.0 interface suggested connection is the following:



Connection for USB3.0

The table below describes the USB interface signals:

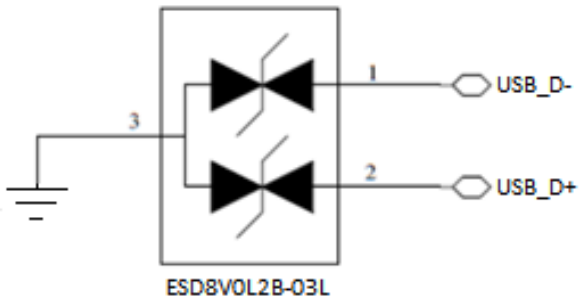
Signal	Pad No.	Usage
USB_VBUS	A18	Power sense for the internal USB transceiver. Acceptable input voltage range 2.2V – 5.25V @ max 5mA consumption
USB_D-	F19	Minus (-) line of the differential, bi-directional USB signal to/from the peripheral device
USB D+	D19	Plus (+) line of the differential, bi-directional USB signal to/from the peripheral device
USB_SS_RX_P	C20	USB 3.0 super-speed receive – plus
USB_SS_RX_M	E20	USB 3.0 super-speed receive – minus
USB_SS_TX_P	G20	USB 3.0 super-speed transmit – plus
USB_SS_TX_M	J20	USB 3.0 super-speed transmit – minus

NOTE:

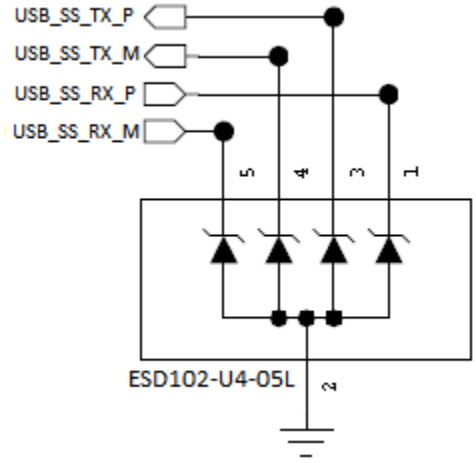
Even if USB communication is not used, it is still highly recommended to place an optional USB connector in the application board.

USB physical communication is needed to SW update

In case there is a need to add an ESD protection the suggested connection is the following:



ESD Protection for USB2.0



ESD Protection for USB3.0

9. Serial Ports

The serial port on the Telit LE922A6 is typically a secondary interface between the module and OEM hardware.

Two serial ports are available on the module:

- MODEM SERIAL PORT 1(Main)
- MODEM SERIAL PORT 2 (Auxiliary)

Several configurations can be designed for the serial port on the OEM hardware.

The most common are:

- RS232 PC com port;
- Microcontroller UART @ 1.8V (Universal Asynchronous Receive Transmit) ;
- Microcontroller UART @ 5V or other voltages different from 1.8V.

Depending on the type of serial port on the OEM hardware, a level translator circuit may be needed to make the system operate. The only configuration that does not need a level translation is the 1.8V UART.

The serial port 1 on LE922A6 is a +1.8V UART with all the 7 RS232 signals. It differs from the PC-RS232 in signal polarity (RS232 is reversed) and levels.

The Serial port 2 is a +1.8V Auxiliary UART.

The levels for LE922A6 UART are the CMOS levels:

Absolute Maximum Ratings -Not Functional

Parameter	LE922A6	
	Min	Max
Input level on any digital pin when on	-0.3V	+2.3V
Input voltage on analog pins when on	-0.3V	+2.3V

Operating Range - Interface levels

Level	LE922A6	
	Min	Max
Input high level	1.26V	2.1V
Input low level	-0.3V	0.36V
Output high level	1.44V	1.8V
Output low level	0V	0.4V

9.1. Modem Serial Port 1

Serial port 1 on the LE922A6 is a +1.8V UART with all 7 RS232 signals.

It differs from the PC-RS232 in the signal polarity (RS232 is reversed) and levels.

RS232 Pin Number	Signal	Pad Number	Name	Usage
1	DCD - dcd_uart	AE18	Data Carrier Detect	Output from the LE922A6 that indicates the carrier presence
2	RXD - Tx_uart	AF19	Transmit line *see Note	Output transmit line of the LE922A6 UART
3	TXD - Rx_uart	AH19	Receive line *see Note	Input receive of the LE922A6 UART
4	DTR - dtr_uart	AC18	Data Terminal Ready	Input to the LE922A6 that controls the DTE READY condition
5	GND	A6, A12, B13, B15….	Ground	Ground
6	DSR - dsr_uart	AG18	Data Set Ready	Output from the LE922A6 that indicates the module is ready
7	RTS - rts_uart	AA18	Request to Send	Input to the LE922A6 that controls the Hardware flow control
8	CTS - cts_uart	AK19	Clear to Send	Output from the LE922A6 that controls the Hardware flow control
9	RI - ri_uart	AJ18	Ring Indicator	Output from the LE922A6 that indicates the Incoming call condition

NOTE:

In order to avoid a back-powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the module when it is powered OFF or during an ON/OFF transition.

TIP:

For minimum implementations, only the TXD and RXD lines need be connected, the other lines can be left open provided a software flow control is implemented.

NOTE:

According to RX/TX signal names are referred to the application side, therefore on the LE922A6 side these signal are in the opposite direction: TXD on the application side will be connected to the receive line (here named TXD/ rx_uart) of the LE922A6 serial port and vice versa for RX.

9.2. Modem Serial Port 2

Serial port 2 on the LE922A6 is a +1.8V UART with only the RX and TX signals.

The signals of the LE922A6 serial port are:

PAD	Signal	I/O	Function	Type	COMMENT
AB19	TXD_AUX	O	Auxiliary UART (TX Data to DTE)	1.8V	
AD19	RXD_AUX	I	Auxiliary UART (RX Data to DTE)	1.8V	

NOTE:

In order to avoid a back-powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the module when it is powered OFF or during an ON/OFF transition.

9.3. RS232 Level Translation

In order to interface the Telit LE922A6 with a PC com port or a RS232 (EIA/TIA-232) application a level translator is required. This level translator must:

- Invert the electrical signal in both directions;
- Change the level from 0/1.8V to +15/-15V.

Actually, the RS232 UART 16450, 16550, 16650 & 16750 chipsets accept signals with lower levels on the RS232 side (EIA/TIA-562), allowing a lower voltage-multiplying ratio on the level translator. Note that the negative signal voltage must be less than 0V and hence some sort of level translation is always required.

The simplest way to translate the levels and invert the signal is by using a single chip level translator. There are a multitude of them, differing in the number of drivers and receivers and in the levels (be sure to get a true RS232 level translator not a RS485 or other standards).

By convention the driver is the level translator from the 0-1.8V UART to the RS232 level. The receiver is the translator from the RS232 level to 0-1.8V UART.

In order to translate the whole set of control lines of the UART you will need:

- 5 drivers
- 3 receivers

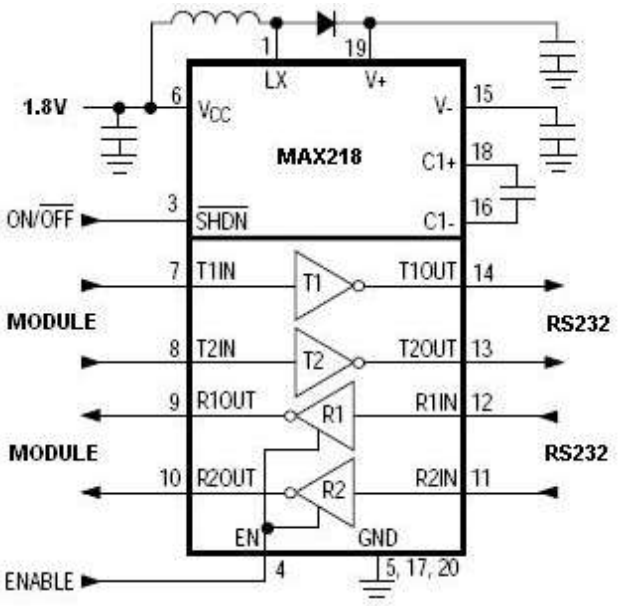
NOTE:

The digital input lines operating at 1.8V CMOS have an absolute maximum input voltage of 2.7V; therefore the level translator IC shall not be powered by the +3.8V supply of the module. Instead, it must be powered from a +1.8V (dedicated) power supply.

This is because in this way the level translator IC outputs on the module side (i.e. LE922A6 inputs) will operate at +3.8V interface levels, damaging the module inputs.

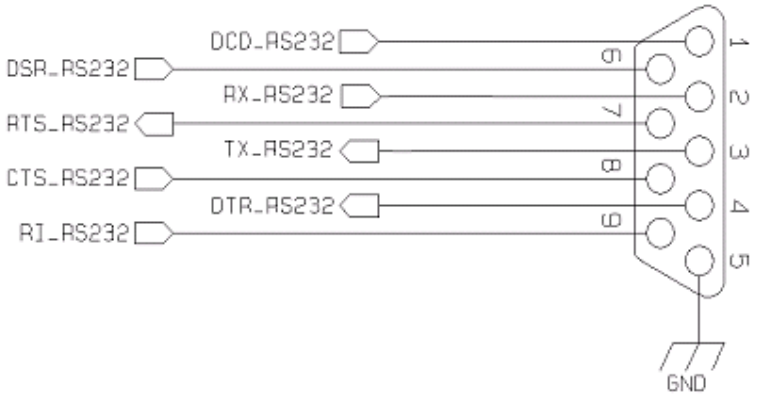
An example of RS232 level adaption circuitry could be accomplished using a MAXIM transceiver (MAX218).

In this case the chipset is capable of translating directly from 1.8V to the RS232 levels (Example on 4 signals only).



NOTE:
In this case the length of the lines on the application must be taken into account to avoid problems in the case of High-speed rates on RS232.

The RS232 serial port lines are usually connected to a DB9 connector with the following layout: signal names and directions are named and defined from the DTE point of view



10. Peripheral Ports

In addition to Telit LE922A6 serial ports, the LE922A6 supports the following peripheral ports:

- SPI – Serial Peripheral Interface
- I2C – Inter-integrated circuit
- SDIO – Secure Digital I/O

10.1. SPI – Serial Peripheral Interface

The LE922A6 supports SPI. And its characteristic is in the following:

- Master Mode only
- 1.8V CMOS level
- Up to 26MHz clock rate

NOTE:

SPI is supported only on the Linux side.

LE922A6 can support Master mode only, and can't be configured as slave mode.

PAD	Signal	I/O	Function	Type	COMMENT
P19	SPI_CLK	O	SPI Clock output	1.8V	
M19	SPI_MISO	I	SPI data Master Input Slave output	1.8V	
K19	SPI_MOSI	O	SPI data Master Output Slave input	1.8V	
N18	SPI_CS	O	SPI Chip select output	1.8V	

10.2. I2C - Inter-integrated circuit

The LE922A6 I2C is an alternate function of our GPIO 1-10 pins.

Any GPIO can be configured as SCL and SDA

Available only from Modem side as SW emulation of I2C on GPIO lines.

LE922A6 supports I2C Master Mode only.

NOTE:

I2C is supported only on from Modem side as SW emulation of I2C on GPIO lines.

Refer to LE922A6 AT SW manual for command settings

11. Audio Section Overview

The LE922A6 module support only digital audio interfaces.

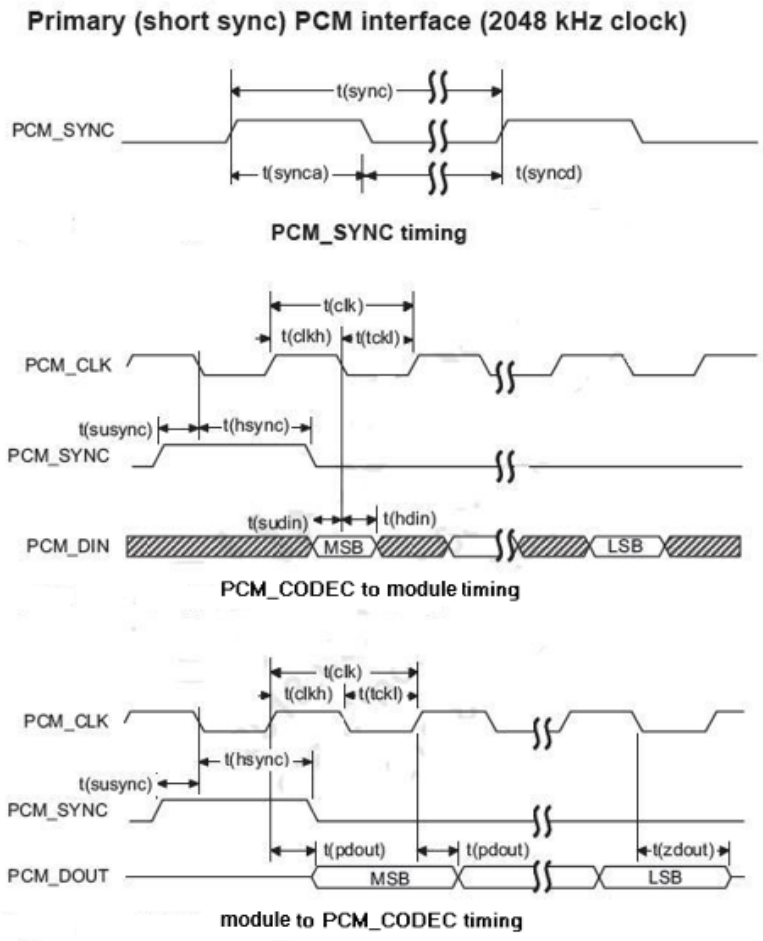
11.1. Digital Audio

LE922A6 can be connected to an external codec through the digital interface.

The product provides one Digital Audio Interface (DVI) on the following Pins:

PAD	Signal	I/O	Function	Type	COMMENT
D11	DVI_WA0	O	Digital Audio Interface (WA0)	B-PD 1.8V	PCM_SYNC
C8	DVI_RX	I	Digital Audio Interface (RX)	B-PD 1.8V	PCM_DIN
D9	DVI_TX	O	Digital Audio Interface (TX)	B-PD 1.8V	PCM_DOUT
C10	DVI_CLK	O	Digital Audio Interface (CLK)	B-PD 1.8V	PCM_CLK

LE922A6 DVI supports PCM master 2048 KHz short frame



PCM_CODEC timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(sync)	PCM_SYNC cycle time		–	125	–	µs
t(synca)	PCM_SYNC asserted time		–	488	–	ns
t(syncd)	PCM_SYNC de-asserted time		–	124.5	–	µs
t(clk)	PCM_CLK cycle time		–	488	–	ns
t(clkh)	PCM_CLK high time		–	244	–	ns
t(clkl)	PCM_CLK low time		–	244	–	ns
t(sync_offset)	PCM_SYNC offset time to PCM_CLK falling		–	122	–	ns
t(sudin)	PCM_DIN setup time to PCM_CLK falling		60	–	–	ns
t(hdin)	PCM_DIN hold time after PCM_CLK falling		60	–	–	ns
t(pdout)	Delay from PCM_CLK rising to PCM_DOUT valid		–	–	60	ns
t(zdout)	Delay from PCM_CLK falling to PCM_DOUT HIGH-Z		–	–	60	ns

12. General Purpose I/O

The general-purpose I/O pads can be configured to act in three different ways:

- input
- output
- alternate function (internally controlled)

Input pads can only be read and report the digital value (high or low) present on the pad at the read time; output pads can only be written or queried and set the value of the pad output; an alternate function pad is internally controlled by the LE922A6 firmware and acts depending on the function implemented.

The following GPIOs are available on the LE922A6.

PAD	Signal	I/O	Function	Type	Drive Strength
F9	GPIO_01	I/O	Configurable GPIO	CMOS 1.8V	2 mA
E10	GPIO_02	I/O	Configurable GPIO	CMOS 1.8V	2 mA
F11	GPIO_03	I/O	Configurable GPIO	CMOS 1.8V	2 mA
E12	GPIO_04	I/O	Configurable GPIO	CMOS 1.8V	2 mA
F13	GPIO_05	I/O	Configurable GPIO	CMOS 1.8V	2 mA
E14	GPIO_06	I/O	Configurable GPIO	CMOS 1.8V	2 mA
R18	GPIO_07	I/O	Configurable GPIO	CMOS 1.8V	2 mA
S19	GPIO_08	I/O	Configurable GPIO	CMOS 1.8V	2 mA
U19	GPIO_09	I/O	Configurable GPIO	CMOS 1.8V	2 mA
W19	GPIO_10	I/O	Configurable GPIO	CMOS 1.8V	2 mA

NOTE:

In order to avoid a back-powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the module when it is powered OFF or during an ON/OFF transition.

NOTE:

LE922A6 GPIO can also be used as alternate I2C function.
Refer to I2C section

12.1. Logic Level Specifications

Where not specifically stated, all the interface circuits work at 1.8V CMOS logic levels.

The following table shows the logic level specifications used in the LE922A6 interface circuits:

For 1,8V signals:

Absolute Maximum Ratings -Not Functional

Parameter	LE922A6	
	Min	Max
Input level on any digital pin when on	-0.3V	+2.3V
Input voltage on analog pins when on	-0.3V	+2.3V

Operating Range - Interface levels (1.8V CMOS)

Level	LE922A6	
	Min	Max
Input high level	1.26V	2.1V
Input low level	-0.3V	0.36V
Output high level	1.44V	1.8V
Output low level	0V	0.4V

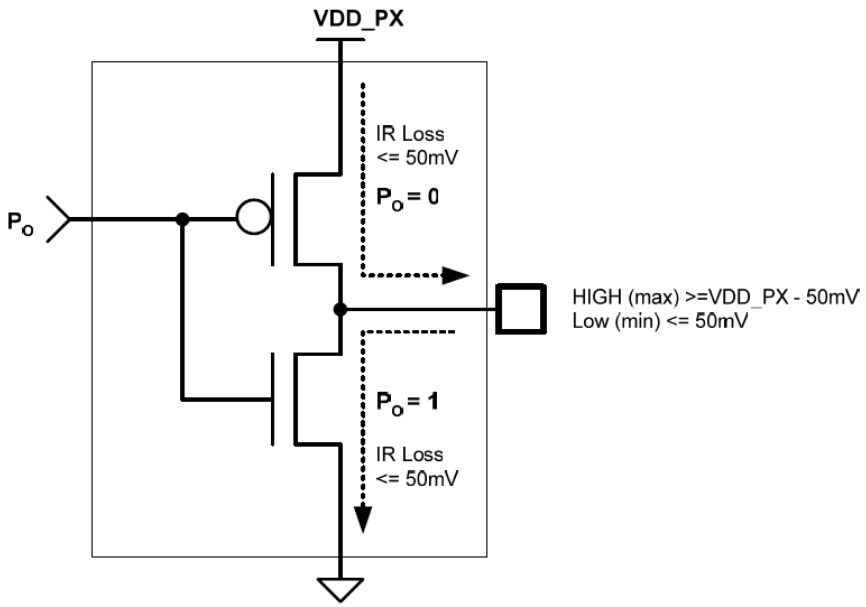
12.2. Using a GPIO Pad as Input

The GPIO pads, when used as inputs, can be connected to a digital output of another device and report its status, provided this device has interface levels compatible with the 1.8V CMOS levels of the GPIO.

If the digital output of the device is connected with the GPIO input, the pad has interface levels different from the 1.8V CMOS. It can be buffered with an open collector transistor with a 47KΩ pull-up resistor to 1.8V.

12.3. Using a GPIO Pad as Output

The GPIO pads, when used as outputs, can drive 1.8V CMOS digital devices or compatible hardware. When set as outputs, the pads have a push-pull output and therefore the pull-up resistor may be omitted.



output PAD equivalent circuit

12.4. Using the Temperature Monitor Function

12.4.1. Short Description

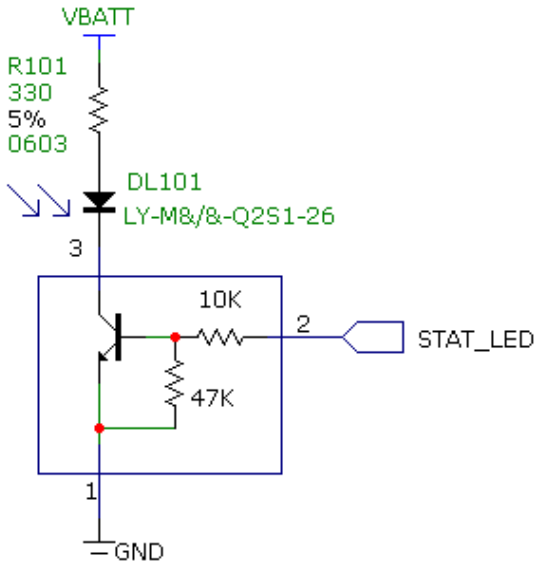
The Temperature Monitor is a function of the module that monitor its internal temperature and if properly set (see the #TEMPMON command on AT Interface guide) it raises to High Logic level a GPIO when the maximum temperature is reached.

12.5. Indication of Network Service Availability

The STAT_LED pin status shows information on the network service availability and call status. In the LE922A6 modules, the STAT_LED usually needs an external transistor to drive an external LED.

The status indicated in the following table is configurable. Refer to AT Commands Reference Guide for the full description of this function

LED Status		Device Status
Permanently off		Device off
Blinking	Period 3s, Ton 1s	Registered with full service
	Period depends on network condition	Registered with power saving
Permanently on		Not registered



12.6. VAUX Power Output

A regulated power supply output is provided in order to supply small devices from the module. This output is active when the module is ON and goes OFF when the module is shut down. The operating range characteristics of the supply are:

Operating Range – VAUX power supply

	Min	Typical	Max
Output voltage	1.75V	1.80V	1.85V
Output current			100mA
Output bypass capacitor (Inside the module)			1µF

13. DAC and ADC section

13.1. DAC Converter

13.1.1. Description

The LE922A6 module provides a Digital to Analog Converter. The signal (named DAC_OUT) is available on pad E14 of the LE922A6 module.

The on board DAC is in the range from 0 to 1023.

However, an external low-pass filter is necessary.

	Min	Max	Units
Voltage range (filtered)	0	1.8	Volt
Range	0	1023	Steps

The precision is 1023 steps, so if we consider that the maximum voltage is 1.8V, the integrated voltage could be calculated with the following formula:

Integrated output voltage = 1.8 * value / 1023

DAC_OUT line must be integrated (for example with a low band pass filter) in order to obtain an analog voltage.

13.1.2. Enabling DAC

An AT command is available to use the DAC function.

The command is:AT#DAC[=<enable>[,<value>]]

<value> - scale factor of the integrated output voltage (0..1023 - 10 bit precision)

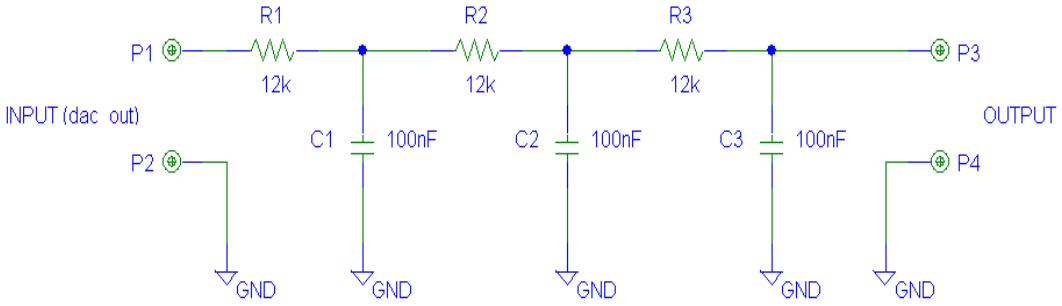
it must be present if <enable>=1

Refer to SW User Guide or AT Commands Reference Guide for the full description of this function.

NOTE:

The DAC frequency is selected internally. D/A converter must not be used during POWERSAVING.

13.1.3. Low Pass Filter Example



13.2. ADC Converter

13.2.1. Description

The on board ADCs are 8-bit converters. They are able to read a voltage level in the range of 0-1.7 volts applied on the ADC pin input and store and convert it into 8 bit word.

	Min	Max	Units
Input Voltage range	0	1.7	Volt
AD conversion	-	8	bits
Resolution	-	< 6.6	mV

The LE922A6 module provides 3 Analog to Digital Converters

13.2.2. Using ADC Converter

An AT command is available to use the ADC function.

The command is AT#ADC? The read value is expressed in mV

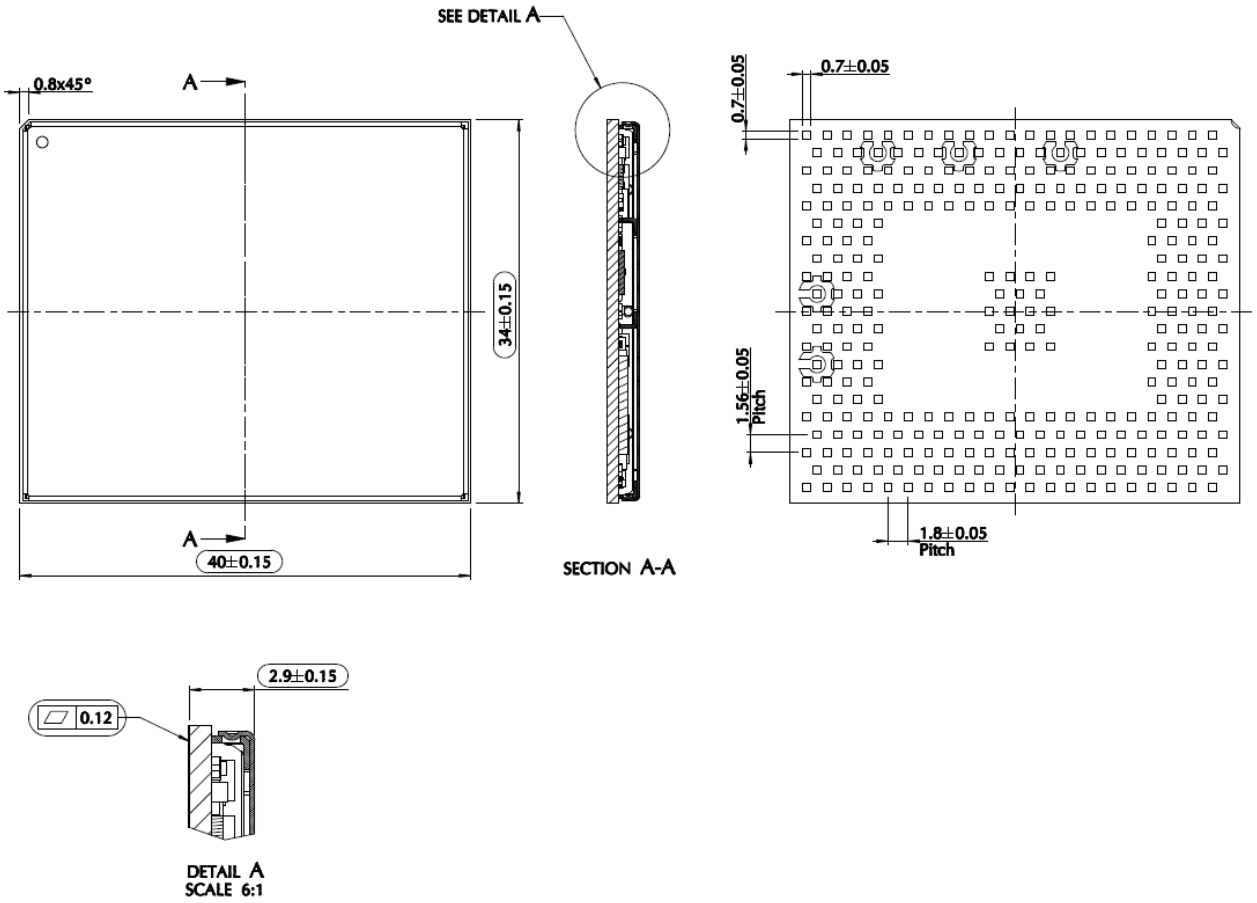
Refer to SW User Guide or AT Commands Reference Guide for the full description of this function.

14. Mounting the module on your board

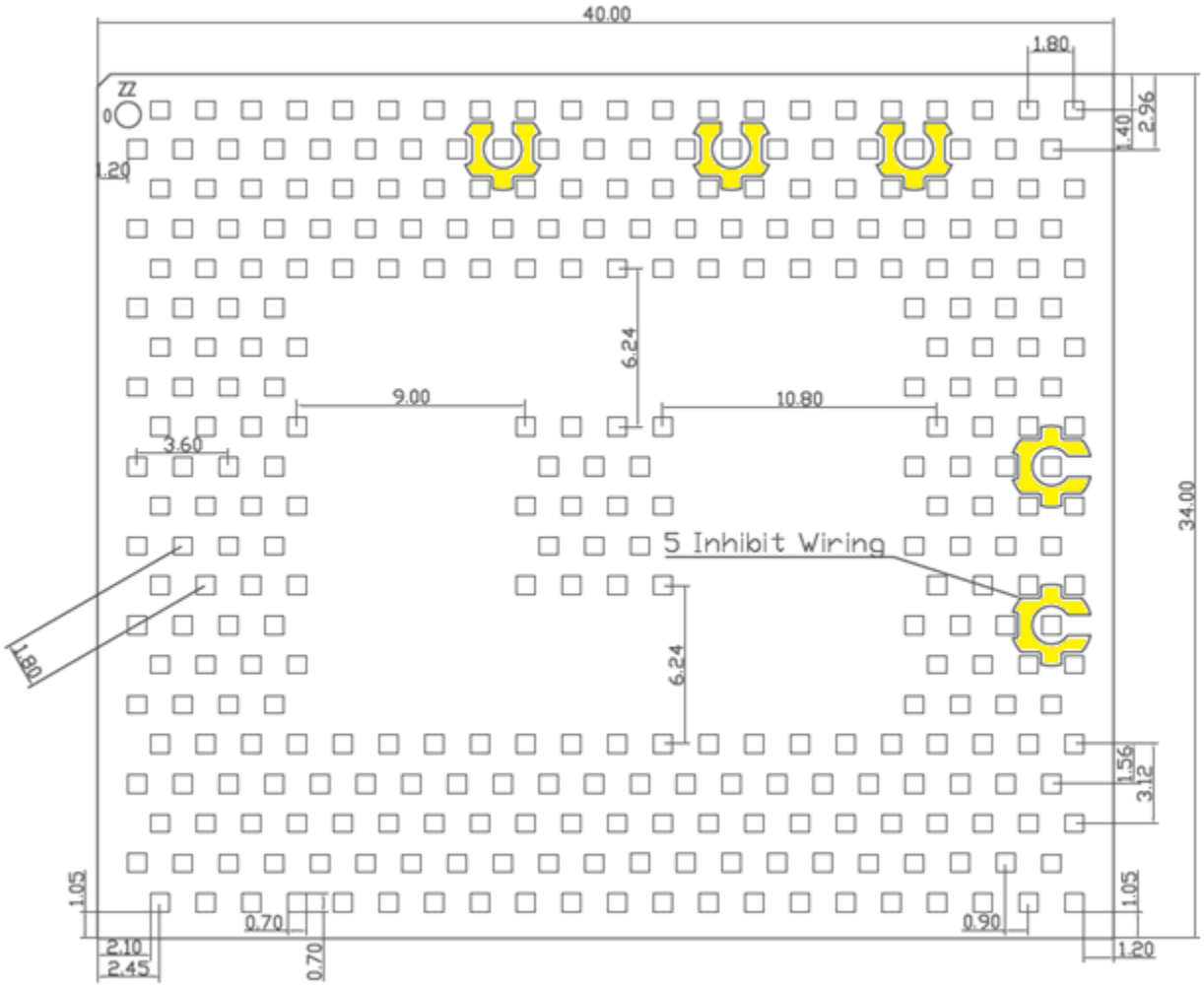
14.1. General

The LE922A6 module is designed to be compliant with a standard Pb free soldering process as defined in JESD22b102d, table 3b. The number of reflows shall not exceed two. This limits Tmax to 245 °C.

14.2. Finishing & Dimensions



14.3. Recommended foot print for the application



LE922A6 316 pads

Top View

In order to easily rework the LE922A6 it is suggested to consider that the application has a 1.5 mm placement inhibit area around the module.

It is also suggested, as a common rule for an SMT component, to avoid having a mechanical part of the application in direct contact with the module.

NOTE:

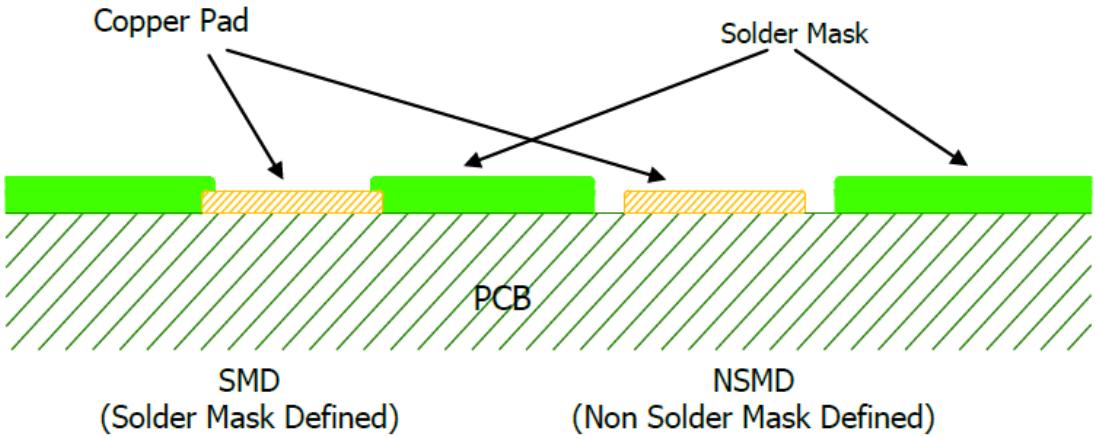
In the customer application, the region under WIRING INHIBIT (see figure above) must be clear from signal or ground paths.

14.4. Stencil

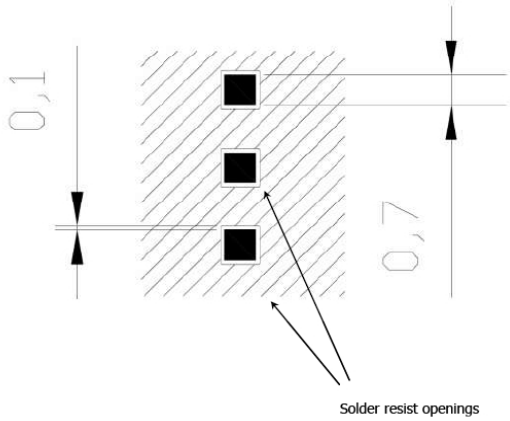
Stencil's apertures layout can be the same as the recommended footprint (1:1). A suggested thickness of stencil foil is greater than 120 µm.

14.5. PCB Pad Design

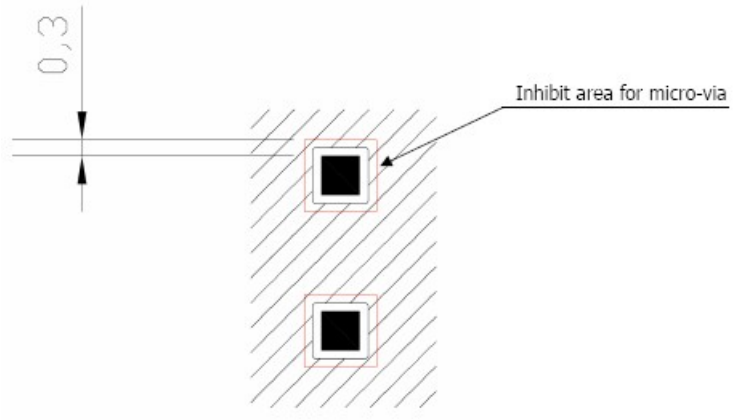
Non solder mask defined (NSMD) type is recommended for the solder pads on the PCB.



14.6. Recommendations for PCB Pad Dimensions (mm)



It is not recommended to place via or micro-via, which are not covered by solder resist in an area of 0,3 mm around the pads unless it carries the same signal of the pad itself (see following figure).



Holes in pad are allowed only for blind holes and not for through holes.

Recommendations for PCB Pad Surfaces:

Finish	Layer thickness (um)	Properties
Electro-less Ni / Immersion Au	3 –7 / 0.05 – 0.15	good solder ability protection, high shear force values

The PCB must be able to resist the higher temperatures which occur during the lead-free process. This issue should be discussed with the PCB-supplier. Generally, the wettability of tin-lead solder paste on the described surface plating is better compared to lead-free solder paste.

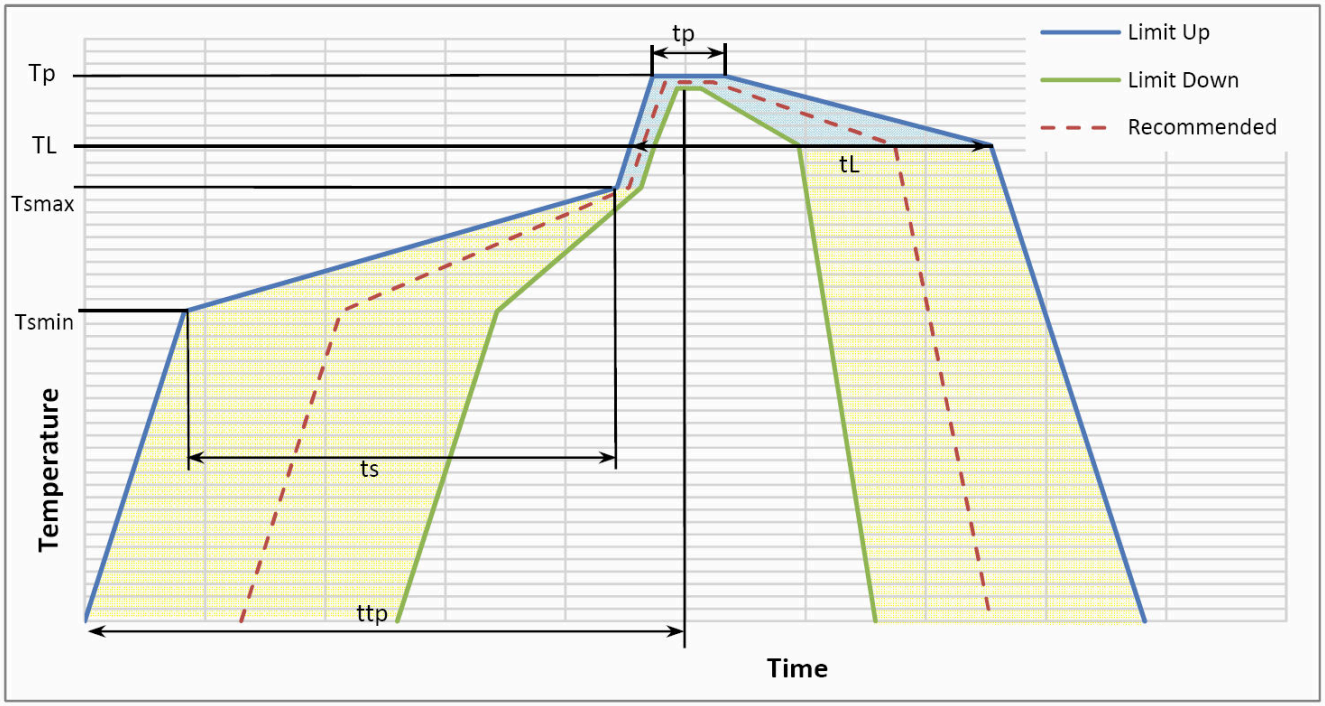
14.7. Solder Paste

Solder Paste	Lead free
	Sn/Ag/Cu

We recommend using only “no clean” solder paste in order to avoid the cleaning of the modules after assembly.

14.7.1. Solder Reflow

Recommended solder reflow profile is shown below:



Profile Feature	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max
Preheat – Temperature Min (Tsmin) – Temperature Max (Tsmax) – Time (min to max) (ts)	 150°C 200°C 60-180 seconds
Tsmax to TL – Ramp-up Rate	 3°C/second max
Time maintained above: – Temperature (TL) – Time (tL)	 217°C 60-150 seconds
Peak Temperature (Tp)	245 +0/-5°C
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds
Ramp-down Rate	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

NOTE:

All temperatures refer to topside of the package, measured on the package body surface.

WARNING:

The LE922A6 module withstands one reflow process only.

15. Application guide

15.1. Debug of the LE922A6 in production

To test and debug the mounting of LE922A6 we strongly recommend foreseeing test pads on the host PCB, in order to check the connection between the LE922A6 itself and the application and to test the performance of the module by connecting it with an external computer. Depending on the customer application, these pads include, but are not limited to the following signals:

- TXD, RXD
- ON_OFF_N
- SHUTDOWN_N
- RESET_N
- GND
- VBATT
- TXD_AUX, RXD_AUX
- VAUX/PWRMON
- USB_VBUS, USB_D+, USB_D-
- USB_SS_RX_P, USB_SS_RX_M, USB_SS_TX_P, USB_SS_TX_M
- Signals for Analysis

15.2. Bypass capacitor on Power supplies

When a sudden voltage is asserted to or cut from the power supplies, the steep transition makes some reactions such as overshoot and undershoot.

This abrupt voltage transition can affect the device causing it to not work or make it malfunction.

Bypass capacitors are needed to alleviate this behavior. The behavior can be affected differently according to the various applications. Customers must pay special attention to this when they design their application board.

The length and width of the power lines need to be considered carefully and the capacitance of the capacitors need to be selected accordingly.

The capacitor will also prevent ripple of the power supplies and the switching noise caused in TDMA systems like GSM.

Especially, a suitable bypass capacitor must be mounted on the Vbatt & Vbatt_PA (Pads AP17,AP19,AR18,AR20,AS17,AS19,AT18,AU17,AU19,AT20) and USB_VBUS (Pad A18) lines in the application board.

The recommended values can be presented as:

- 100uF for Vbatt
- 10uF for USB_VBUS

Customers must still consider that the capacitance mainly depends on the conditions of their application board.

Generally more capacitance is required when the power line is longer.

15.3. SIM interface

This section deals with the recommended schematics for the design of SIM interfaces on the application boards.

15.3.1. SIM schematic example

Figure 1 illustrates in particular how the application side should be designed, and what values the components should have.

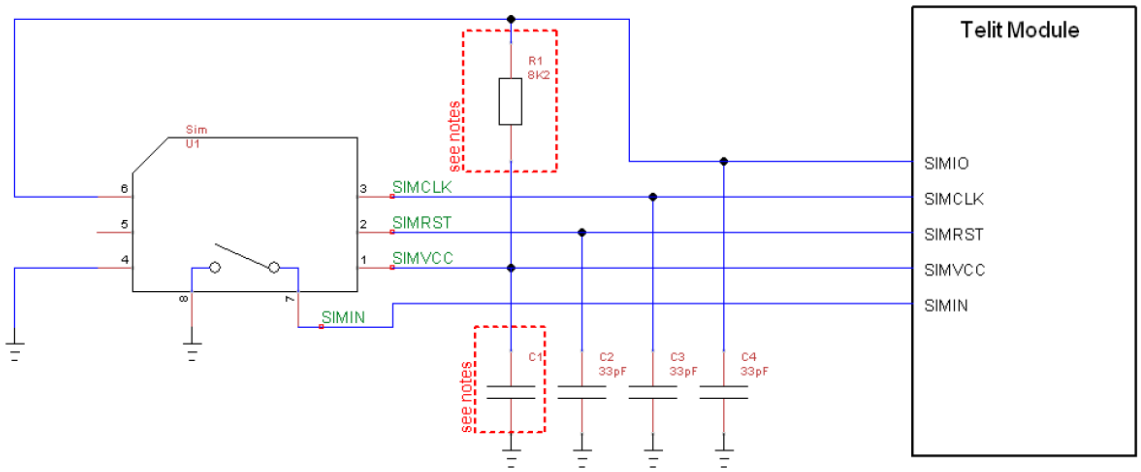


Figure 1

NOTE FOR R1:

The resistor value on SIMIO pulled up to SIMVCC should be defined accordingly in order to be compliant with 3GPP specification.

LE922A6 contains an internal pull-up resistor on SIMIO.

However, the un-mounted option in the application design can be recommended in order to tune R1 if necessary.

The following Table lists the values of C1 to be adopted with the LE922A6 product:

Product P/N	C1 range (nF)
LE922A6	100 nF

Refer to the following document for the detail:

- Telit_SIM integration design guide_Application_note_r10

15.4. ESD Protection

ESD protection on the pins in the table below should be designed by application side according to the customer's requirement.

Pad	Signal	I/O	Function
SIM Card Interface			
A8	SIMVCC	-	External SIM signal – Power supply for the SIM
B11	SIMRST	O	External SIM signal – Reset
B9	SIMIO	I/O	External SIM signal - Data I/O
A10	SIMCLK	O	External SIM signal – Clock
USB HS 2.0 Communication Port			
D19	USB_D+	I/O	USB differential Data(+)
F19	USB_D-	I/O	USB differential Data(-)
A18	USB_VBUS	AI	Power sense for the internal USB transceiver
USB SS 3.0 Communication Port			
C20	USB_SS_RX_P	I	USB super-speed receive (+)
E20	USB_SS_RX_M	I	USB super-speed receive (-)
G20	USB_SS_TX_P	O	USB super-speed transmit (+)
J20	USB_SS_TX_M	O	USB super-speed transmit (-)
Miscellaneous Functions			
P17	VAUX/PWRMON	-	Power output for external accessories
AS1	ON_OFF_N	I	Input command for switching power ON or OFF
AN8	RESET_N	I	Reset input
AN12	SHDN_N	I	Unconditional Shut down Input

All other pins have the following characteristics:
Human Body Model (HBM): ± 1000
Charged Device Model (CDM) JESD22-C101-C: ± 250 V

All Antenna pins up to ± 4kV

WARNING:

Do not touch without proper electrostatic protective equipment. The product must be handled with care, avoiding any contact with the pins because electrostatic discharge may damage the product itself.

15.5. Download and Debug Port

One of the following options should be chosen in the design of host system in order to download or upgrade the Telit software and debug LE922A6 when LE922A6 is already mounted on a host system.

Users who use both UART and USB interfaces to communicate with LE922A6

- Must implement a USB download method in a host system for upgrading LE922A6 when it is mounted.

Users who use USB interface only to communicate with LE922A6

- Must arrange for a UART port in a host system for debugging or upgrading LE922A6 when it is mounted.

Users who use UART interface only to communicate with LE922A6

- Must arrange for a USB port in a host system for debugging or upgrading LE922A6 when it is mounted.

For debugging

- It would be good for debugging if you designed module's UART2 RX/TX pins are exposed to outside.

16. Packing system

The Telit LE922A6 is packaged on trays. The tray is JEDEC compliant, injection molded antistatic Modified Polyphenylene ether (MPPO). It has good thermal characteristics and can withstand a the standard baking temperature up to 125°C, thereby avoiding handling the modules if baking is required. The trays are rigid, thus providing more mechanical protection against transport stress. Additionally they are re-usable and so environmentally sustainable.

There are 2 (two) antistatic rubber bands that enclose each envelope.

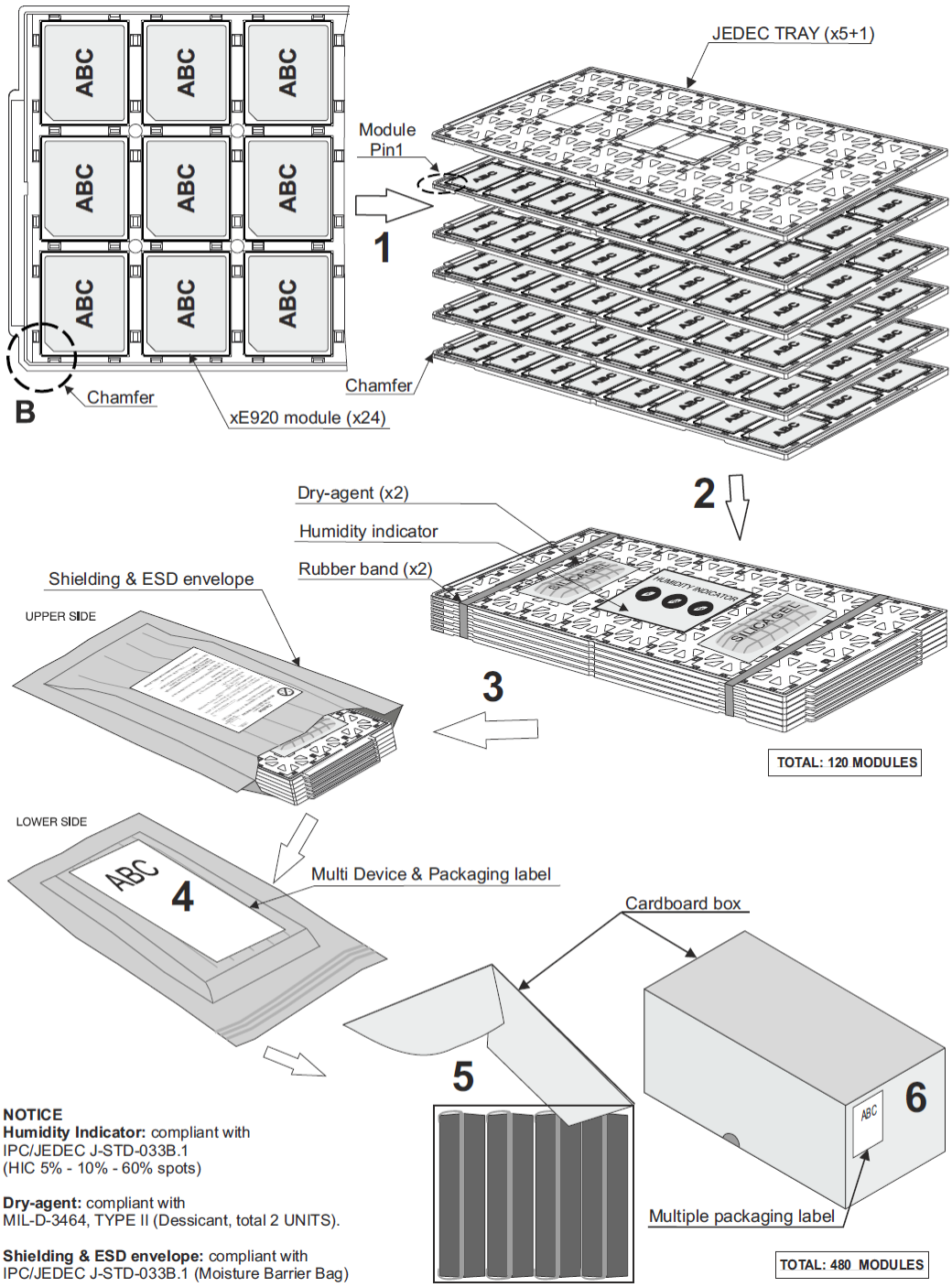
The carton box is rigid, thus offering mechanical protection. The carton box has one flap across the whole top surface. It is sealed with tape along the edges of the box.

Below is an example diagram of packing for a module with 920 form factor

Tray		in each tray	inside each envelope		inside each carton box	
Modules/tray	**Description**	**modules/ tray**	**trays/ envelope**	**modules/ envelope**	**envelopes/ carton box**	**modules/ box**
xE920 packaging	JEDEC Tray	24	**5+ 1 empty**	**120**	4	**480**

	Qty
Minimum Order Quantity (MOQ)	**120**
Standard Packing Quantity (SPQ)	**480**

Each tray contains 24 pieces as shown in the following picture:



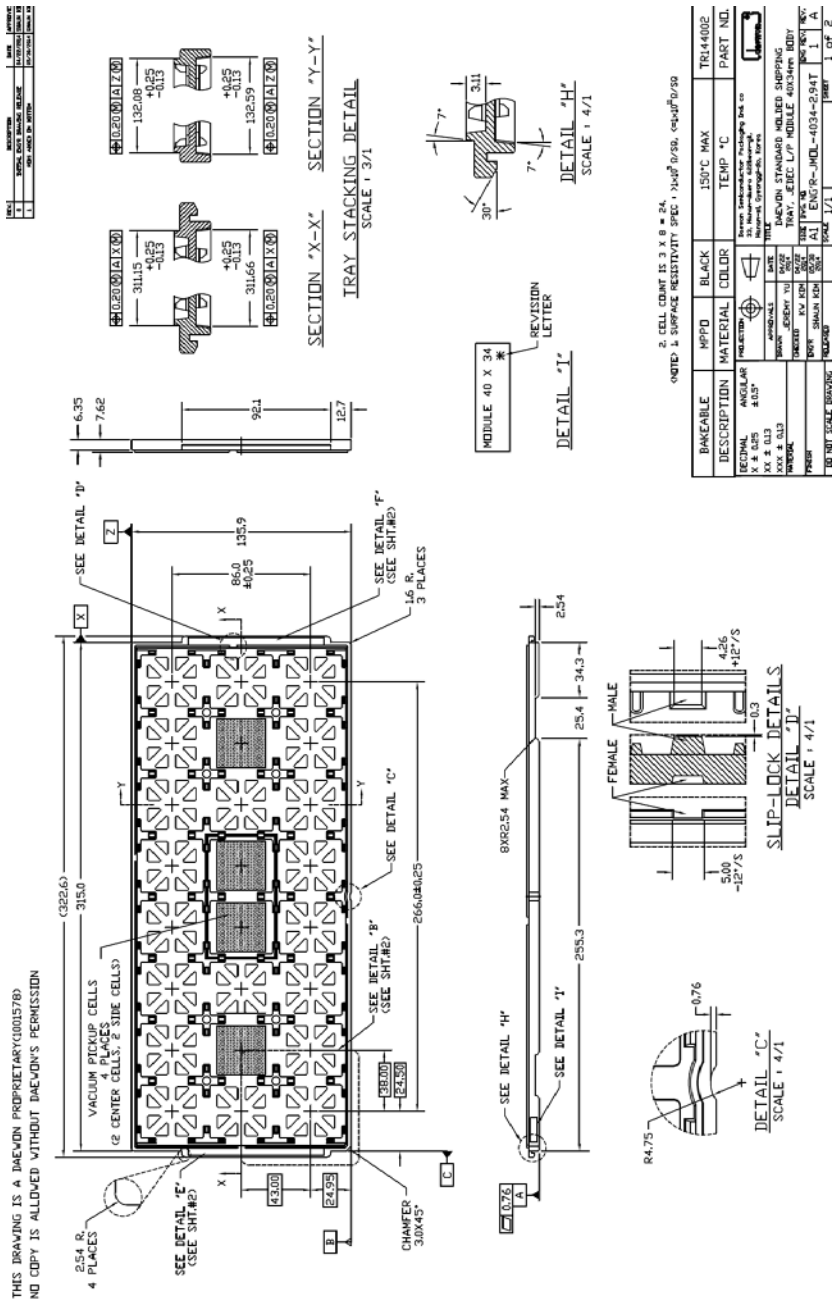
NOTICE
Humidity Indicator: compliant with IPC/JEDEC J-STD-033B.1 (HIC 5% - 10% - 60% spots)

Dry-agent: compliant with MIL-D-3464, TYPE II (Dessicant, total 2 UNITS).

Shielding & ESD envelope: compliant with IPC/JEDEC J-STD-033B.1 (Moisture Barrier Bag)

16.1. Tray Drawing

The Telit LE922A6 is packaged on trays. Each tray contains 24 pieces with the following dimensions:



16.2. Moisture Sensitivity

The LE922A6 is a Moisture Sensitive Device level 3, in accordance with standard IPC/JEDEC J-STD-020. Observe all of the requirements for using this kind of components.

Calculated shelf life in sealed bag: 4 months at <40°C and <90% relative humidity (RH).

17. Safety Recommendations

READ CAREFULLY

Be sure that the use of this product is allowed in your country and in the environment required. The use of this product may be dangerous and must be avoided in the following areas:

- Where it can interfere with other electronic devices in environments such as hospitals, airports, aircrafts, etc.
- Where there is risk of explosion such as gasoline stations, oil refineries, etc.

It is the responsibility of the user to enforce the country regulations and the specific environment regulations.

Do not disassemble the product; any mark of tampering will compromise the warranty validity.

We recommend following the instructions of the hardware user guides for correct wiring of the product. The product must be supplied with a stabilized voltage source and the wiring conform to the security and fire prevention regulations.

The product must be handled with care, avoiding any contact with the pins because electrostatic discharges may damage the product itself. The same caution must be taken for the SIM, checking carefully the instructions for its use. Do not insert or remove the SIM when the product is in power saving mode.

The system integrator is responsible for the functioning of the final product; therefore, care must be taken of the external components of the module, as well as of any project or installation issue, because of the risk of disturbing the GSM network or external devices or having any impact on safety. Should there be any doubt, please refer to the technical documentation and the regulations in force.

Every module must be equipped with a proper antenna with the specified characteristics. The antenna must be installed with care in order to avoid any interference with other electronic devices and must be installed with the guarantee of a minimum 20 cm distance from a human body. In case this requirement cannot be satisfied, the system integrator must assess the final product against the SAR regulation.

The European Community provides some Directives for electronic equipment introduced on the market. All the relevant information is available on the European Community website:

http://europa.eu.int/comm/enterprise/rtte/dir99-5.htm

The text of the Directive 99/05 regarding telecommunication equipment is available, while the applicable Directives (Low Voltage and EMC) are available at:

http://europa.eu.int/comm/enterprise/rtte/dir99-5.htm

18. Conformity assessment issues

18.1. 1999/5/EC Directive

The LE922A6-E1 module has been evaluated against the essential requirements of the 1999/5/EC Directive.

Bulgarian	С настоящето Telit Communications S.p.A. декларира, че 2G/3G module отговаря на съществените изисквания и другите приложими изисквания на Директива 1999/5/EC.
Czech	Telit Communications S.p.A. tímto prohlašuje, že tento 2G/3G module je ve shodě se základními požadavky a dalšími příslušnými ustanoveními směrnice 1999/5/ES.
Danish	Undertegnede Telit Communications S.p.A. erklærer herved, at følgende udstyr 2G/3G module overholder de væsentlige krav og øvrige relevante krav i direktiv 1999/5/EF.
Dutch	Hierbij verklaart Telit Communications S.p.A. dat het toestel 2G/3G module in overeenstemming is met de essentiële eisen en de andere relevante bepalingen van richtlijn 1999/5/EG.
English	Hereby, Telit Communications S.p.A., declares that this 2G/3G module is in compliance with the essential requirements and other relevant provisions of Directive 1999/5/EC.
Estonian	Käesolevaga kinnitab Telit Communications S.p.A. seadme 2G/3G module vastavust direktiivi 1999/5/EÜ põhinõuetele ja nimetatud direktiivist tulenevatele teistele asjakohastele sätetele.
German	Hiermit erklärt Telit Communications S.p.A., dass sich das Gerät 2G/3G module in Übereinstimmung mit den grundlegenden Anforderungen und den übrigen einschlägigen Bestimmungen der Richtlinie 1999/5/EG befindet.
Greek	ΜΕ ΤΗΝ ΠΑΡΟΥΣΑ Telit Communications S.p.A. ΔΗΛΩΝΕΙ ΟΤΙ 2G/3G module ΣΥΜΜΟΡΦΩΝΕΤΑΙ ΠΡΟΣ ΤΙΣ ΟΥΣΙΩΔΕΙΣ ΑΠΑΙΤΗΣΕΙΣ ΚΑΙ ΤΙΣ ΛΟΙΠΕΣ ΣΧΕΤΙΚΕΣ ΔΙΑΤΑΞΕΙΣ ΤΗΣ ΟΔΗΓΙΑΣ 1999/5/ΕΚ.
Hungarian	Alulírott, Telit Communications S.p.A. nyilatkozom, hogy a 2G/3G module megfelel a vonatkozó alapvetõ követelményeknek és az 1999/5/EC irányelv egyéb elõírásainak.
Finnish	Telit Communications S.p.A. vakuuttaa täten että 2G/3G module tyyppinen laite on direktiivin 1999/5/EY oleellisten vaatimusten ja sitä koskevien direktiivin muiden ehtojen mukainen.
French	Par la présente Telit Communications S.p.A. déclare que l'appareil 2G/3G module est conforme aux exigences essentielles et aux autres dispositions pertinentes de la directive 1999/5/CE.
Icelandic	Hér með lýsir Telit Communications S.p.A. yfir því að 2G/3G module er í samræmi við grunnkröfur og aðrar kröfur, sem gerðar eru í tilskipun 1999/5/EC
Italian	Con la presente Telit Communications S.p.A. dichiara che questo 2G/3G module è conforme ai requisiti essenziali ed alle altre disposizioni pertinenti stabilite dalla direttiva 1999/5/CE.
Latvian	Ar šo Telit Communications S.p.A. deklarē, ka 2G/3G module atbilst Direktīvas 1999/5/EK būtiskajām prasībām un citiem ar to saistītajiem noteikumiem.
Lithuanian	Šiuo Telit Communications S.p.A. deklaruoja, kad šis 2G/3G module atitinka esminius reikalavimus ir kitas 1999/5/EB Direktyvos nuostatas.
Maltese	Hawnhekk, Telit Communications S.p.A., jiddikjara li dan 2G/3G module jikkonforma mal-ħtiġijiet essenzjali u ma provvedimenti oħrajn relevanti li hemm fid-Dirrettiva 1999/5/EC.
Norwegian	Telit Communications S.p.A. erklærer herved at utstyret 2G/3G module er i samsvar med de grunnleggende krav og øvrige relevante krav i direktiv 1999/5/EF.
Polish	Niniejszym Telit Communications S.p.A. oświadcza, że 2G/3G module jest zgodny z zasadniczymi wymogami oraz pozostałymi stosownymi postanowieniami Dyrektywy 1999/5/EC
Portuguese	Telit Communications S.p.A. declara que este 2G/3G module está conforme com os requisitos essenciais e outras disposições da Directiva 1999/5/CE.
Slovak	Telit Communications S.p.A. týmto vyhlasuje, že 2G/3G module spĺňa základné požiadavky a všetky príslušné ustanovenia Smernice 1999/5/ES.
Slovenian	Telit Communications S.p.A. izjavlja, da je ta 2G/3G module v skladu z bistvenimi zahtevami in ostalimi relevantnimi določili direktive 1999/5/ES.
Spanish	Por medio de la presente Telit Communications S.p.A. declara que el 2G/3G module cumple con los requisitos esenciales y cualesquiera otras disposiciones aplicables o exigibles de la Directiva 1999/5/CE.
Swedish	Härmed intygar Telit Communications S.p.A. att denna 2G/3G module står I överensstämmelse med de väsentliga egenskapskrav och övriga relevanta bestämmelser som framgår av direktiv 1999/5/EG.

In order to satisfy the essential requirements of 1999/5/EC Directive, the LE922A6-E1 module is compliant with the following standard:

Essential requirements	Specifications / Standards
Article 3.1(a): Electrical safety	EN 60950-1:2006 + A11:2009 + A1:2010 + A12:2011 + AC:2011 + A2:2013
Article 3.1(a): Exposure to electromagnetic fields	EN 62311:2008
Article 3.1(b): EMC	EN 301 489-1 V1.9.2 EN 301 489-24 V1.5.1
Article 3.2: Radio spectrum use	EN 301 908-1 V7.1.1 EN 301 908-13 V6.2.1

The conformity assessment procedure referred to in Article 10 and detailed in Annex IV of Directive 1999/5/EC has been followed with the involvement of the following Notified Body:

AT4 wireless S.A.
Parque Technologico de Andalucia
C/ Severo Ochoa 2
29590 Campanillas – Malaga
SPAIN
Notified Body No: 1909

Thus the following marking is included in the product:

CE 1909

There is no restriction for the commercialization of the LE922A6-E1 module in all The countries of the European Union.

Final product integrating this module must be assessed against essential requirements of the 1999/5/EC(R&TTE) Directive. It should be noticed that assessment does not necessarily lead to testing. Telit Communications S.p.A recommends carrying out the following assessments:

RF spectrum use (R&TTE art. 3.2)	It will depend on the antenna used on the final product.
EMC (R&TTE art. 3.1b)	Testing
Health & Safety (R&TTE art. 3.1a)	Testing

Alternately, assessment of the final product against EMC (Art. 3.1b) and Electrical safety (Art. 3.1a)
Essential requirements can be done against the essential requirements of the EMC and the LVD Directives:

- Low Voltage Directive 2006/95/EC and product safety
- Directive EMC 2004/108/EC for conformity for EMC

18.2. RCM

The LE922A6-A1 module has been evaluated against the essential requirements of the RCM. The LE922A6-A1 module is compliant with all applicable requirements of the standards and regulations listed below:

Test specification:	Telecommunications (Labelling Notice for Customer Equipment and Customer Cabling) Instrument 2015, (Schedule 1, item 3) AS/NZS 60950.1:2011, AS/CA S042.1:2015; AS/CA S042.4:2015
Compliance Marking:	RCM
Certificate No.:	CBA160750.01

19. Document History

Revision	Date	Changes
Preliminary	2015-12-14	First issue
Preliminary - 1	2016-01-27	Section 5.1, update Current consumption Section 14.3, correct type error
Preliminary - 2	2016-03-22	Section 2.2, update Operating Frequency Section 2.5, update Temperature range Section 3.1, update Pin-out Section 3.1.1, update LE922A6 LGA Pads Layout Section 5.2.2, update Thermal Design Guidelines Section 4, update Hardware Commands Section 6, update Antenna Section 8, update USB Port Section 13, update DAC and ADC section Section 14.3, update Recommended foot print for the application Section 15.1, update Debug of the LE922A6 in production Section 15.3, update SIM interface Section 15.4, ESD Protection
0	2016-04-05	Section 2.2, update Operating Frequency Section 2.5, update Rx sensitivity and Maximum Tx Power Section 3.1, update Pin-out Section 3.1.1, update LE922A6 LGA Pads Layout Section 4.2, update Initialization and Activation state Section 4.3, change section title 'RESET and Shutdown the LE922A6' Section 6.4, update Secondary Antenna Requirements Section 16.1, update Tray Drawing
1	2016-05-12	Section 2.2, correct error Operating Frequency Section 2.5, change TX power and RX sensitivity tolerance Section 3.1, add comments Section 4.2, update paragraph Section 4.4, update paragraph Section 4.5.1 update paragraph Section 5.1, correct error of current consumption and Tip Section 7,9,12.1, correct logic level Section 8 add comments for USB3.0 Section 12.5 update comments Section 14.2, add Finishing & Dimensions Section 15.4 add Warning for ESD
2	2016-08-03	Section 2.5, change TX maximum power and RX sensitivity tolerance Section 3.1, update Note Section 4.2 change delay time in the flow chart

		Section 4.3.2 update paragraph Section 4.4, update paragraph Section 4.5.1, update Ctank value Section 16.5, update download and debug port Section 18, add conformity assessment issues; 1999/5/EC Directive, RCM
3	2016-08-16	Section 3.1, update ON_OFF_N pin description Section 4.2, update comments, paragraph and flow chart Section 4.3.1, update paragraph Section 4.3.2, update paragraph Section 4.3.4, remove paragraph and update comments Section 4.4, update paragraph Section 4.5.1, update Ctank value Section 8, update Note Section 10, update comments Section 12.4.1, update comments Section 12.5, update comments
4	2016-08-22	Section 4.2, update paragraph and flow chart Section 4.3.3, update paragraph Section 4.3.4, update paragraph Section 4.4, update paragraph Section 5.1, update comments Section 5.2, update comments Section 6.4, update comments Section 14.3, update foot print
5	2017-04-12	Section 2.2, add LE922A6-E2 Section 2.5, add LE922A6-E2 Section 3.1.1, update paragraph Section 6.1, add LE922A6-E2 Section 6.4, add LE922A6-E2 Section 6.4, add LE922A6-E2 Section 18.1, correct error typo