ML865C1
HW User Guide

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TELIT
TECHNICAL
DOCUMENTATION

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APPLICABILITY TABLE

PRODUCTS

- ML865C1-NA
- ML865C1-EA

Contents

1. INTRODUCTION

1.1. Scope

Scope of this document is is the description of some hardware solutions useful for developing a product with the Telit ML865C1 module.

1.2. Audience

This document is intended for Telit customers, who are integrators, about to implement their application using our ML865C1 module.

1.3. Contact Information, Support

For general contact, technical support services, technical questions and report documentation errors contact Telit Technical Support at:

- TS-EMEA@telit.com
- TS-AMERICAS@telit.com
- TS-APAC@telit.com
- TS-SRD@telit.com

Alternatively, use:

http://www.telit.com/support

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

http://www.telit.com

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

1.4. Text Conventions

Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

1.5. Related Documents

80000NT10001A - SIM INTEGRATION DESIGN GUIDES Application Note

2. OVERVIEW

The aim of this document is the description of some hardware solutions useful for developing a product with the Telit ML865C1 module. In this document all the basic functions of a mobile phone will be taken into account; for each one of them a proper hardware solution will be suggested and eventually the wrong solutions and common errors to be avoided will be evidenced. Obviously this document cannot embrace the whole hardware solutions and products that may be designed. The wrong solutions to be avoided shall be considered as mandatory, while the suggested hardware configurations shall not be considered mandatory, instead the information given shall be used as a guide and a starting point for properly developing your product with the Telit ML865C1 module. For further hardware details that may not be explained in this document refer to the Telit ML865C1 Product Description document where all the hardware information is reported.

NOTE:

(EN) The integration of the ML865C1 cellular module within user application shall be done according to the design rules described in this manual.

(IT) L'integrazione del modulo cellulare ML865C1 all'interno dell'applicazione dell'utente dovrà rispettare le indicazioni progettuali descritte in questo manuale.

(DE) Die Integration des ML865C1 Mobilfunk-Moduls in ein Gerät muß gemäß der in diesem Dokument beschriebenen Kunstruktionsregeln erfolgen.

(SL) Integracija ML865C1 modula v uporabniški aplikaciji bo morala upoštevati projektna navodila, opisana v tem priročniku.

(SP) La utilización del modulo ML865C1 debe ser conforme a los usos para los cuales ha sido deseñado descritos en este manual del usuario.

(FR) L'intégration du module cellulaire ML865C1 dans l'application de l'utilisateur sera faite selon les règles de conception décrites dans ce manuel.

(HE) האינטגרטור מתבקש ליישם את ההנחיות המפורטות במסמך זה בתהליך האינטגרציה של המודם הסלולרי LE910 V2 עם המוצר.

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3. PINS ALLOCATION

Warning: ML865C1 is adopting a modified 56-pin xL865 Form Factor, pin to pin compatible with the previous 48-pin xL865 FF and with 8 additional pads.

The numbering of the pins has been changed accordingly and attention has to be paid when comparing with previous 48-pin xL865 FF design.

3.1. Pin-out

Pin	Signal	I/O	Function	Type	Comment
USB HS 2.0 COMMUNICATION PORT					
20	USB_D+	I/O	USB differential Data (+)	3V	
19	USB_D-	I/O	USB differential Data (-)	3V	
18	VUSB	I	Power sense for the internal USB transceiver.	3-5V	Internal PD (100K)
Asynchronous Serial Port (USIF0) - Prog. / Data + HW Flow Control					
1	C109/DCD/GPO	O	Output for Data carrier detect signal (DCD) to DTE / GP output	CMOS 1.8V	
2	C125/RING/GPO	O	Output for Ring indicator signal (RI) to DTE / GP output	CMOS 1.8V	

3	C107/DSR/GPO	O	Output for Data set ready signal (DSR) to DTE / GP output	CMOS 1.8V	
4	C108/DTR/GPI	I	Input for Data terminal ready signal (DTR) from DTE / GP input	CMOS 1.8V	
5	C105/RTS/GPI	I	Input for Request to send signal (RTS) from DTE / GP input	CMOS 1.8V	
6	C106/CTS/GPO	O	Output for Clear to send signal (CTS) to DTE / GP output	CMOS 1.8V	
9	C103/TXD	I	Serial data input (TXD) from DTE	CMOS 1.8V	
10	C104/RXD	O	Serial data output to DTE	CMOS 1.8V	
SIM card interface					
11	SIMVCC	-	External SIM signal – Power supply for the SIM		1,8 / 3V
12	SIMRST	O	External SIM signal – Reset		1,8 / 3V
13	SIMCLK	O	External SIM signal – Clock		1,8 / 3V
14	SIMIO	I/O	External SIM signal – Data I/O	47k Pull up	1,8 / 3V
ADC					

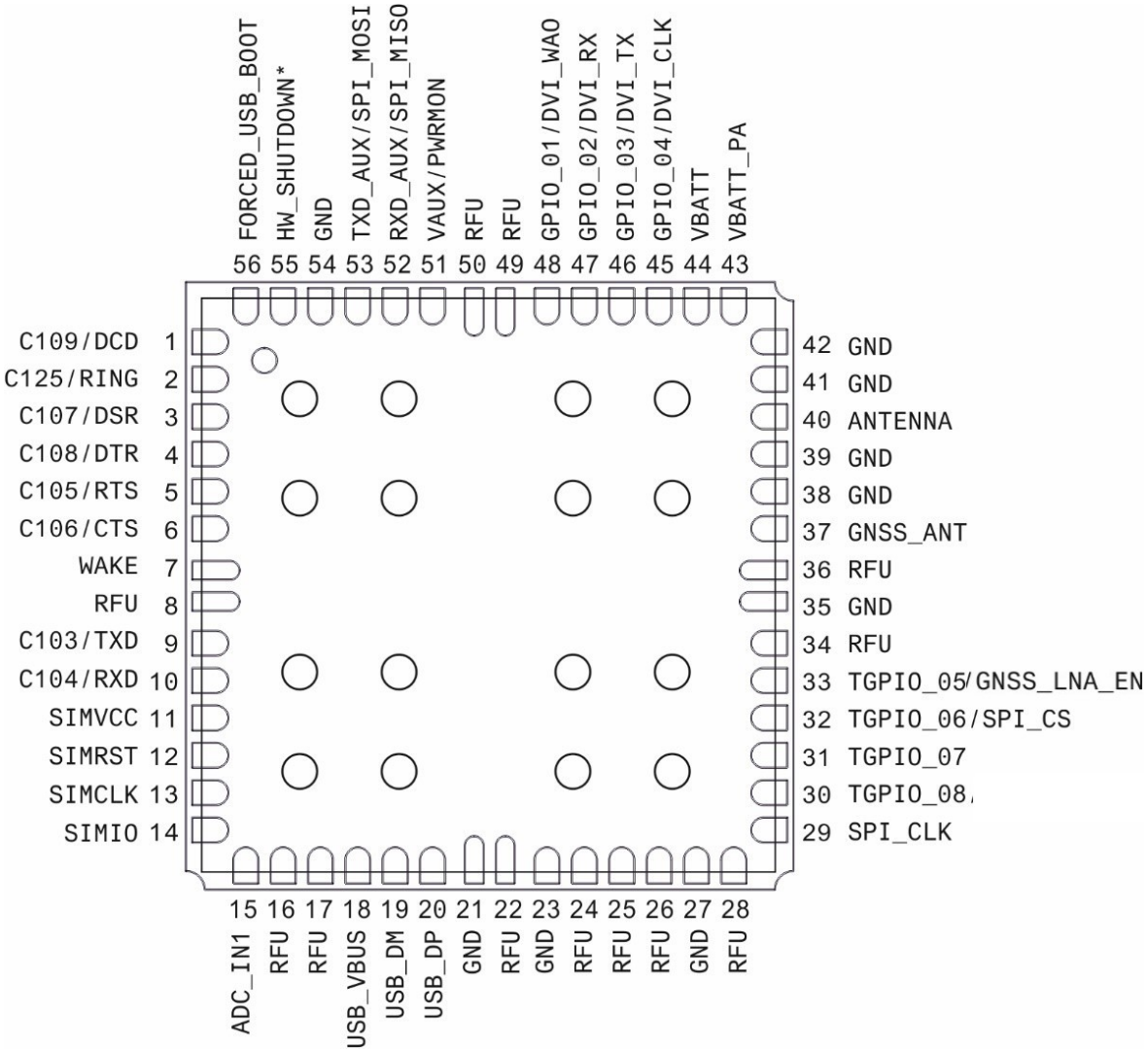
15	ADC_IN1	I	Analog/Digital converter input		
Auxiliary					
52	RXD_AUX /SPI_MISO	I	Auxiliary UART (RX Data)/SPI_MISO		CMOS 1.8V
53	TXD_AUX / SPI_MOSI	O	Auxiliary UART (TX Data)/SPI_MOSI		CMOS 1.8V
Miscellaneous					
7	WAKE	I	ASYNCRONOUS WAKEUP FROM PSM	1.8V	
55	HW_SHUTDOWN*	I	UNCONDITIONAL SHUTDOWN	1.8V	
51	V_AUX/PWRMON	O		1.8V	
56	FORCED_USB_BOOT	I		1.8V	
40	ANTENNA	I/O	Antenna pad – 50 Ω		RF
37	GNSS_ANT	I/O	GNSS receiver input - 50 Ω		RF
GPIO					
48	GPIO_01 / DVI_WA0	I/O	GPIO01 Configurable GPIO / Digital Audio Interface (WA0)		CMOS 1.8V
47	GPIO_02 /DVI_RX	I/O	GPIO02 I/O pin Digital Audio Interface (RX)		CMOS 1.8V
46	GPIO_03 / DVI_TX	I/O	GPIO03 GPIO I/O pin/ Digital Audio Interface (TX)		CMOS 1.8V

45	GPIO_04 / DVI_CLK	I/O	GPIO04 Configurable GPIO/ Digital Audio Interface (CLK)		CMOS 1.8V
33	GPIO_05/ GNSS_LNA_EN	I/O	GPIO05 Configurable GPIO		CMOS 1.8V
32	GPIO_06 / SPI_CS	I/O	GPIO06 Configurable GPIO /SPI_CS		CMOS 1.8V
31	GPIO_07	I/O	GPIO07 Configurable GPIO		CMOS 1.8V
30	GPIO_08	I/O	GPIO08 Configurable GPIO		CMOS 1.8V
29	SPI_CLK	O	SPI_CLK		CMOS 1.8V
X	STAT_LED	O	STAT_LED	CMOS 1.8V	All 8 GPIO pins can be configured
Power Supply					
44	VBATT	-	Main power supply (Baseband)		Power
43	VBATT_PA	-	Main power supply (Radio PA)		Power
42	GND	-	Ground		Power
41	GND	-	Ground		Power
39	GND	-	Ground		Power
38	GND	-	Ground		Power
35	GND	-	Ground		Power
27	GND	-	Ground		Power
23	GND	-	Ground		Power

21	GND	-	Ground	Power
54	GND	-	Ground	Power
Reserved				
8			RFU	
15			RFU	
16			RFU	
17			RFU	
22			RFU	
24			RFU	
25			RFU	
26			RFU	
28			RFU	
34			RFU	
36			RFU	

3.2. Pin Layout

TOP VIEW



NOTE:

The pins defined as NC/RFU shall be considered RESERVED and must not be connected to any pin in the application.

4. POWER SUPPLY

The power supply circuitry and board layout are a very important part in the full product design and they strongly reflect on the product overall performance, hence read the requirements carefully and the guidelines that will follow for a proper design.

4.1. Power Supply Requirements

The external power supply must be connected to VBATT & VBATT_PA signals and must fulfill the following requirements:

Power Supply	Value
Nominal Supply Voltage	3.8V
Operating Voltage Range	3.40 V÷ 4.20 V
Extended Voltange Range	3.20 V÷ 4.50 V

NOTE:
The Operating Voltage Range MUST never be exceeded; care must be taken when designing the application's power supply section to avoid having an excessive voltage drop. If the voltage drop is exceeding the limits it could cause a Power Off of the module.
The Power supply must be higher than 3.20 V to power on the module.

Overshoot voltage (regarding MAX Extended Operating Voltage) and drop in voltage (regarding MIN Extended Operating Voltage) MUST never be exceeded;
The "Extended Operating Voltage Range" can be used only with completely assumption and application of the HW User guide suggestions.

	NOTE: For PTCRB approval on the final products the power supply is required to be within the “Normal Operating Voltage Range”.

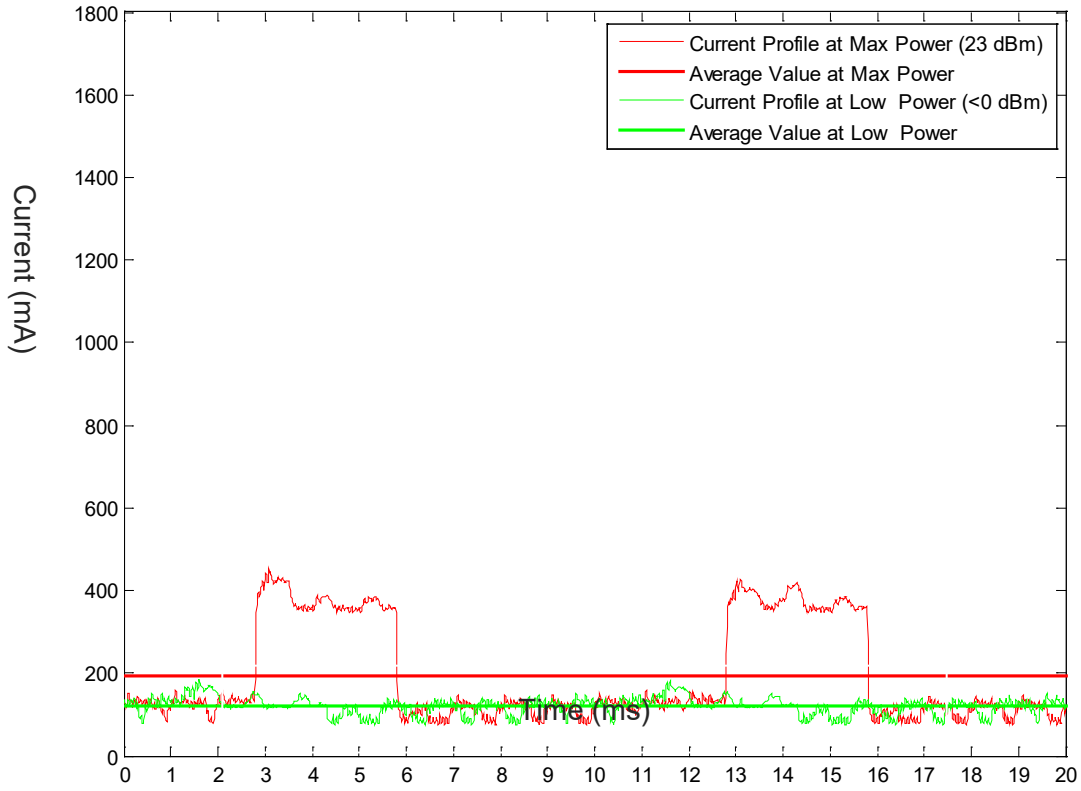
4.2. Power Consumption

*Preliminary data

Mode	Average (mA)	Mode Description
Switched off	0.008mA	Module supplied but switched off
IDLE mode		
AT+CFUN=1	12 mA	Normal mode: full functionality of the module
AT+CFUN=4	11 mA	Disabled TX and RX; module is not registered on the network
AT+CFUN=5	2.3 mA	Paging cycle #64 frames (0.64 sec DRx cycle)
	1.4 mA	Paging cycle #128 frames (1.28 sec DRx cycle)
	1.1 mA	Paging cycle #256 frames (2.56 sec DRx cycle)
Operative Mode		
LTE Data call	190 mA	CAT M1 RB=1, TX=23dBm
	115 mA	CAT M1 Channel BW 10MHz, RB=1, TX=0dBm
GPRS 1TX+1RX **GSM 850/900**	240 mA	GPRS Sending data mode, TX=33dBm

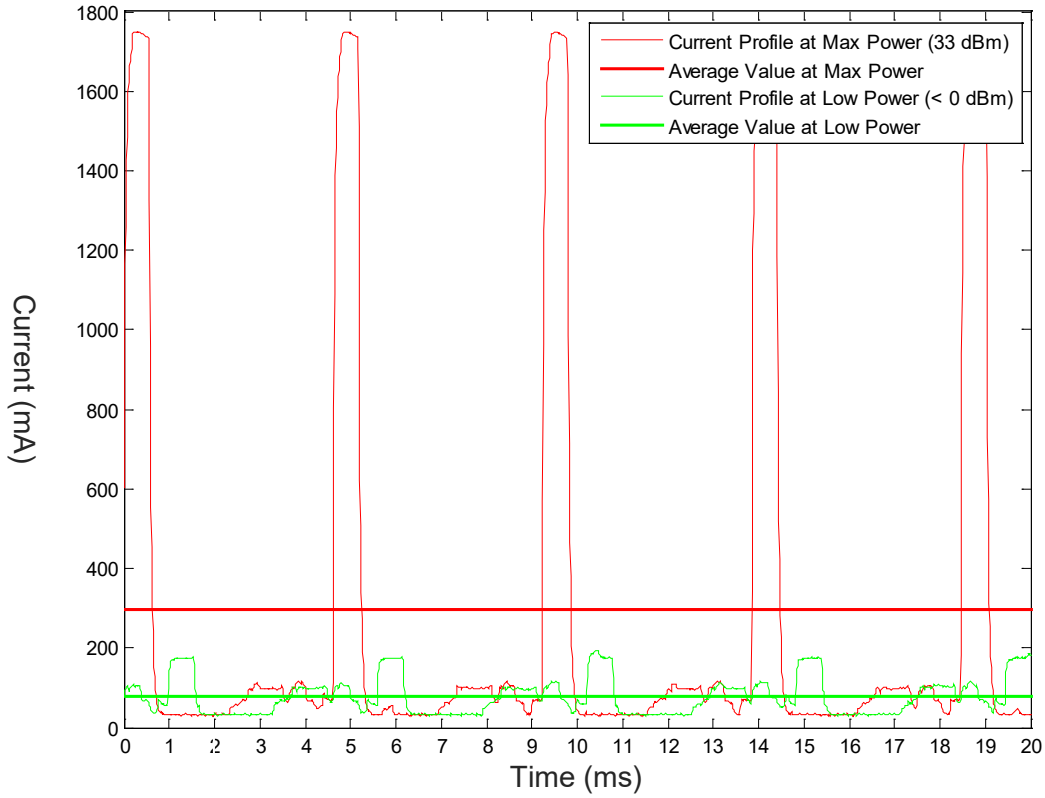
GPRS 1TX+1RX GSM 1800/1900	170 mA	GPRS Sending data mode, TX=30dBm
PSM Mode		
AT+CPSMS=1	0.008mA	No current source or sink by any connected pin
GNSS ACTIVE		
GNSS	29 mA	GNSS Standalone 1Hz Acquisition (Non-Dpo)
GNSS	30 mA	GNSS Standalone 1Hz Tracking (Non-DPO)
GPS	28 mA	GPS Standalone 1Hz Acquisition (Non-Dpo)
GPS	29 mA	GPS Standalone 1Hz Tracking (Non-DPO)

4.2.1. Current consumption plots



Current Consumption in LTE data call CAT M1

Current Consumption in GPRS 1 slot TX



NOTE: The electrical design for the Power supply should be made ensuring it will be capable of a peak current output of at least:

0.6 A for LTE mode (3.80V supply).

2A for GPRS mode (3.80V supply).

NOTE: The reported LTE values are an average among all the product variants and bands for each network wireless technology.

The support of specific network wireless technology depends on product variant configuration.

4.3. General Design Rules

The principal guidelines for the Power Supply Design embrace three different design steps:

- the electrical design of the power supply
- the thermal design
- the PCB layout

4.3.1. Electrical Design Guidelines

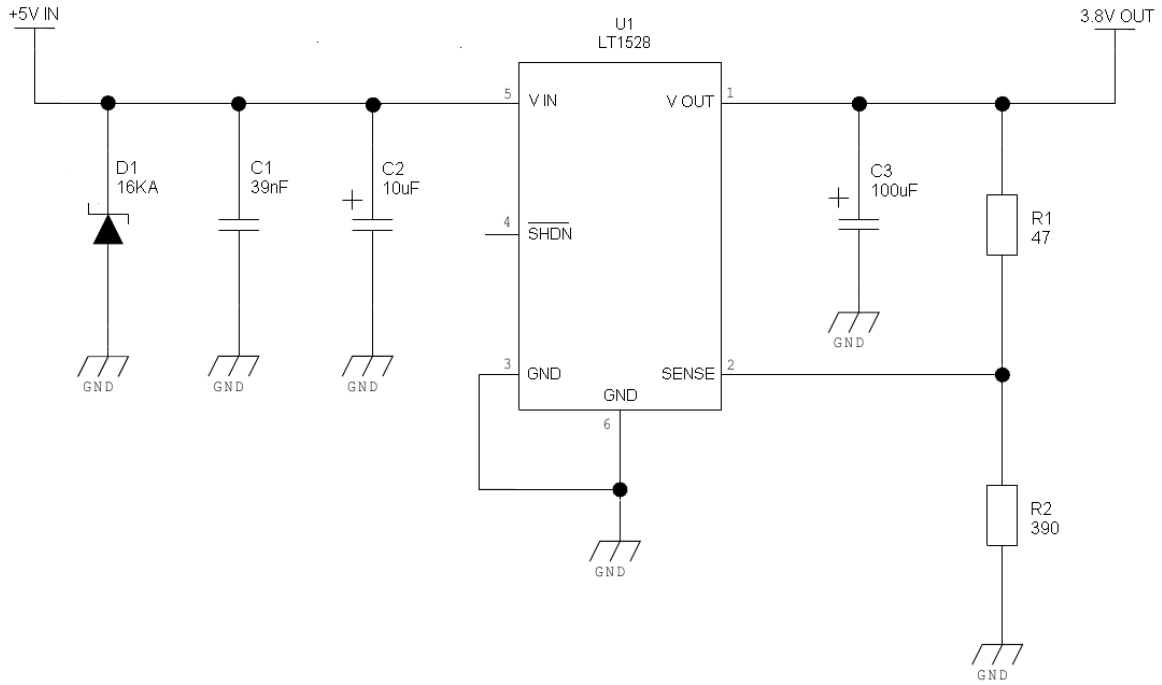
The electrical design of the power supply depends strongly from the power source where this power is drained. We will distinguish them into three categories:

- +5V input (typically PC internal regulator output)
- +12V input (typically automotive)
- Battery

4.3.1.1. +5V Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, hence there's not a big difference between the input source and the desired output and a linear regulator can be used. A switching power supply will not be suited because of the low drop out requirements.
- When using a linear regulator, a proper heat sink shall be provided in order to dissipate the power generated.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks close to the ML865C1, a 100µF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- A protection diode should be inserted close to the power input, in order to save the ML865C1 from power polarity inversion.

An example of linear regulator with 5V input is:

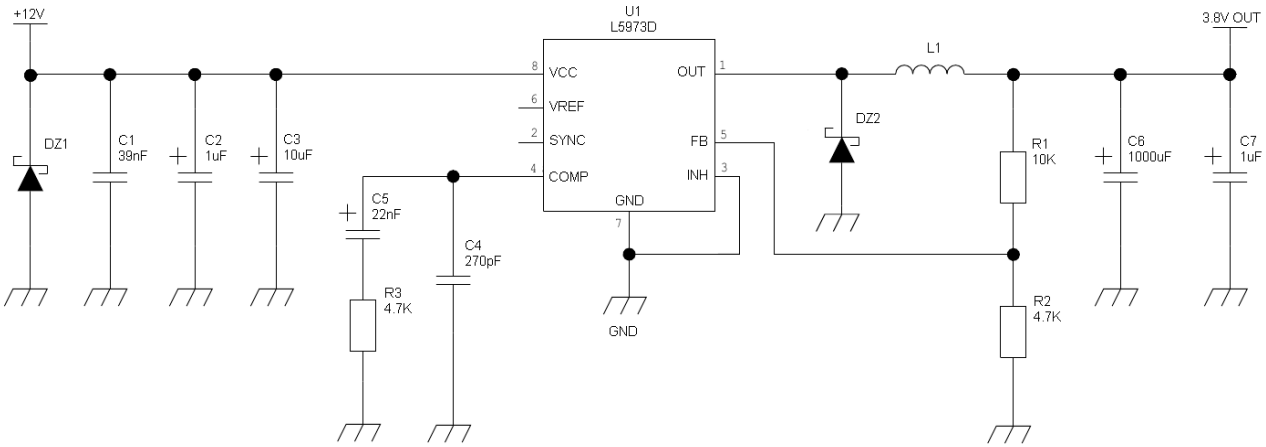


4.3.1.2. +12V Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, hence due to the big difference between the input source and the desired output, a linear regulator is not suited and shall not be used. A switching power supply will be preferable because of its better efficiency especially with the 2A peak current load represented by the ML865C1.
- When using a switching regulator, a 500kHz or more switching frequency regulator is preferable because of its smaller inductor size and its faster transient response. This allows the regulator to respond quickly to the current peaks absorption.
- In any case the frequency and Switching design selection is related to the application to be developed due to the fact the switching frequency could also generate EMC interferences.
- For car PB battery the input voltage can rise up to 15,8V and this should be kept in mind when choosing components: all components in the power supply must withstand this voltage.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100µF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- For Car applications a spike protection diode should be inserted close to the power input, in order to clean the supply from spikes.

- A protection diode should be inserted close to the power input, in order to save the ML865C1 from power polarity inversion. This can be the same diode as for spike protection.

An example of switching regulator with 12V input is in the below schematic:



4.3.1.3. Battery Source Power Supply Design Guidelines

A single 3.7V Li-Ion cell battery type is suited for supply of Telit ML865C1 module.

WARNING:

The three cells Ni/Cd or Ni/MH 3,6 V Nom. battery types or 4V PB types ***MUST NOT BE USED DIRECTLY*** since their maximum voltage can rise over the absolute maximum voltage for the ML865C1 and damage it.

NOTE:

DON'T USE any Ni-Cd, Ni-MH, and Pb battery types directly connected with ML865C1. Their use can lead to overvoltage on the ML865C1 and damage it. USE ONLY Li-Ion battery types.

- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100µF tantalum capacitor is usually suited.

- Make sure the low ESR capacitor (usually a tantalum one) is rated at least 10V.
- A protection diode should be inserted close to the power input, in order to save the ML865C1 from power polarity inversion. Otherwise the battery connector should be done in a way to avoid polarity inversions when connecting the battery.
- The battery capacity must be at least 500mAh in order to withstand the current peaks of 2A; the suggested capacity is from 500mAh to 1000mAh.

4.3.2. Thermal Design Guidelines

The thermal design for the power supply heat sink should be done with the following specifications:

- Average current consumption: 250 mA (LTE modes)
- Average current consumption: 600 mA (GPRS and EDGE modes)
- Supply voltage: 4.50V

NOTE:
Make PCB design in order to have the best connection of GND pads to large surfaces of copper.

NOTE:
The ML865C1 includes a function to prevent overheating.

4.3.3. Power Supply PCB layout Guidelines

As seen on the electrical design guidelines the power supply shall have a low ESR capacitor on the output to cut the current peaks and a protection diode on the input to protect the supply from spikes and polarity inversion. The placement of these components is crucial for the correct working of the circuitry. A misplaced component can be useless or can even decrease the power supply performances.

- The Bypass low ESR capacitor must be placed close to the Telit ML865C1 power input pads or in the case the power supply is a switching type it can be placed close to the inductor to cut the ripple provided the PCB trace from the capacitor to the ML865C1 is wide enough to ensure a dropless connection even during the 2A current peaks.

- The protection diode must be placed close to the input connector where the power source is drained.

- The PCB traces from the input connector to the power regulator IC must be wide enough to ensure no voltage drops occur when the 2A current peaks are absorbed. Note that this is not made in order to save power loss but especially to avoid the voltage drops on the power line at the current peaks frequency of 216 Hz that will reflect on all the components connected to that supply, introducing the noise floor at the burst base frequency. For this reason while a voltage drop of 300-400 mV may be acceptable from the power loss point of view, the same voltage drop may not be acceptable from the noise point of view. If your application doesn't have audio interface but only uses the data feature of the Telit ML865C1, then this noise is not so disturbing and power supply layout design can be more forgiving.

- The PCB traces to the ML865C1 and the Bypass capacitor must be wide enough to ensure no significant voltage drops occur when the 2A current peaks are absorbed. This is for the same reason as previous point. Try to keep this trace as short as possible.

- The PCB traces connecting the Switching output to the inductor and the switching diode must be kept as short as possible by placing the inductor and the diode very close to the power switching IC (only for switching power supply). This is done in order to reduce the radiated field (noise) at the switching frequency (100-500 kHz usually).

- The use of a good common ground plane is suggested.

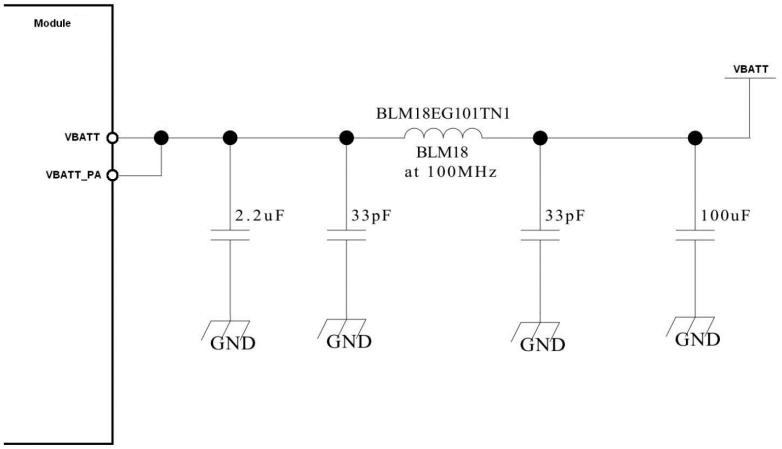
- The placement of the power supply on the board should be done in such a way to guarantee that the high current return paths in the ground plane are not overlapped to any noise sensitive circuitry as the microphone amplifier/buffer or earphone amplifier.

- The power supply input cables should be kept separate from noise sensitive lines such as microphone/earphone cables.

- The insertion of EMI filter on VBATT pins is suggested in those designs where antenna is placed close to battery or supply lines.

  A ferrite bead like Murata BLM18EG101TN1 or Taiyo Yuden P/N FBMH1608HM101 can be used for this purpose.

  The below figure shows the recommended circuit:



4.4. RTC supply

RTC is functional when ML865C1 is in PSM state and VBATT pin is supplied.

RTC settings are erased if VBATT supply is temporary disconnected.

4.5. VAUX Power Output

A regulated power supply output is provided in order to supply small devices from the module, like: level translators, audio codec, sensors, and others.

Pin R11 can be used also as PWRMON (module powered ON indication) function, because is always active when the module is powered ON and cannot be set to LOW level by any AT command.

Host can only detect deep sleep mode by monitoring of VAUX/PWRMON output pin, since there is no pin dedicated to PSM status indicator,

The operating range characteristics of the supply are:

Item	Min	Typical	Max
Output voltage	1.78V	1.80V	1.82V
Output current	-	-	60mA
Output bypass capacitor (inside the module)		1uF	

If power saving configuration is enabled by AT+CPSMS Command, VAUX during deep sleep mode period is OFF

5. DIGITAL SECTION

5.1. Logic Levels

Parameter	Min	Max
ABSOLUTE MAXIMUM RATINGS – NOT FUNCTIONAL		
Input level on any digital pin (CMOS 1.8) with respect to ground	-0.3V	2.1V
Operating Range - Interface levels (1.8V CMOS)		
Input high level	1.5V	1.9V
Input low level	0V	0.35V
Output high level	1.6V	1.9V
Output low level	0V	0.2V

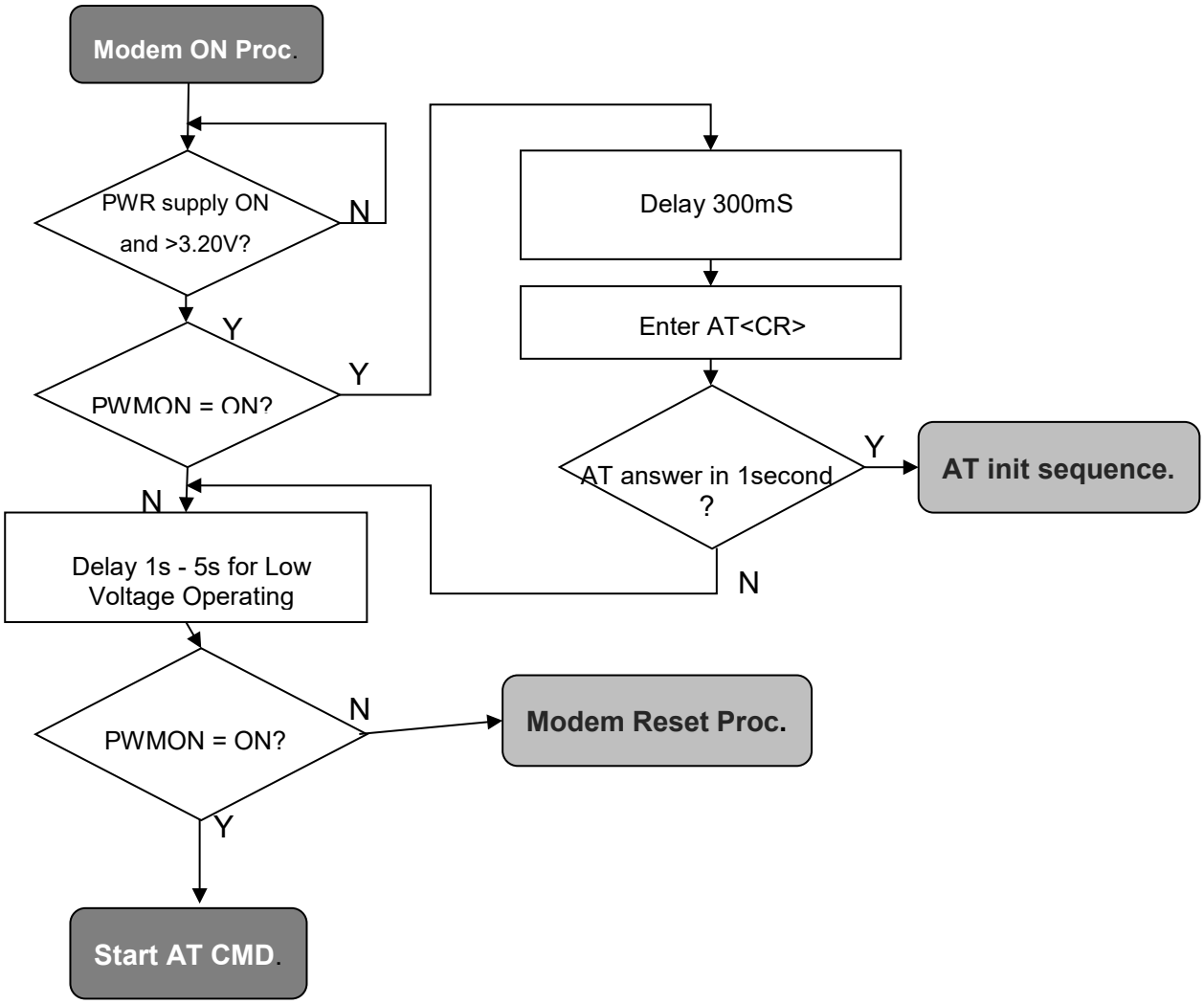
Parameter	AVG
CURRENT CHARACTERISTICS:	
Output Current	1mA
Input Current	1uA

5.2. Power On (Auto-Turning ON ML865)

The ML865C1 will automatically power on itself when VBATT & VBATT_PA are applied to the module.

V_AUX / PWRMON pin will be at the high logic level and the module can be considered fully operating after 5 seconds.

The following flow chart shows the proper turn on procedure:



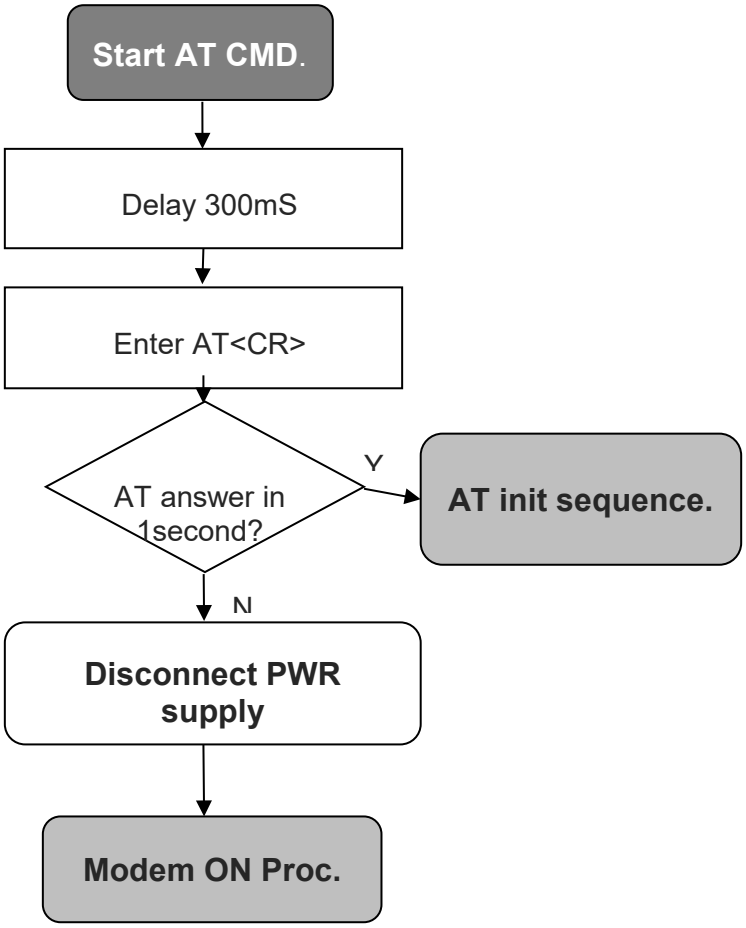
NOTE:

The power supply must be applied either at the same time on pins VBATT and VBATT_PA.

NOTE:

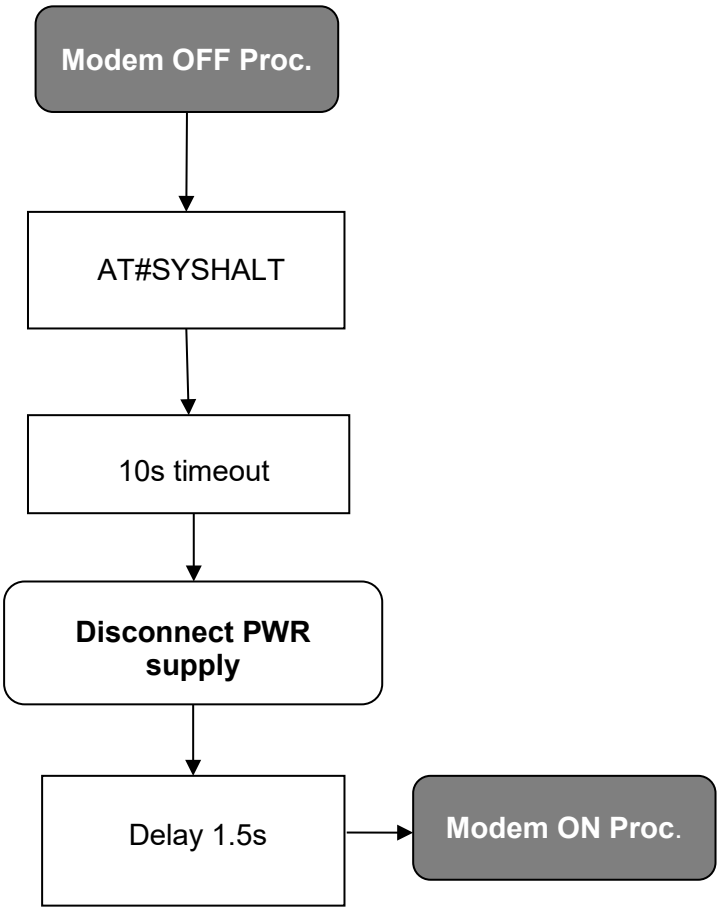
In order to prevent a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the ML865C1 when the module is powered OFF or during an ON/OFF transition.

A flow chart showing the AT commands managing procedure is displayed below:



5.3. Power Off

The following flow chart shows the proper turnoff procedure:



NOTE:

In order to prevent a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the ML865C1 when the module is powered off or during an ON/OFF transition.

5.4. Wake from deep sleep mode

ML865C1 supports Power Saving Mode (PSM) functionality defined in 3GPP Release 12.

When Periodic Update Timer expires, ML910C1 power off until the next scheduled wake-up time.

Asynchronous event controlled by host can wake up from deep sleep mode by asserting WAKE pin HIGH for at least 5 seconds.

Host can detect deep sleep mode by polling VAUX/PWRMON pin.

5.5. Unconditional Shutdown (Hardware Unconditional restart)

HW_SHUTDOWN* is used to unconditionally shutdown the ML865C1. Whenever this signal is pulled low, the ML865C1 is reset. When the device is reset it stops any operation. After the release of the line, the ML865C1 is unconditionally shut down, without doing any detach operation from the network where it is registered. This behaviour is not a proper shut down because any cellular device is requested to issue a detach request on turn off. The HW_SHUTDOWN* is internally controlled on start-up to achieve always a proper power-on reset sequence, so there's no need to control this pin on start-up.
To unconditionally shutdown the ML865C1, the pad HW_SHUTDOWN* must be tied low for at least 200 milliseconds and then released. The maximum current that can be drained from the ON* pad is 0,15 mA.
The signal is internally pulled up so the pin can be left floating if not used.

During PSM mode, HW_SHUTDOWN toggle has no effect. The use of HW_SHUTDOWN* pin is valid only when ML865C1 has VAUX/PWRMON output HI.

WARNING:

The hardware unconditional Restart must not be used during normal operation of the device since it does not detach the device from the network. It shall be kept as an emergency exit procedure to be done in the rare case that the device gets stuck waiting for some network or SIM responses.

NOTE:

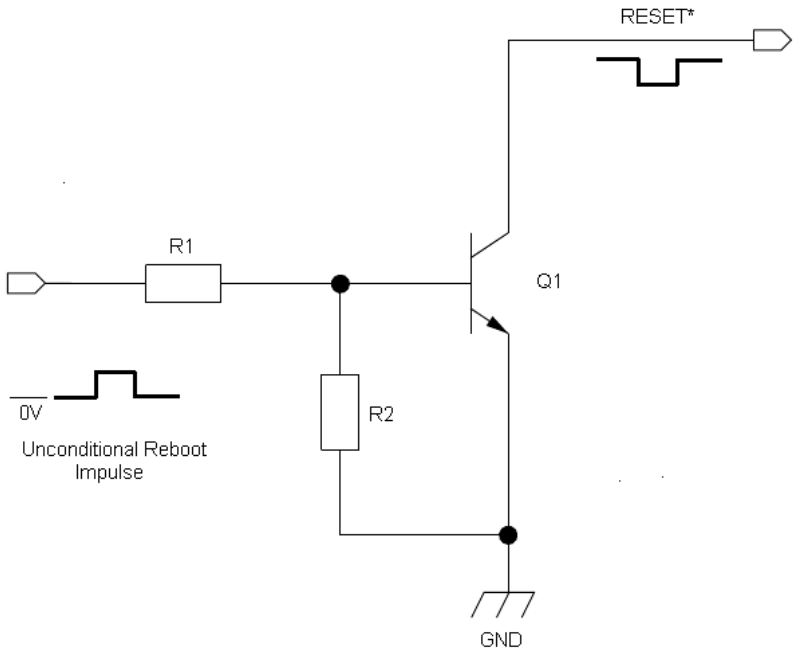
Do not use any pull up resistor on the HW_SHUTDOWN* line nor any totem pole digital output.

The line HW_SHUTDOWN* must be connected only in open collector configuration; the transistor must be connected as close as possible to the HW_SHUTDOWN* pin.

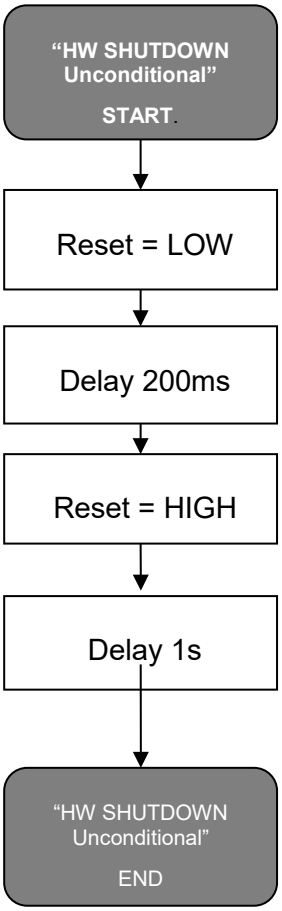
TIP:

The unconditional hardware restart must always be implemented on the boards and the software must use it as an emergency exit procedure.

A simple circuit to do it is:



In the following flow chart is detailed the proper restart procedure:



NOTE:

In order to prevent a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the ML865C1 when the module is powered OFF or during an ON/OFF transition.

5.6. Fast power down

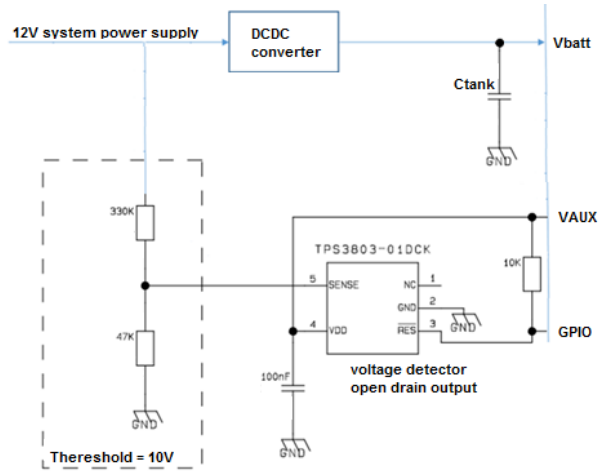
The procedure to power off ML865C1 described in Chapter 5.3 normally takes more than 1 second to detach from network and make ML865C1internal filesystem properly closed.
In case of unwanted supply voltage loss the system can be switched off without any risk of filesystem data corruption by implementing Fast Shut Down feature.
Fast Shut Down feature permits to reduce the current consumption and the time-to-poweroff to minimum values.

NOTE:
Refer to ML865C1 series AT command reference guide (Fast power down - #FASTSHDN) in order to set up detailed AT command.

5.6.1. Fast Shut Down by Hardware

The Fast Power Down can be triggered by configuration of any GPIO. HI level to LOW level transition of GPIO commands fast power down.

Example circuit:



NOTE:
Consider voltage drop under max current conditions when defining the voltage detector thereshold in order to avoid unwanted shutdown.

The capacitor is rated with the following formula:

$$C = I \frac{\Delta t}{\Delta V}$$

TIP:
Make the same plot during system verification to check timings and voltage levels.

5.6.2. Fast Shut Down by Software

The Fast Power Down can be triggered by AT command.

5.7. Communication ports

5.7.1. USB 2.0 HS

The ML865C1 includes one integrated universal serial bus (USB 2.0 HS) transceiver. The following table is listing the available signals:

PAD	Signal	I/O	Function	NOTE
19	USB_D+	I/O	USB differential Data (+)	
20	USB_D-	I/O	USB differential Data (-)	

18	VUSB	AI	Power sense for the internal USB transceiver.	Accepted range: 3.0V to 5.5V 100K pull down

The USB_DPLUS and USB_DMINUS signals have a clock rate of 480 MHz, therefore signal traces should be routed carefully. Trace lengths, number of vias and capacitive loading should be minimized. The characteristic impedance value should be as close as possible to 90 Ohms differential.
ESD protection can be added to USB D+/D- lines in case of external connector for cable connection.
Proper components for USB 2.0 must be used.

NOTE:
Disconnect or assert to GND the VUSB pin before activating the Power Saving Mode.

5.7.2. SPI

The ML865C1 Module is provided by a standard 3-wire master SPI interface + chip select control.

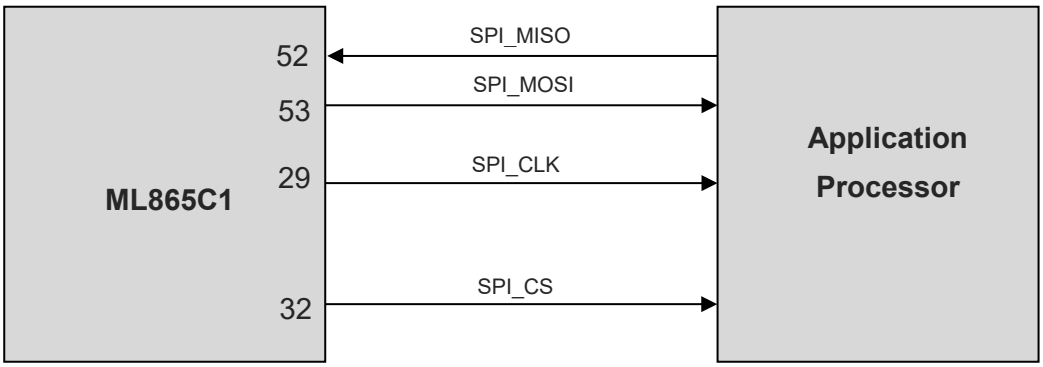
The following table is listing the available signals:

PAD	Signal	I/O	Function	Type	NOTE
29	SPI_CLK	O	SPI Clock	CMOS 1.8V	
52	SPI_MISO	I	SPI MISO	CMOS 1.8V	Shared with RX_AUX
53	SPI_MOSI	O	SPI MOSI	CMOS 1.8V	Shared with TX_AUX
32	SPI_CS	O	SPI Chip Select	CMOS 1.8V	

NOTE:
Due to the shared functions, SPI port and TX_AUX/RX_AUX port cannot be used simultanously.

Refer to ML865C1 series AT command reference guide for port configuration.

SPI Connections



5.7.3. Serial Ports

The ML865C1 module is provided with by 2 Asynchronous serial ports:

- MODEM SERIAL PORT 1 (Main)
- MODEM SERIAL PORT 2 (Auxiliary)

Several configurations can be designed for the serial port on the OEM hardware, but the most common are:

- RS232 PC com port
- microcontroller UART @ 1.8V (Universal Asynchronous Receive Transmit)
- microcontroller UART @ 5V or other voltages different from 1.8V

Depending from the type of serial port on the OEM hardware a level translator circuit may be needed to make the system work. On the ML865C1 the ports are CMOS 1.8.

5.7.3.1. Modem serial port 1

The serial port 1 on the ML865C1 is a +1.8V UART with all the 7 RS232 signals. It differs from the PC-RS232 in the signal polarity (RS232 is reversed) and levels.

The following table is listing the available signals:

RS232 Pin	Signal	ML865C1 PAD	Name	Usage
1	C109/DCD	**1**	Data Carrier Detect	Output from the ML865C1 that indicates the carrier presence
2	C104/RXD	**10**	Transmit line *see Note	Output transmit line of ML865C1 UART
3	C103/TXD	**9**	Receive line *see Note	Input receive of the ML865C1 UART
4	C108/DTR	**4**	Data Terminal Ready	Input to the ML865C1 that controls the DTE READY condition
6	C107/DSR	**3**	Data Set Ready	Output from the ML865C1 that indicates the module is ready
7	C106/CTS	**5**	Clear to Send	Output from the ML865C1 that controls the Hardware flow control
8	C105/RTS	**6**	Request to Send	Input to the ML865C1 that controls the Hardware flow control
9	C125/RING	**2**	Ring Indicator	Output from the ML865C1 that indicates the incoming call condition

NOTE:
According to V.24, some signal names are referred to the application side, therefore on the ML865C1 side these signal are on the opposite direction:
TXD on the application side will be connected to the receive line (here named C103/TXD)
RXD on the application side will be connected to the transmit line (here named C104/RXD)

For a minimum implementation, only the TXD, RXD lines can be connected, the other lines can be left open provided a software flow control is implemented.

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the ML865C1 when the module is powered off or during an ON/OFF transition.

5.7.3.2. Modem serial port 2

The secondary serial port on the ML865C1 is a CMOS1.8V with only the RX and TX signals.
The signals of the ML865C1 serial port are:

PAD	Signal	I/O	Function	Type	NOTE
53	TX_AUX	O	Auxiliary UART (TX Data to DTE)	CMOS 1.8V	Shared with SPI_MOSI
52	RX_AUX	I	Auxiliary UART (RX Data from DTE)	CMOS 1.8V	Shared with SPI_MISO

NOTE:
Due to the shared functions, TX_AUX/RX_AUX port and SPI port cannot be used simultanously.

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the ML865C1 when the module is powered off or during an ON/OFF transition.

Refer to ML865C1 series AT command reference guide for port configuration.

5.7.3.3. RS232 level translation

In order to interface the ML865C1 with a PC com port or a RS232 (EIA/TIA-232) application a level translator is required. This level translator must:

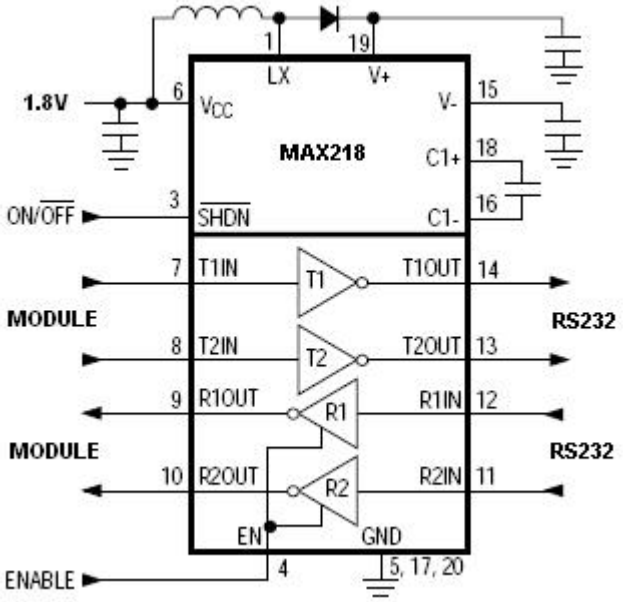
- invert the electrical signal in both directions;
- Change the level from 0/1.8V to +15/-15V.

Actually, the RS232 UART 16450, 16550, 16650 & 16750 chipsets accept signals with lower levels on the RS232 side (EIA/TIA-562), allowing a lower voltage-multiplying ratio on the level translator. Note that the negative signal voltage must be less than 0V and hence some sort of level translation is always required.
The simplest way to translate the levels and invert the signal is by using a single chip level translator. There are a multitude of them, differing in the number of drivers and receivers and in the levels (be sure to get a true RS232 level translator not a RS485 or other standards).
By convention the driver is the level translator from the 0-1.8V UART to the RS232 level. The receiver is the translator from the RS232 level to 0-1.8V UART.
In order to translate the whole set of control lines of the UART you will need:

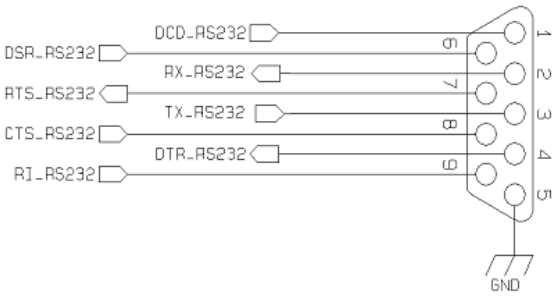
- 5 drivers

- 3 receivers

An example of RS232 level adaptation circuitry could be done using a MAXIM transceiver (MAX218)
In this case the chipset is capable to translate directly from 1.8V to the RS232 levels (Example done on 4 signals only).



The RS232 serial port lines are usually connected to a DB9 connector with the following layout:



5.8. General purpose I/O

The ML865C1 module is provided by a set of Configurable Digital Input / Output pins (CMOS 1.8V). Input pads can only be read; they report the digital value (high or low) present on the pad at the read time. Output pads can only be written or queried and set the value of the pad output.
An alternate function pad is internally controlled by the ML865C1 firmware and acts depending on the function implemented.

The following table shows the available GPIO on the ML865C1:

PAD	Signal	I/O	Output Drive Strength	Default State	NOTE
48	GPIO_01	I/O	1mA	INPUT – PD (100K)	
47	GPIO_02	I/O	1mA	INPUT – PD (100K)	
46	GPIO_03	I/O	1mA	INPUT – PD (100K)	
45	GPIO_04	I/O	1mA	INPUT – PD (100K)	
33	GPIO_05	I/O	1mA	INPUT – PD (100K)	
32	GPIO_06	I/O	1mA	INPUT – PD (100K)	
31	GPIO_07	I/O	1mA	INPUT – PD (100K)	
30	GPIO_08	I/O	1mA	INPUT – PD (100K)	

5.8.1. Using a GPIO as INPUT

The GPIO pads, when used as inputs, can be connected to a digital output of another device and report its status, provided this device has interface levels compatible with the 1.8V CMOS levels of the GPIO.

Input current (@1.8V) is about 18uA (corrisponding to 100K pulldown value) in all GPIO pin expect GPIO_09 where current is about 100uA. This value is present since ML865 poweron.

If the digital output of the device to be connected with the GPIO input pad has interface levels different from the 1.8V CMOS, then it can be buffered with an open collector transistor with a 47K pull up to 1.8V supplied by VAUX/POWERMON R11 pad.

NOTE:
In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the ML865C1 when the module is powered off or during an ON/OFF transition.

Refer to ML865C1 series AT command reference guide for GPIO pins configuration.

5.8.2. Using a GPIO as OUTPUT

The GPIO pads, when used as outputs, can drive 1.8V CMOS digital devices or compatible hardware. When set as outputs, the pads have a push-pull output and therefore the pull-up resistor may be omitted.

5.8.3. Indication of network service availability

The STAT_LED pin status shows information on the network service availability and Call status.
The function is available as alternate function of GPIO_08 (to be enabled using the AT#GPIO=1,0,2 command).

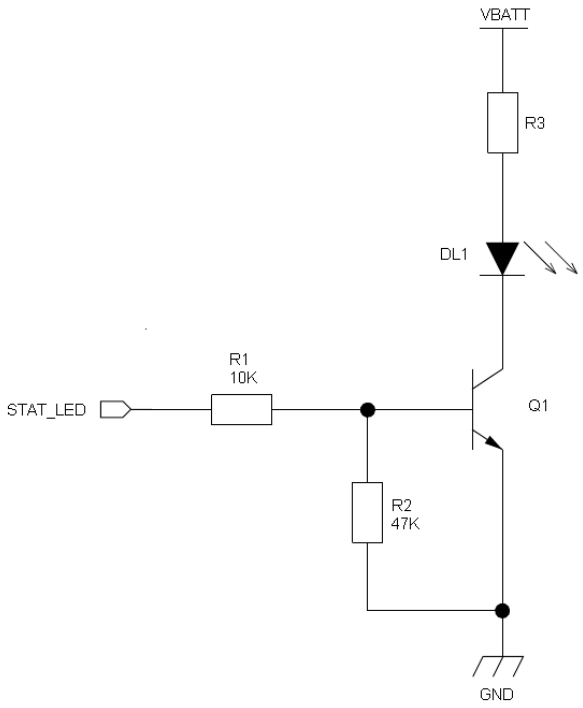
In the ML865C1 modules, the STAT_LED needs an external transistor to drive an external LED and its voltage level is defined accordingly to the table below:.

Device Status	Led Status
Device off	Permanently off
Not Registered	Permanently on
Registered in idle	Blinking 1sec on + 2 sec off

Registered in idle + power saving	It depends on the event that triggers the wakeup (In sync with network paging)
Connecting	Blinking 1 sec on + 2 sec off

The reference schematic for LED indicator,

R3 must be calculated taking in account VBATT value and LED type. :



5.9. External SIM Holder

Please refer to the related User Guide (SIM Holder Design Guides, 80000NT10001a).

5.10. ADC Converter

The ML865C1 is provided by one AD converters. It is able to read a voltage level in the range of 0÷1.8 volts applied on the ADC pin input, store and convert it into 10 bit word. The input lines are named as **ADC_IN1** and they are available on Pad **13**.

The following table is showing the ADC characteristics:

Item	Min	Typical	Max	Unit
Input Voltage range	0	-	1.8	Volt
AD conversion	-	-	10	bits
Input Resistance	1	-	-	Mohm
Input Capacitance	-	1	-	pF

The ADC could be controlled using an AT command.

The command is ***AT#ADC=1,2***

The read value is expressed in mV

Refer to SW User Guide or AT Commands Reference Guide for the full description of this function.

6. RF SECTION

6.1. Bands Variants

Product	LTE bands	2G bands
ML865C1-NA	B2,B4,B12, B13	
ML865C1-EA	B3,B5,B8,B20,B28	850/900/1800/1900

6.2. TX Output power

Band	Class	RF power (dBm)
LTE (UE CAT-M1) all bands	3	23
GSM 850/900	4	33
DCS 1800/PCS 1900	1	30

6.3. RX Sensitivity

Measurement setup

Band	Measurement conditions
LTE (UE CAT-M1)	Throughput >95% According to 3GPP 36. 521-1
2G BANDS	BLER <10%, CS2 According to 3GPP 51.010-1

ML865C1-NA

Band	REFsens (dBm)	3GPP REFsens (dBm)
Band 2	-105	-100.3
Band 4	-105	-102.3
Band 12	-105	-99.3
Band 13	-105	-99.3

ML865C1-EA

Band	REFsens (dBm)	3GPP REFsens (dBm)
Band 3	-105	-99.3
Band 5	-105	-100.8
Band 8	-105	-99.8
Band 20	-105	-100.8
Band 28	-105	-100.8
GSM 900	-107	-104
DCS 1800	-106	-104
GSM 850	-107	-104
GSM 1900	-106	-104

6.4. Antenna requirements

The antenna connection and board layout design are the most important aspect in the full product design as they strongly affect the product overall performances, hence read carefully and follow the requirements and the guidelines for a proper design.
The antenna and antenna transmission line on PCB for a Telit ML865C1 device shall fulfil the following requirements:

ML865C1-NA

Item	Value
Frequency range	Depending by frequency band(s) provided by the network operator, the customer shall use the most suitable antenna for that/those band(s)
Bandwidth	140 MHz in LTE Band 2 445 MHz in LTE Band 4 47 MHz in LTE Band 12 41 MHz in LTE Band 13
Impedance	50 ohm
Input power	> 24dBm Average power
VSWR absolute max	≤ 10:1 (limit to avoid permanent damage)
VSWR recommended	≤ 2:1 (limit to fulfill all regulatory requirements)

ML865C1-EA

Item	Value
Frequency range	Depending by frequency band(s) provided by the network operator, the customer shall use the most suitable antenna for that/those band(s)

Bandwidth	170 MHz in LTE Band 3 70 MHz in LTE Band 5 80 MHz in LTE Band 8 71 MHz in LTE Band 20 110 MHz in LTE Band 28
Impedance	50 ohm
Input power	> 24dBm Average power
VSWR absolute max	≤ 10:1 (limit to avoid permanent damage)
VSWR recommended	≤ 2:1 (limit to fulfill all regulatory requirements)

6.4.1. PCB Design guidelines

When using the ML865C1, since there's no antenna connector on the module, the antenna must be connected to the ML865C1 antenna pad (K1) by means of a transmission line implemented on the PCB.

This transmission line shall fulfil the following requirements:

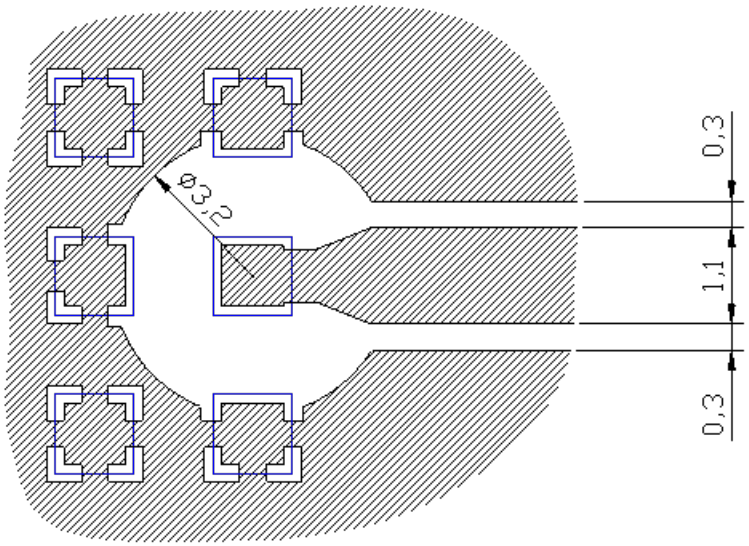
Item	Value
Characteristic Impedance	50 ohm (+-10%)
Max Attenuation	0,3 dB
Coupling	Coupling with other signals shall be avoided
Ground Plane	Cold End (Ground Plane) of antenna shall be equipotential to the ML865C1 ground pins

The transmission line should be designed according to the following guidelines:

- Make sure that the transmission line's characteristic impedance is 50ohm ;

- Keep line on the PCB as short as possible, since the antenna line loss shall be less than about 0,3 dB;
- Line geometry should have uniform characteristics, constant cross section, avoid meanders and abrupt curves;
- Any kind of suitable geometry / structure (Microstrip, Stripline, Coplanar, Grounded Coplanar Waveguide...) can be used for implementing the printed transmission line afferent the antenna;
- If a Ground plane is required in line geometry, that plane has to be continuous and sufficiently extended, so the geometry can be as similar as possible to the related canonical model;
- Keep, if possible, at least one layer of the PCB used only for the Ground plane; If possible, use this layer as reference Ground plane for the transmission line;
- It is wise to surround (on both sides) the PCB transmission line with Ground, avoid having other signal tracks facing directly the antenna line track.
- Avoid crossing any un-shielded transmission line footprint with other signal tracks on different layers;
- The ground surrounding the antenna line on PCB has to be strictly connected to the main Ground Plane by means of via holes (once per 2mm at least), placed close to the ground edges facing line track;
- Place EM noisy devices as far as possible from ML865C1 antenna line;
- Keep the antenna line far away from the ML865C1 power supply lines;
- If EM noisy devices (such as fast switching ICs, LCD and so on) are present on the PCB hosting the ML865, take care of the shielding of the antenna line by burying it in an inner layer of PCB and surround it with Ground planes, or shield it with a metal frame cover.
- If EM noisy devices are not present around the line, the use of geometries like Microstrip or Grounded Coplanar Waveguide has to be preferred, since they typically ensure less attenuation if compared to a Stripline having same length;

The following image is showing the suggested layout for the Antenna pad connection:



6.4.2. PCB Guidelines in case of FCC Certification

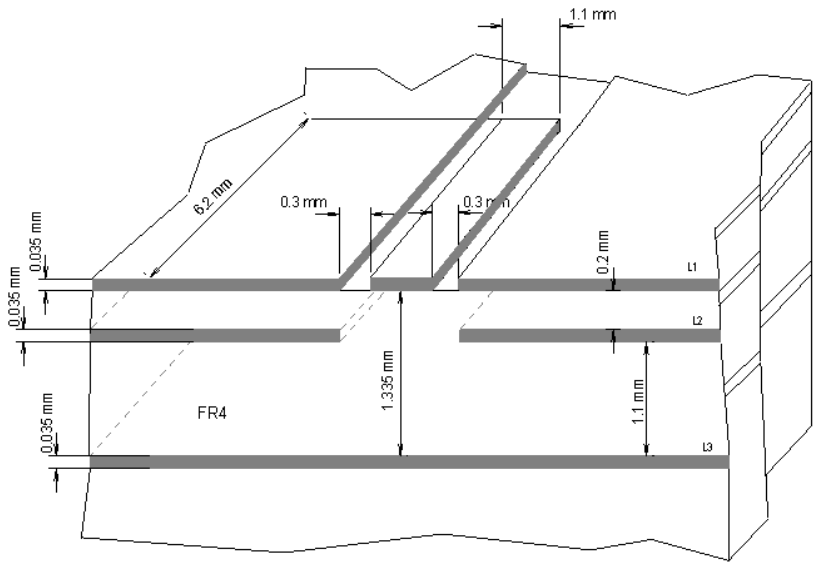
In the case FCC certification is required for an application using ML865C1, according to FCC KDB 996369 for modular approval requirements, the transmission line has to be similar to that implemented on ML865C1 interface board and described in the following chapter.

6.4.2.1. Transmission line design

During the design of the ML865C1 interface board, the placement of components has been chosen properly, in order to keep the line length as short as possible, thus leading to lowest power losses possible. A Grounded Coplanar Waveguide (G-CPW) line has been chosen, since this kind of transmission line ensures good impedance control and can be implemented in an outer PCB layer as needed in this case. A SMA female connector has been used to feed the line.

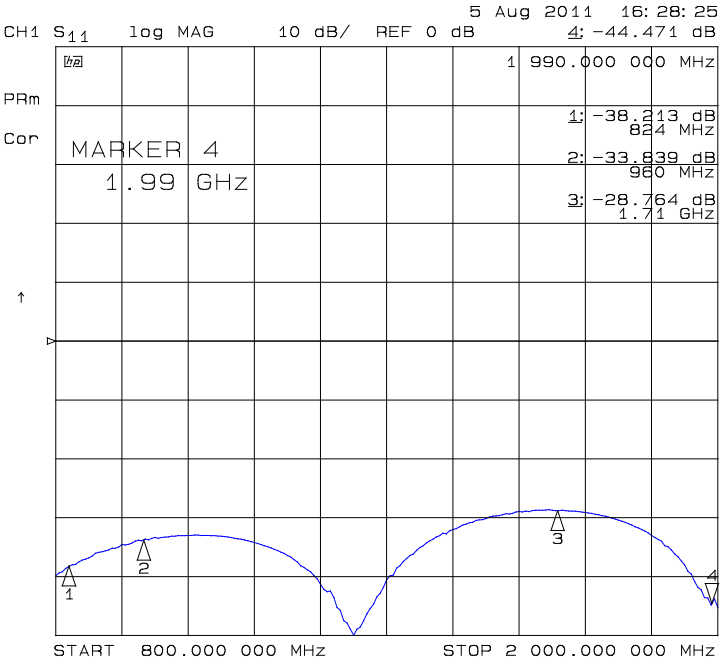
The interface board is realized on a FR4, 4-layers PCB. Substrate material is characterized by relative permittivity εr = 4.6 ± 0.4 @ 1 GHz, TanD= 0.019 ÷ 0.026 @ 1 GHz.

A characteristic impedance of nearly 50 Ω is achieved using trace width = 1.1 mm, clearance from coplanar ground plane = 0.3 mm each side. The line uses reference ground plane on layer 3, while copper is removed from layer 2 underneath the line. Height of trace above ground plane is 1.335 mm. Calculated characteristic impedance is 51.6 Ω, estimated line loss is less than 0.1 dB. The line geometry is shown below:

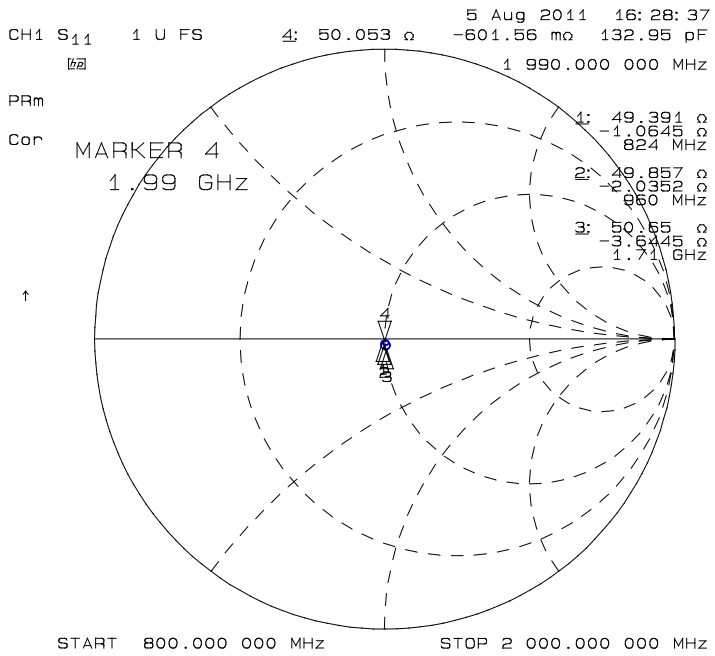


6.4.2.2. Transmission Line Measurements

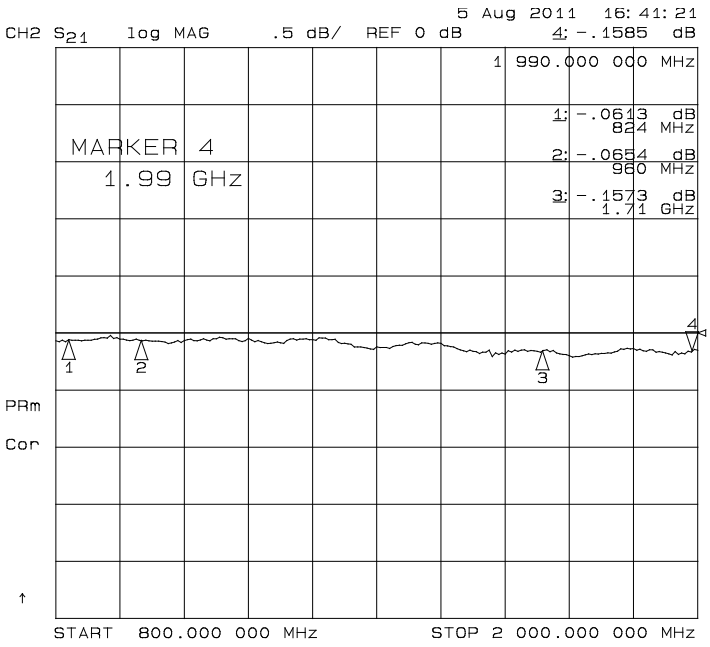
An HP8753E VNA (Full-2-port calibration) has been used in this measurement session. A calibrated coaxial cable has been soldered at the pad corresponding to RF output; a SMA connector has been soldered to the board in order to characterize the losses of the transmission line including the connector itself. During Return Loss / impedance measurements, the transmission line has been terminated to 50 Ω load.
Return Loss plot of line under test is shown below:



Line input impedance (in Smith Chart format, once the line has been terminated to 50 Ω load) is shown in the following figure:



Insertion Loss of G-CPW line plus SMA connector is shown below:



6.4.2.3. Antenna Installation Guidelines

- Install the antenna in a place covered by the LTE signal with CAT-M1 support.
- Antenna must not be installed inside metal cases
- Antenna must not be installed according Antenna manufacturer instructions
- Antenna integration should optimize the Radiation Efficiency. Efficiency values > 50% are recommended on all frequency bands
- Antenna integration should not perturb the radiation pattern described in Antenna manufacturer documentation.
- It is preferable to get an omnidirectional radiation pattern to
- Antenna Gain must not exceed values indicated in regulatory requirements, where applicable, in order to meet related EIRP limitations. Typical antenna Gain in most M2M applications does not exceed 2dBi
- If the device antenna is located farther than 20cm from the human body and there are no co-located transmitter then the Telit FCC/IC approvals can be re-used by the end product
- If the device antenna is located closer than 20cm from the human body or there are co-located transmitter then the additional FCC/IC testing may be required for the end product (Telit FCC/IC approvals cannot be reused)

7. AUDIO SECTION

The Telit digital audio interface (DVI) of the ML865C1 Module is based on the I^2S serial bus interface standard. The audio port can be connected to end device using digital interface, or via one of the several compliant codecs (in case an analog audio is needed).

7.1. Electrical Characteristics

The product is providing the DVI on the following pins:

Pin	Signal	I/O	Function	Type
48	DVI_WA0	O	Digital Audio Interface (Word Alignment / LRCLK)	CMOS 1.8V
47	DVI_RX	I	Digital Audio Interface (RX)	CMOS 1.8V
46	DVI_TX	O	Digital Audio Interface (TX)	CMOS 1.8V
45	DVI_CLK	O	Digital Audio Interface (BCLK)	CMOS 1.8V

7.2. Codec examples

Please refer to the Digital Audio Application note.

8. GNSS SECTION

ML865C1 module includes a state-of-art receiver that can simultaneously search and track satellite signals from multiple satellite constellations. This multi-GNSS receiver uses the entire spectrum of GNSS systems available: GPS, GLONASS, BeiDou, Galileo, and QZSS.

8.1. GNSS Signals Pin-out

Pin	Signal	I/O	Function	Type
37	ANT_GNSS	I	GNSS Antenna (50 ohm)	CMOS 1.8V
33	GNSS_LNA_EN	O	GNSS External LNA Enable	

8.2. RF Front End Design

The ML865C1 Module contains a pre-select SAW filter but doesn't contain the LNA needed to reach the maximum sensitivity. Active antenna (antenna with a built-in low noise amplifier) must be used and must be supplied with proper bias-tee circuit.

8.2.1. Guidelines of PCB line for GNSS Antenna

- Ensure that the antenna line impedance is 50ohm.
- Keep the antenna line on the PCB as short as possible to reduce the loss.
- Antenna line must have uniform characteristics, constant cross section, avoid meanders and abrupt curves.
- Keep one layer of the PCB used only for the Ground plane, if possible.
- Surround (on both the sides, over and under) the antenna line on PCB with Ground, avoid having other signal tracks facing directly the antenna line of track.
- The ground around the antenna line on PCB has to be strictly connected to the Ground Plane by placing vias once per 2mm at least.
- Place EM noisy devices as far as possible from antenna line.
- Keep the antenna line far away from power supply lines.
- Keep the antenna line far away from GSM RF lines.
- If you have EM noisy devices around the PCB hosting the module, such as fast switching ICs, take care of the shielding of the antenna line by burying it inside the layers of PCB and surround it with Ground planes, or shield it with a metal frame cover.
- If you do not have EM noisy devices around the PCB hosting the module, use a strip-line on the superficial copper layer for the antenna line. The line attenuation will be lower than a buried one.

8.3. GNSS Antenna Requirements

GNSS active antenna must be used or integrated in the application.

8.3.1. GNSS Antenna specification

Item	Value
Frequency range	1559.0 ~ 1610.0 MHz
Gain	20 ~ 30dB
Impedance	50 ohm
Noise Figure of LNA	< 1.5 (recommended)
DC supply voltage	DC 1.8 ~ 3.3V
VSWR	≤ 3:1 (recommended)

8.3.2. GNSS Antenna – Installation Guidelines

- The antenna must be installed according to the antenna manufacturer's instructions to obtain the maximum performance of GNSS receiver.
- The antenna location must be evaluated carefully if operating in conjunction with any other antenna or transmitter.
- The antenna must not be installed inside metal cases or near any obstacle that may degrade features like antenna lobes and gain.

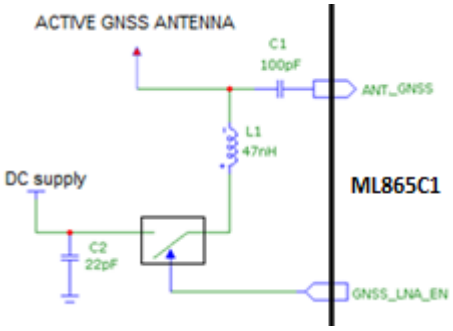
8.3.3. Powering the External LNA (active antenna)

The LNA of active antenna needs a source of power because 1.8V or 3V DC voltage needed by active antenna is not supplied by the ML865C1 module, but can be easily included by the host design.

The electrical characteristics of the GPS_LNA_EN signal are:

Level	Min [V]	Max [V]
Output High Level	1.6	1.9
Output Low Level	0V	0.3

Example of external antenna bias circuitry:



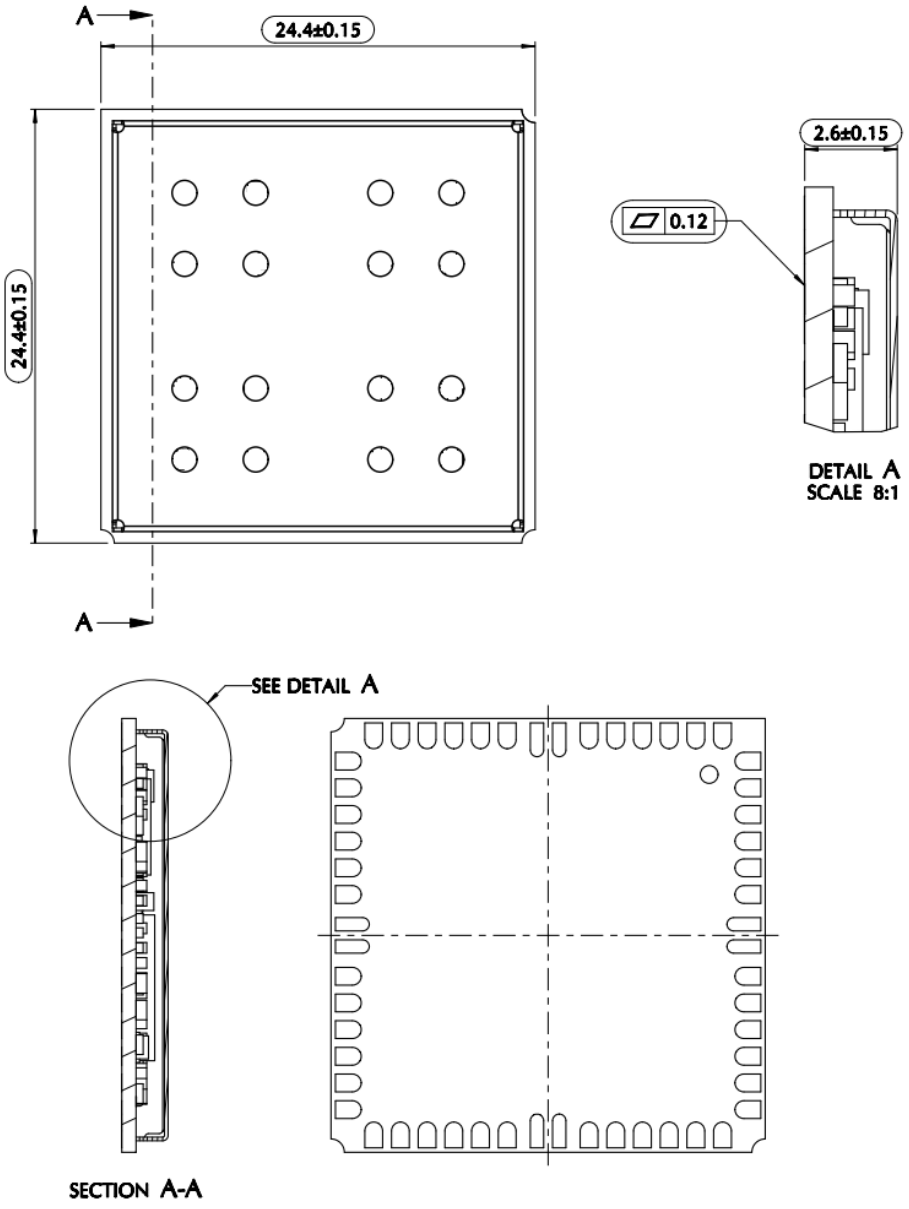
8.4. GNSS Characteristics *

The table below specifies the GNSS characteristics and expected performance
The values are related to typical environment and conditions Table 1 GNSS Characteristics
(* external LNA)

Parameters		Typical Measurement	Notes
Sensitivity	Standalone or MS Based Tracking Sensitivity	-161 dBm	
	Navigation	-158 dBm	
	Cold Start Sensitivity	-146 dBm	
TTFF	Hot	<1s	GNSS Simulator test
	Warm	21s	GNSS Simulator test
	Cold	32s	GNSS Simulator test
Min Navigation update rate		1Hz	
Dynamics		2g	
A-GPS		Supported	

9. MECHANICAL DESIGN

9.1. Drawing



NOTE:

Dimensions in mm.

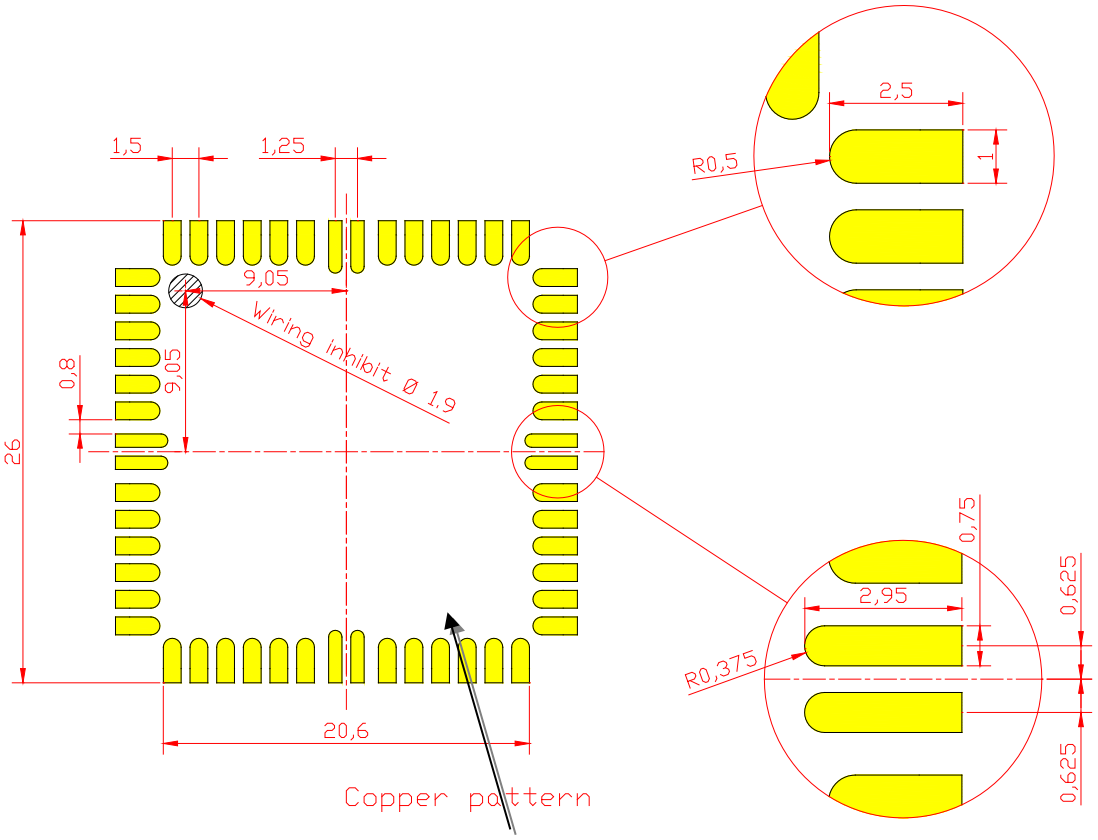
General Tolerance ±0.1, Angular Tolerance ±1°, The tolerance is not cumulative.

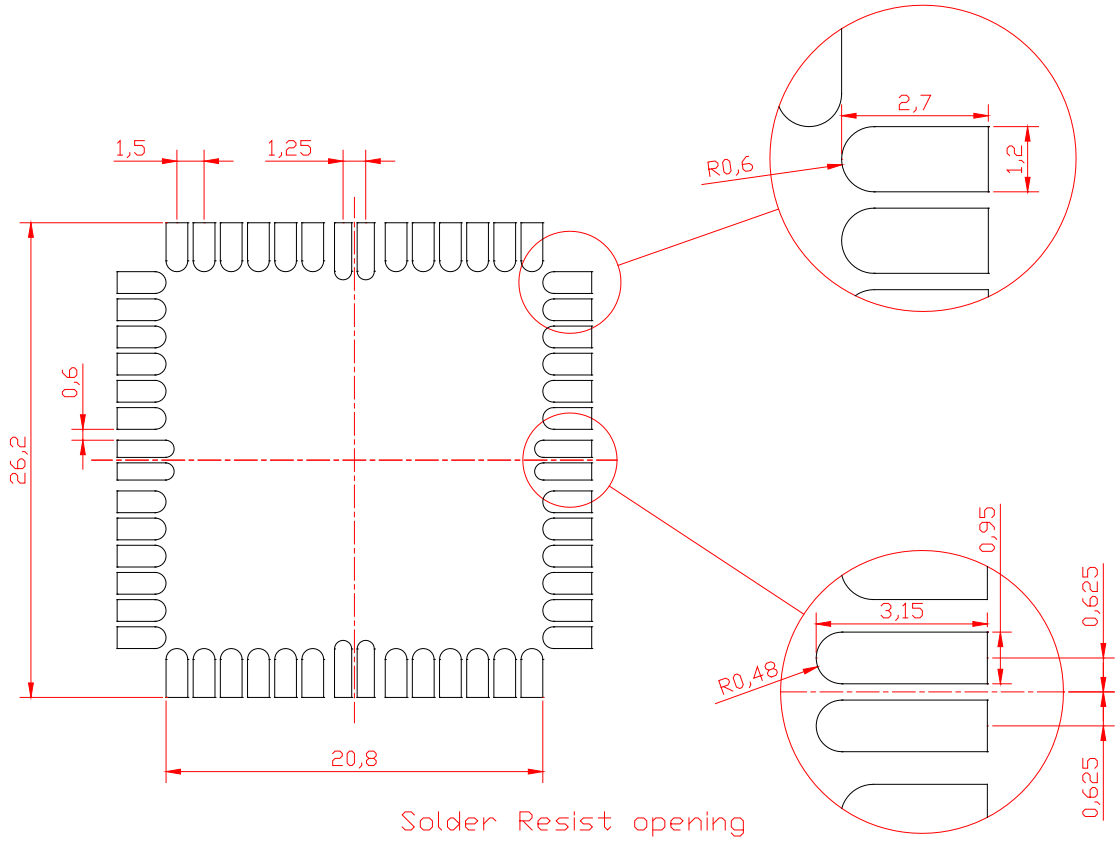
10. APPLICATION PCB DESIGN

10.1. General

The ML865C1 modules have been designed to be compliant with a standard lead-free SMT process.

10.2. Footprint





In order to easily rework the ML865C1 is suggested to consider on the application a 1.5 mm placement inhibit area around the module.

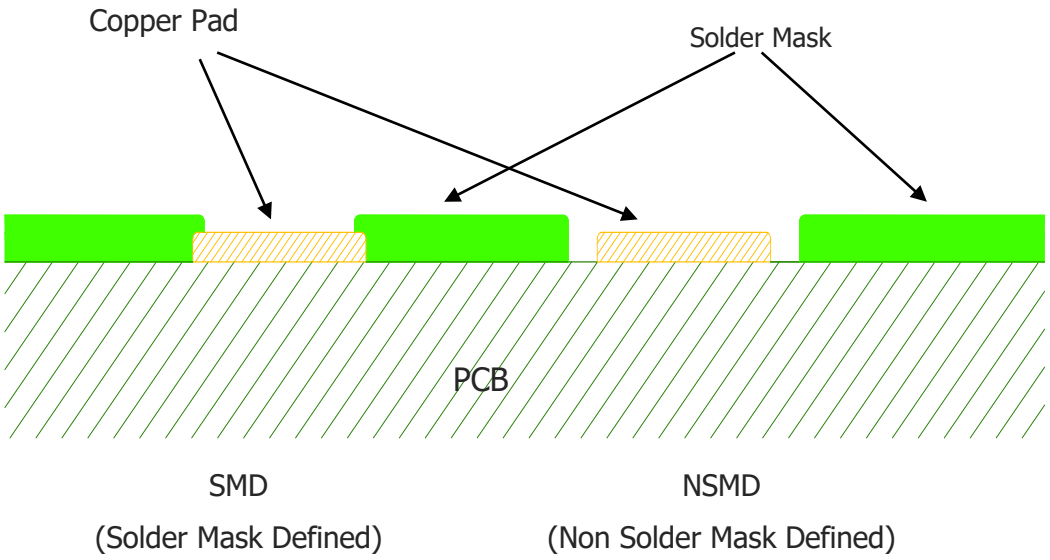
It is also suggested, as common rule for an SMT component, to avoid having a mechanical part of the application in direct contact with the module.

NOTE:

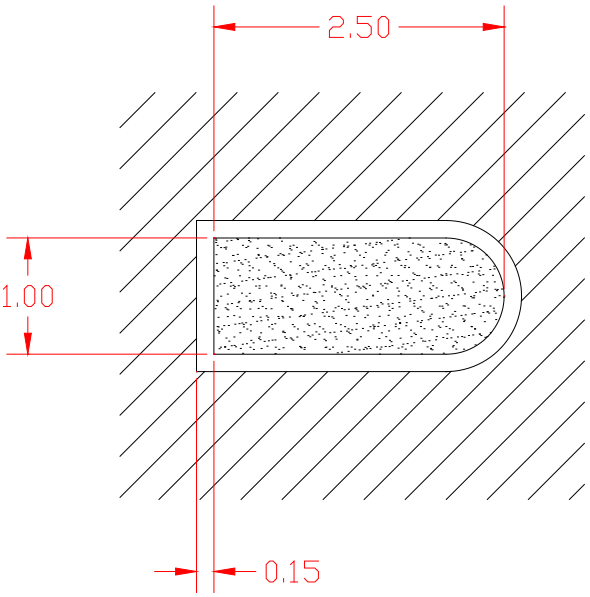
In the customer application, the region under WIRING INHIBIT (see figure above) must be clear from signal or ground paths.

10.3. PCB pad design

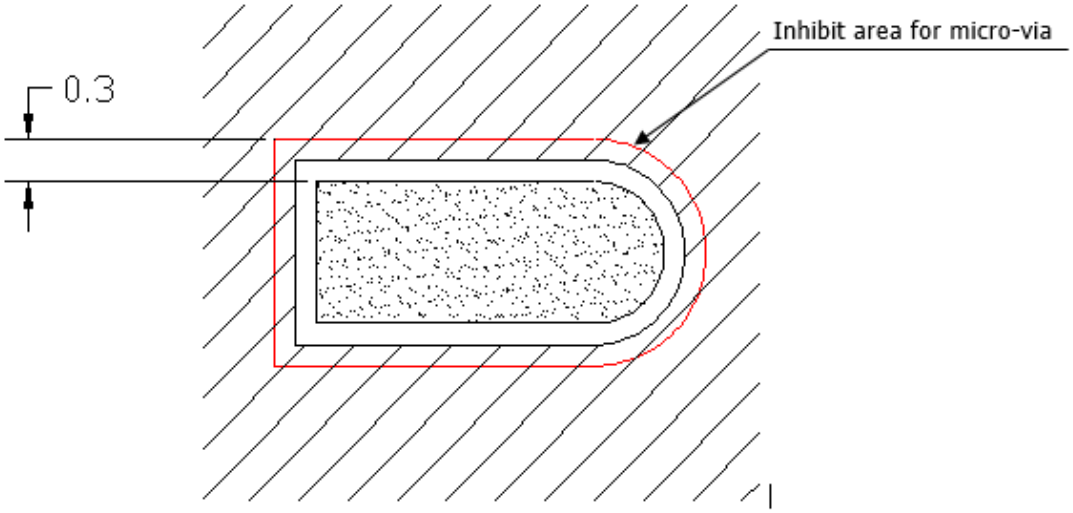
Non solder mask defined (NSMD) type is recommended for the solder pads on the PCB.



10.4. PCB pad dimensions



It is not recommended to place via or micro-via not covered by solder resist in an area of 0.3 mm around the pads unless it carries the same signal of the pad itself (see following figure).



Holes in pad are allowed only for blind holes and not for through holes.
Recommendations for PCB pad surfaces:

Finish	Layer thickness [µm]	Properties
Electro-less Ni / Immersion Au	3 –7 / 0.03 – 0.15	good solder ability protection, high shear force values

The PCB must be able to resist the higher temperatures which are occurring at the lead-free process. This issue should be discussed with the PCB-supplier. Generally, the wettability of tin-lead solder paste on the described surface plating is better compared to lead-free solder paste.
It is not necessary to panel the application PCB, however in that case it is suggested to use milled contours and predrilled board breakouts; scoring or v-cut solutions are not recommended.

10.5. Stencil

Stencil's apertures layout can be the same of the recommended footprint (1:1), we suggest a thickness of stencil foil ≥ 120 µm.

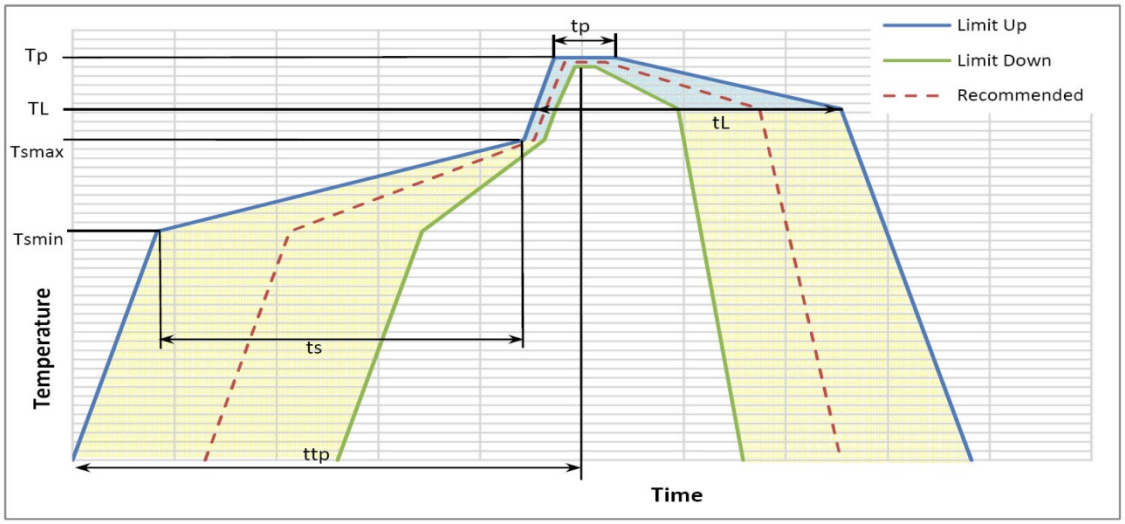
10.6. Solder paste

Item	Lead Free
Solder Paste	Sn/Ag/Cu

We recommend using only “no clean” solder paste in order to avoid the cleaning of the modules after assembly

10.7. Solder Reflow

Recommended solder reflow profile:



WARNING:

The above solder reflow profile represents the typical SAC reflow limits and does not guarantee adequate adherence of the module to the customer application throughout the temperature range. Customer must optimize the reflow profile depending on the overall system taking into account such factors as thermal mass and warpage..

Profile Feature	Pb-Free Assembly Free
Average ramp-up rate (T_L to T_P)	3°C/second max
Preheat **– Temperature Min (Tsmin)** **– Temperature Max (Tsmax)** **– Time (min to max) (ts)**	 150°C 200°C 60-180 seconds
Tsmax to TL **– Ramp-up Rate**	 3°C/second max
Time maintained above: **– Temperature (TL)** **– Time (tL)**	 217°C 60-150 seconds
Peak Temperature (Tp)	245 +0/-5°C
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds
Ramp-down Rate	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

NOTE:

All temperatures refer to topside of the package, measured on the package body surface

WARNING:

THE ML865C1 MODULE WITHSTANDS ONE REFLOW PROCESS ONLY.

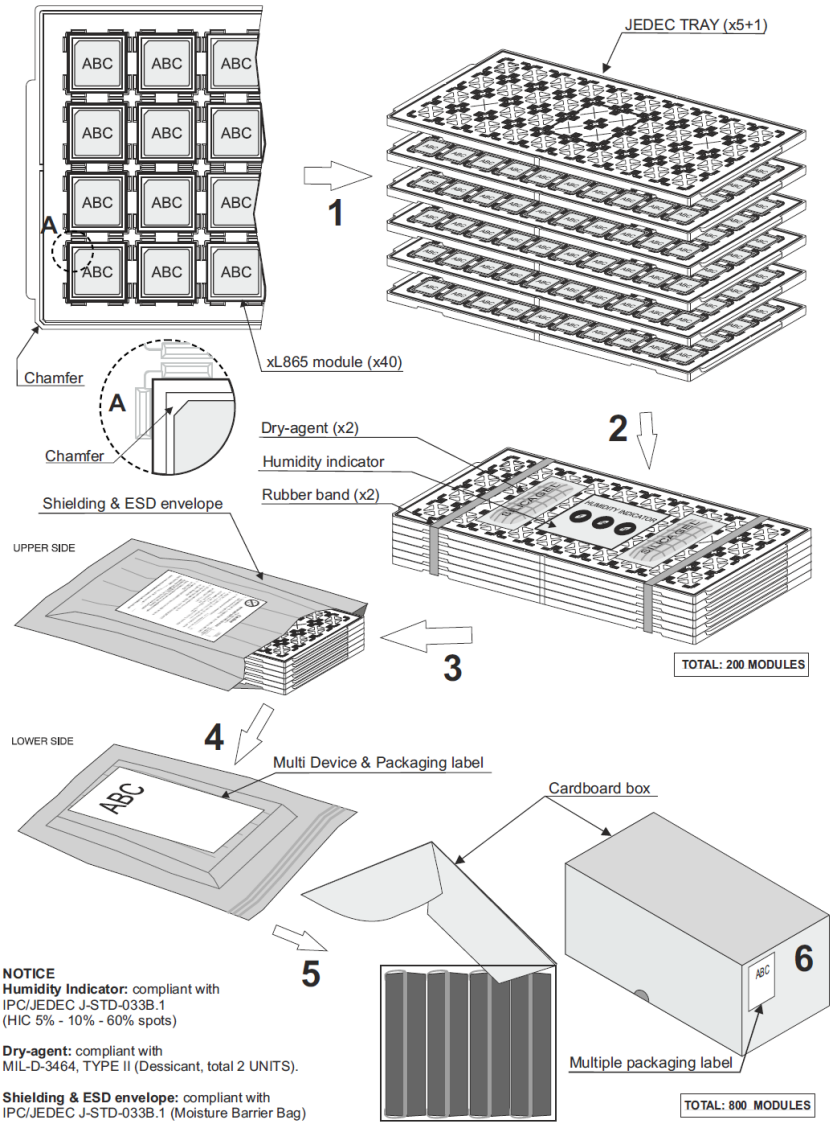
11. PACKAGING

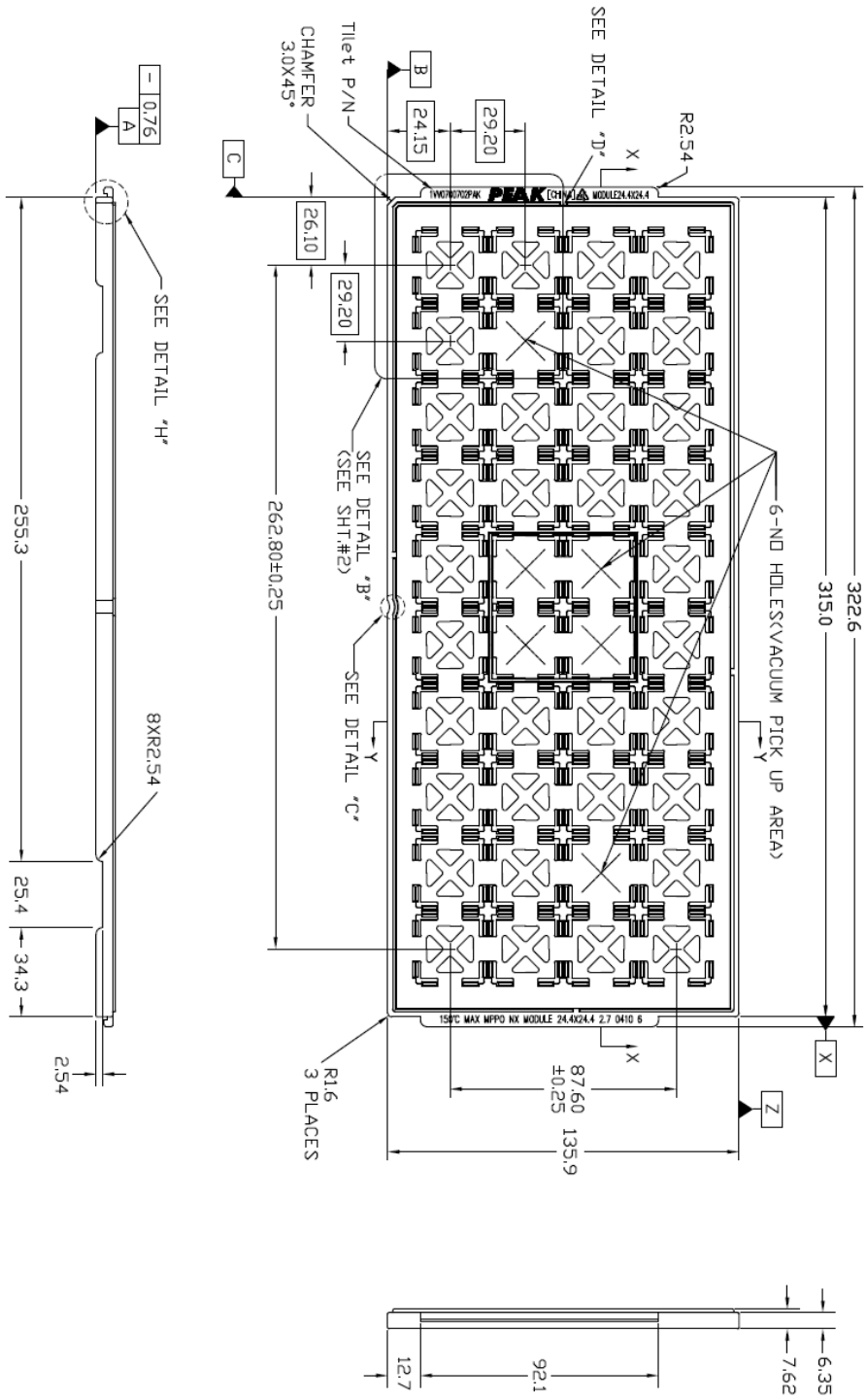
Is possible to order in two packaging system:

- Package on tray
- Package on reel

11.1. Tray

The ML865C1 modules are packaged on trays of 40 pieces each. These trays can be used in SMT processes for pick & place handling.

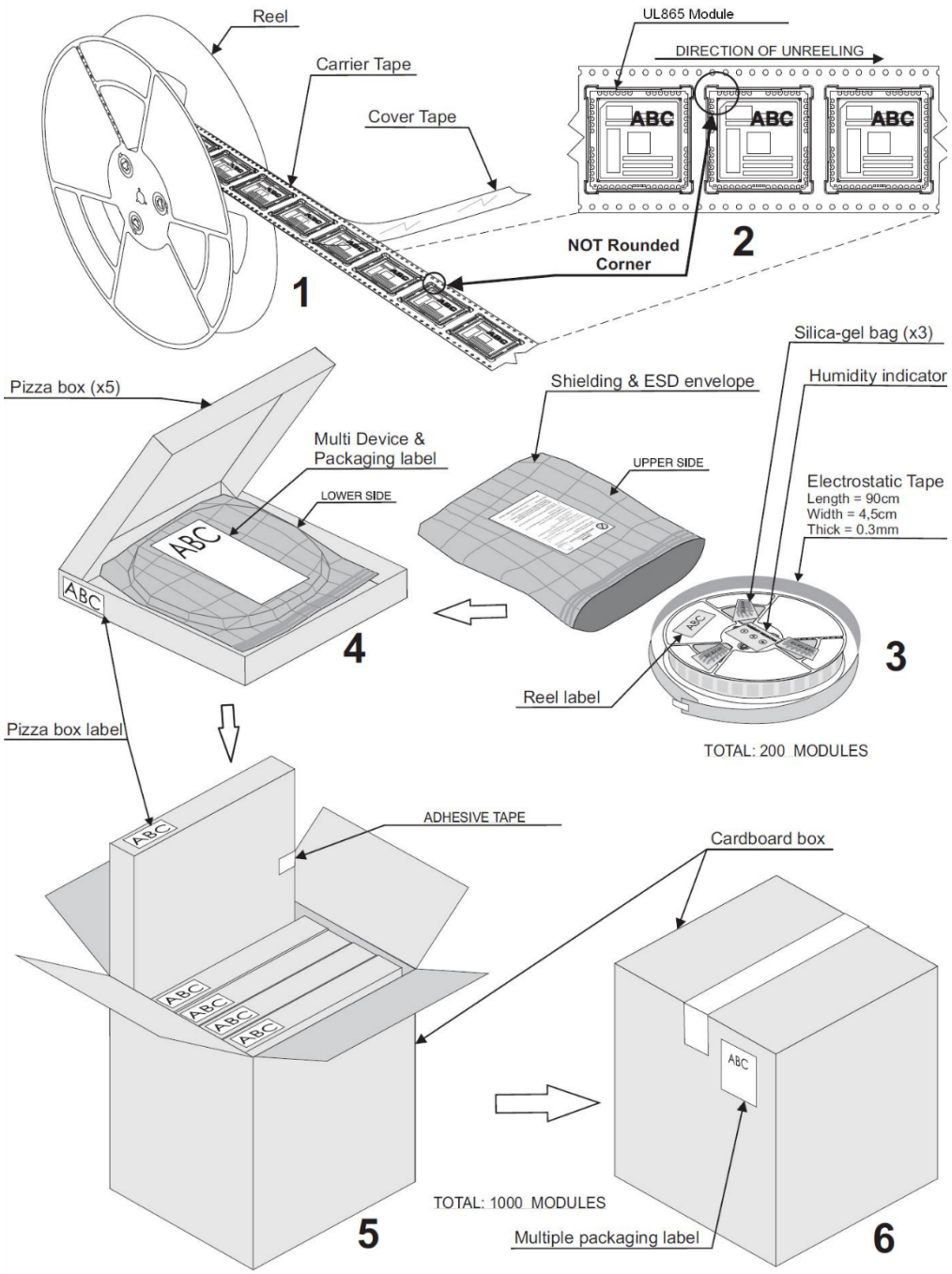



SEE DETAIL "H"
255.3
8XR2.54
25.4
34.3
2.54
0.76
A
B
C
Tilet P/N
CHAMFER 3.0X45°
24.15
29.20
26.10
29.20
SEE DETAIL "D"
R2.54
SEE DETAIL "B" (SEE SHT.#2)
SEE DETAIL "C"
262.80±0.25
6-NO HOLES(VACUUM PICK UP AREA)
322.6
315.0
R1.6 3 PLACES
87.60 ±0.25
135.9
X
Y
Z
12.7
92.1
7.62
6.35

11.2. Reel

The ML865C1 can be packaged on reels of 200 pieces each.

See figure for module positioning into the carrier.



11.3. Moisture sensitivity

The moisture sensitivity level of the Product is “3” according with standard IPC/JEDEC J-STD-020, take care of all the relative requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

a) The shelf life of the Product inside of the dry bag is 12 months from the bag seal date,
   when stored in a non-condensing atmospheric environment of < 40°C and < 90% RH.
b) Environmental condition during the production: <= 30°C / 60% RH according to
   IPC/JEDEC J-STD-033B.
c) The maximum time between the opening of the sealed bag and the reflow process must be
   168 hours if condition b) “IPC/JEDEC J-STD-033B paragraph 5.2” is respected.
d) Baking is required if conditions b) or c) are not respected
e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more.

12. SAFETY RECOMMENDATIONS

12.1. READ CAREFULLY

Be sure the use of this product is allowed in the country and in the environment required. The use of this product may be dangerous and has to be avoided in the following areas:

- Where it can interfere with other electronic devices in environments such as hospitals, airports, aircrafts, etc.
- Where there is risk of explosion such as gasoline stations, oil refineries, etc. It is the responsibility of the user to enforce the country regulation and the specific environment regulation.

Do not disassemble the product; any mark of tampering will compromise the warranty validity. We recommend following the instructions of the hardware user guides for correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to be conformed to the security and fire prevention regulations. The product has to be handled with care, avoiding any contact with the pins because electrostatic discharges may damage the product itself. Same cautions have to be taken for the SIM, checking carefully the instruction for its use. Do not insert or remove the SIM when the product is in power saving mode.

The system integrator is responsible for the functioning of the final product; therefore, care has to be taken to the external components of the module, as well as any project or installation issue, because the risk of disturbing the GSM network or external devices or having impact on the security. Should there be any doubt, please refer to the technical documentation and the regulations in force. Every module has to be equipped with a proper antenna with specific characteristics. The antenna has to be installed with care in order to avoid any interference with other electronic devices and has to guarantee a minimum distance from the body (20 cm). In case this requirement cannot be satisfied, the system integrator has to assess the final product against the SAR regulation.

The European Community provides some Directives for the electronic equipment introduced on the market. All of the relevant information is available on the European Community website:

http://ec.europa.eu/enterprise/sectors/rtte/documents/

The text of the Directive 99/05 regarding telecommunication equipment is available,

while the applicable Directives (Low Voltage and EMC) are available at:

http://ec.europa.eu/enterprise/sectors/electrical/

13. ACRONYMS

TTSC	Telit Technical Support Centre
USB	Universal Serial Bus
HS	High Speed
DTE	Data Terminal Equipment
UMTS	Universal Mobile Telecommunication System
WCDMA	Wideband Code Division Multiple Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
UART	Universal Asynchronous Receiver Transmitter
HSIC	High Speed Inter Chip
SIM	Subscriber Identification Module
SPI	Serial Peripheral Interface
ADC	Analog – Digital Converter
DAC	Digital – Analog Converter
I/O	Input Output
GPIO	General Purpose Input Output
CMOS	Complementary Metal – Oxide Semiconductor
MOSI	Master Output – Slave Input
MISO	Master Input – Slave Output
CLK	Clock
MRDY	Master Ready

SRDY	Slave Ready
CS	Chip Select
RTC	Real Time Clock
PCB	Printed Circuit Board
ESR	Equivalent Series Resistance
VSWR	Voltage Standing Wave Radio
VNA	Vector Network Analyzer

14. DOCUMENT HISTORY

Revision	Date	Changes
0	2018-02-02	First issue
1	2018-05-11	Update Pin allocation and footprint
2	2019-04-08	Updated par 10.7 Solder Reflow Updated ML865C1-EA specs

SUPPORT INQUIRIES

Link to **www.telit.com** and contact our technical support team for any questions related to technical issues.

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