LE910Cx Multi Technology Interface Board TLB - HW User Guide

1VV0301508
Rev. 1 – 2018-02-28

TELIT
TECHNICAL
DOCUMENTATION

SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE

NOTICE

While reasonable efforts have been made to assure the accuracy of this document, Telit assumes no liability resulting from any inaccuracies or omissions in this document, or from use of the information obtained herein. The information in this document has been carefully checked and is believed to be reliable. However, no responsibility is assumed for inaccuracies or omissions. Telit reserves the right to make changes to any products described herein and reserves the right to revise this document and to make changes from time to time in content hereof with no obligation to notify any person of revisions or changes. Telit does not assume any liability arising out of the application or use of any product, software, or circuit described herein; neither does it convey license under its patent rights or the rights of others.

It is possible that this publication may contain references to, or information about Telit products (machines and programs), programming, or services that are not announced in your country. Such references or information must not be construed to mean that Telit intends to announce such Telit products, programming, or services in your country.

COPYRIGHTS

This instruction manual and the Telit products described in this instruction manual may be, include or describe copyrighted Telit material, such as computer programs stored in semiconductor memories or other media. Laws in the Italy and other countries preserve for Telit and its licensors certain exclusive rights for copyrighted material, including the exclusive right to copy, reproduce in any form, distribute and make derivative works of the copyrighted material. Accordingly, any copyrighted material of Telit and its licensors contained herein or in the Telit products described in this instruction manual may not be copied, reproduced, distributed, merged or modified in any manner without the express written permission of Telit. Furthermore, the purchase of Telit products shall not be deemed to grant either directly or by implication, estoppel, or otherwise, any license under the copyrights, patents or patent applications of Telit, as arises by operation of law in the sale of a product.

COMPUTER SOFTWARE COPYRIGHTS

The Telit and 3rd Party supplied Software (SW) products described in this instruction manual may include copyrighted Telit and other 3rd Party supplied computer programs stored in semiconductor memories or other media. Laws in the Italy and other countries preserve for Telit and other 3rd Party supplied SW certain exclusive rights for copyrighted computer programs, including the exclusive right to copy or reproduce in any form the copyrighted computer program. Accordingly, any copyrighted Telit or other 3rd Party supplied SW computer programs contained in the Telit products described in this instruction manual may not be copied (reverse engineered) or reproduced in any manner without the express written permission of Telit or the 3rd Party SW supplier. Furthermore, the purchase of Telit products shall not be deemed to grant either directly or by implication, estoppel, or otherwise, any license under the copyrights, patents or patent applications of Telit or other 3rd Party supplied SW, except for the normal non-exclusive, royalty free license to use that arises by operation of law in the sale of a product.

USAGE AND DISCLOSURE RESTRICTIONS

I. License Agreements

The software described in this document is the property of Telit and its licensors. It is furnished by express license agreement only and may be used only in accordance with the terms of such an agreement.

II. Copyrighted Materials

Software and documentation are copyrighted materials. Making unauthorized copies is prohibited by law. No part of the software or documentation may be reproduced, transmitted, transcribed, stored in a retrieval system, or translated into any language or computer language, in any form or by any means, without prior written permission of Telit

III. High Risk Materials

Components, units, or third-party products used in the product described herein are NOT fault-tolerant and are NOT designed, manufactured, or intended for use as on-line control equipment in the following hazardous environments requiring fail-safe controls: the operation of Nuclear Facilities, Aircraft Navigation or Aircraft Communication Systems, Air Traffic Control, Life Support, or Weapons Systems (High Risk Activities"). Telit and its supplier(s) specifically disclaim any expressed or implied warranty of fitness for such High Risk Activities.

IV. Trademarks

TELIT and the Stylized T Logo are registered in Trademark Office. All other product or service names are the property of their respective owners.

V. Third Party Rights

The software may include Third Party Right software. In this case you agree to comply with all terms and conditions imposed on you in respect of such separate software. In addition to Third Party Terms, the disclaimer of warranty and limitation of liability provisions in this License shall apply to the Third Party Right software.

TELIT HEREBY DISCLAIMS ANY AND ALL WARRANTIES EXPRESS OR IMPLIED FROM ANY THIRD PARTIES REGARDING ANY SEPARATE FILES, ANY THIRD PARTY MATERIALS INCLUDED IN THE SOFTWARE, ANY THIRD PARTY MATERIALS FROM WHICH THE SOFTWARE IS DERIVED (COLLECTIVELY “OTHER CODE”), AND THE USE OF ANY OR ALL THE OTHER CODE IN CONNECTION WITH THE SOFTWARE, INCLUDING (WITHOUT LIMITATION) ANY WARRANTIES OF SATISFACTORY QUALITY OR FITNESS FOR A PARTICULAR PURPOSE.

NO THIRD PARTY LICENSORS OF OTHER CODE SHALL HAVE ANY LIABILITY FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING WITHOUT LIMITATION LOST PROFITS), HOWEVER CAUSED AND WHETHER MADE UNDER CONTRACT, TORT OR OTHER LEGAL THEORY, ARISING IN ANY WAY OUT OF THE USE OR DISTRIBUTION OF THE OTHER CODE OR THE EXERCISE OF ANY RIGHTS GRANTED UNDER EITHER OR BOTH THIS LICENSE AND THE LEGAL TERMS APPLICABLE TO ANY SEPARATE FILES, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

APPLICABILITY TABLE

This documentation applies to the following product families:

Module Name	Description
LE910Cx	LE910C1-NA, LE910C1-AP, LE910C1-NS, LE910C4-NS, LE910C1-EU

Table 1: Applicability Table

The features described by the present document are provided by the products equipped with the software versions equal or higher than the versions shown in the table.

CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. Introduction

1.1. Scope

The scope of this document is to describe the MultiTech Interface Board TLB which is part of the complete EVB Development Kit (Dev-Kit).

1.2. Contact Information, Support

For general contact, technical support services, technical questions and report documentation errors, contact Telit Technical Support at:

- TS-EMEA@telit.com
- TS-AMERICAS@telit.com
- TS-APAC@telit.com
- TS-SRD@telit.com

Alternatively, use:

http://www.telit.com/support

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

http://www.telit.com

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

1.3. Text Conventions

DANGER:
Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

WARNING:
Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

NOTE:
Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

1.4. Related Documents

Document Title	Document Number
LE910C1 HW User Guide	1VV0301298
Generic Evaluation Board Hardware User Guide	1VV0301249

Table 2: Related Documents

1.5. Document Organization

Chapter 1: “Introduction” provides a scope for this document, target audience, contact and support information, and text conventions.

Chapter 2: “General description” provides an overview of the document.

Chapter 3: “The FPGA” describes the FPGA component functions.

Chapter 4: “Component assembly diagram” provides layout placement information.

Chapter 5: “120-Pin Board to board connectors” provides B2B pinout.

Chapter 6: “Schematics”.

Chapter 7: “Revision history”

1.6. Abbreviations and Acronyms

Term	Definition
EVB	Evaluation Board
IFBD	Interface Board
GPIO	General-purpose input/output
SD	Secure digital
UART	Universal asynchronous receiver transmitter
UMTS	Universal mobile telecommunications system
USB	Universal serial bus
USIF	Universal serial interface
FPGA	Field Programmable Array

Table 3: Abbreviations

2. General description

The MultiTech Interface Board TLB (aka MTB) is custom designed to interface the Telit module variant LE910Cx with the Telit Generic Evaluation Board (EVB) thus forming the complete Development Kit of LE910Cx which allows great flexibility for integrating WIFI, BT and GPS technologies with the LE910Cx
The MTB provides the mapping of Telit module signals and functions into the generic EVB signals and functions

The MultiTech Interface Board TLB design includes the following items:

- LE910Cx module.
- 3x M.2 type mini card slots.
- Programmable FPGA.
- RF SMA connectors.
- Board to Board connectors for interfacing to EVB main board
- Module specific circuitry which is not part of the generic circuitry of the EVB

Power supply and control interface for the cellular module is provided from the EVB via the B2B connectors.
To monitor the temperature, a thermistor is placed on the top GND plane, close to the module which should be representative for the module's backside temperature.

A programmable FPGA which is included in the MTB provides options for connecting every functional modem pin to the relevant peripheral M.2 cards hence enabling the most flexible way to demo interoperability between the LE910Cx module and peripheral accessories.
A typical example of this capability is in the case where 3x M.2 cards (WIFI module, GNSS module and BT module) are plugged into the M.2 slots while the FPGA is programmed to perform the correct signals mapping between the LE910Cx and the interfaces of each of the M.2 accessories.

2.1. MultiTech Interface Board TLB view

The following pictures show the MultiTech Interface Board TLB Top and bottom views:

Figure 1 MultiTech Interface Board TLB Top View

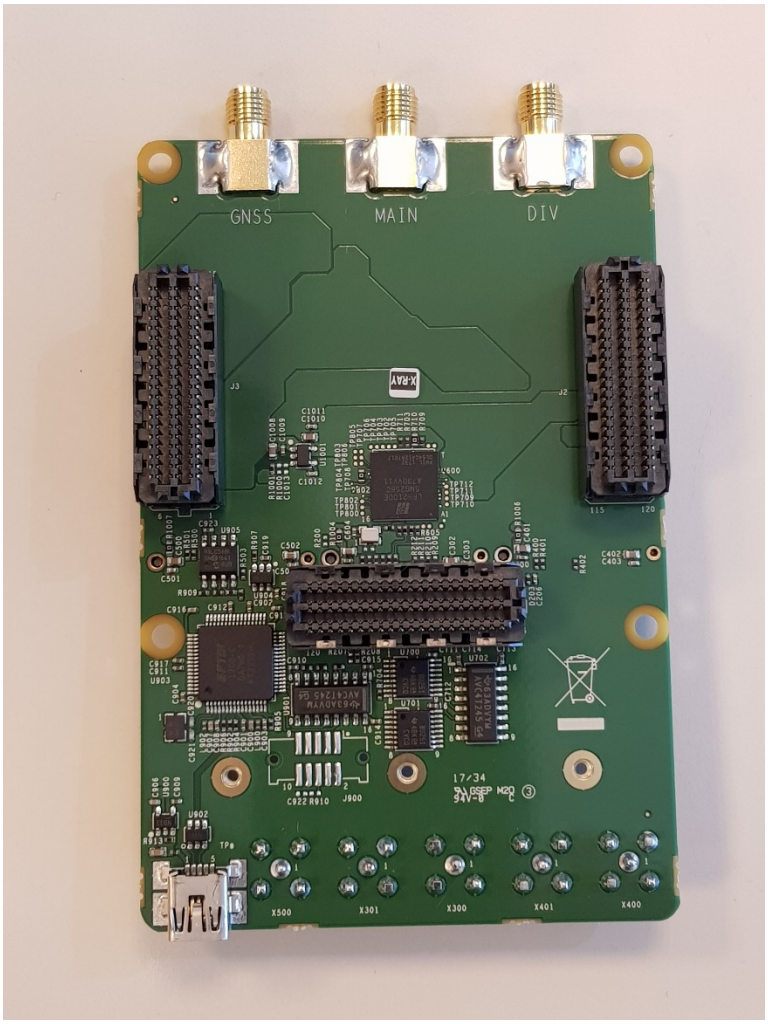


Figure 2 MultiTech Interface Board TLB Bottom View

3. The FPGA

The FPGA used in this board is a Lattice Semiconductor MACHXO3 family device.

More information about this part can be viewed on their web site:
http://www.latticesemi.com/en/Products/FPGAandCPLD/MachXO3

The tools to write, compile, place&route and programming the FPGA can be downloaded from Lattice website.

The purpose of the FPGA in this board is to provide the maximum flexibility connecting different peripherals of the LE910Cx pins.

The board includes a rotary mode selector which is used to select a pre-defined FPGA configuration for mapping the LE910Cx pins to the various peripherals.

For each mode, the signals from the module can be muxed to either or all of the M.2 slots or to the main board connectors on the bottom side (for interfacing to the EVB).

3.1. Programming the FPGA

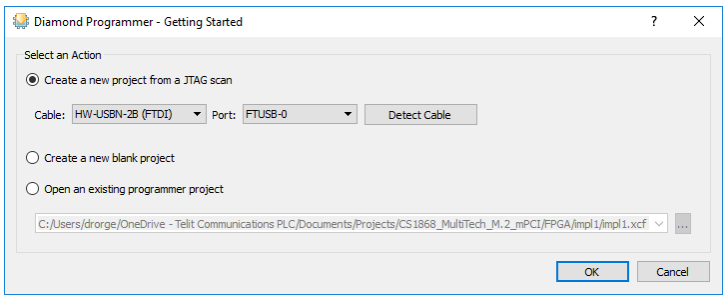
This paragraph details the steps needed to program/flash the FPGA.

Pre-requisites:

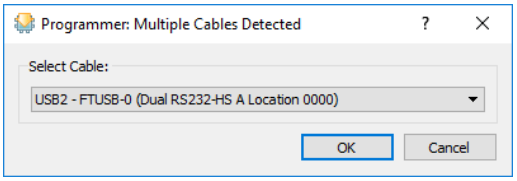
1. The JEDEC file to be programmed. This is the file uploaded/flashed into the FPGA.
2. Programming tool installed. This “Programmer and Deployment Tool” should be downloaded from Lattice Semiconductor website: http://www.latticesemi.com/Products/DesignSoftwareAndIP/ProgrammingAndConfigurationSw/Programmer

Steps for programming the FPGA:

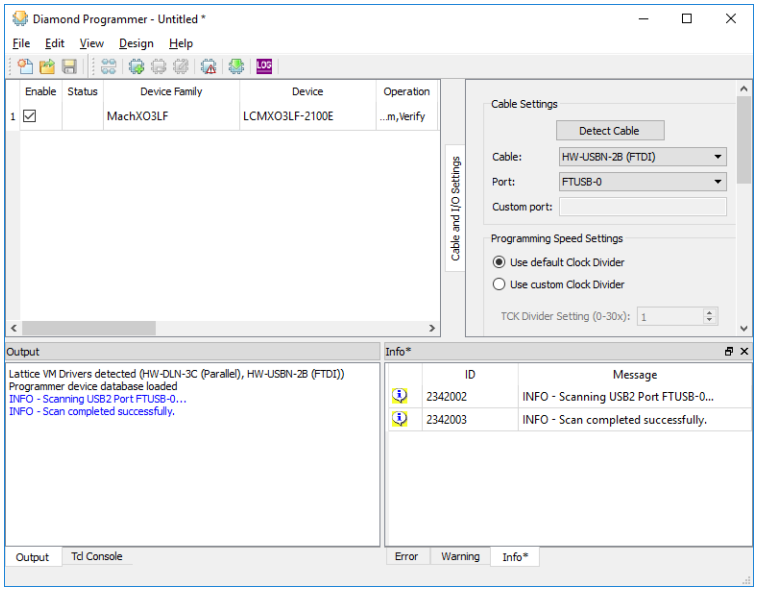
1. Power on the module (pressing the ON button on the EVB main board).
2. Launch the “Diamond Programmer” tool.
3. Select “Detect Cable” on the window that pops up:



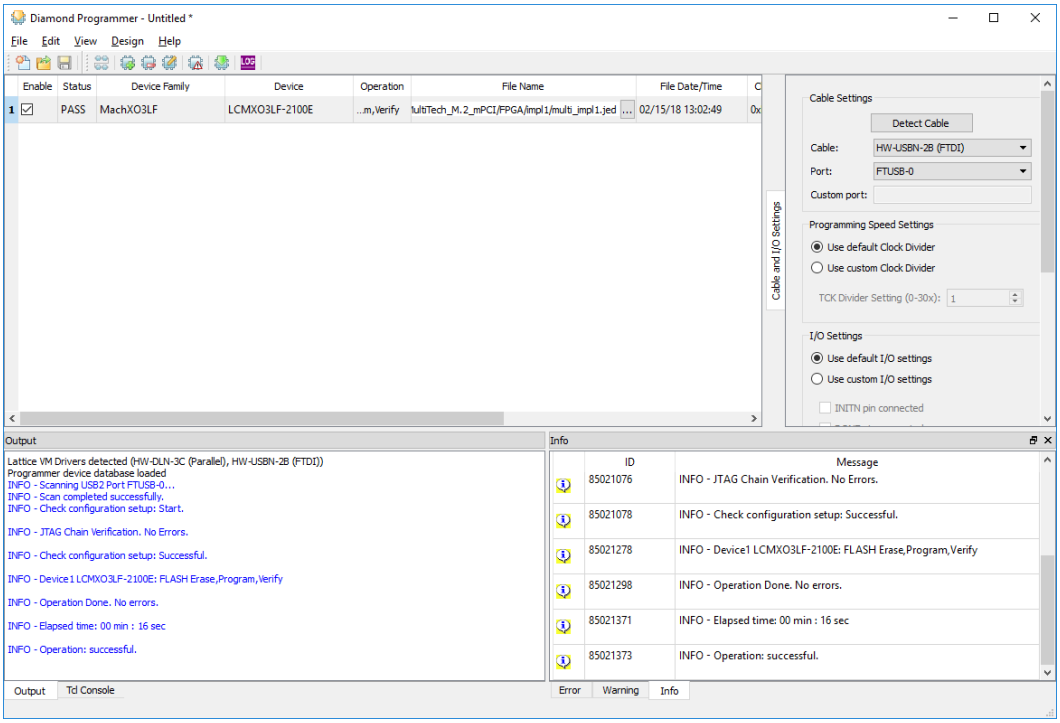
4. Select:



and then OK in the main window.
The main program window will show scanning and searching for the FPGA component.



5. Press the line below the “File name” and select the JEDEC file location. It is now recommended to save the programmer window setup.
6. Program the FPGA by selecting the menu icon  or by “Design” – “Program”.
7. A successful program sequence should be acknowledged as shown below:



3.2. FPGA MODE Selection

As described previously, the board includes a rotary mode selection switch. The switch reference location is SW700. It is a rotary switch with 16 states decoded by the FPGA logic for the different modes needed.

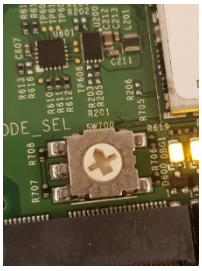


Figure 3 FPGA Mode selection switch

The predefined modes currently supported by the FPGA are detailed below:

Mode switch selection	Functional mode description
0	Default
1	WIFI Slot 1 (SDIO) / BT Slot 2 / GPS slot 3
2	Spare
3	WIFI Slot 2 (SPI) / BT Slot 1 / GPS slot 3
4	Spare
5	Spare
6	Spare
7	Spare
8	Spare
9	Spare
10 (A)	LE910C1: Slot 1 HCI Bluetooth connection to EVB MAIN_UART (for testing only)
11 (B)	Spare
12 (C)	Spare
13 (D)	LE910 V2: SPI, I2C_GPIOs (10-SCL, 8-SDA) AT#I2CWR=8,10,30,4,19
14 (E)	LE910 V2: SPI to UART_AUX
15 (F)	LE910C1: WIFI SDIO SLOT1 (Normal EVB mode)

Figure 4 FPGA Mode Selection

NOTE:

Additional modes for supporting new bundling options might be released later on

Please contact Telit representative for more information.

4. 120-Pin Board to Board Connectors

1	GND	2	GND	3		4		5	GND	6	
7	USB_SS_RX_P	8	GND	9	I2C_SDA	10	TGPIO_06	11		12	
13	USB_SS_RX_M	14	GND	15	TGPIO_05	16	I2C_SCL	17		18	GND
19	GND	20	GND	21	VREG_MSME	22	VREG_MSME	23	GND	24	
25	USB_SS_TX_P	26	GND	27		28		29		30	
31	USB_SS_TX_M	32	GND	33		34	SPI_MOSI	35		36	GND
37	GND	38		39		40	TGPIO_04	41	GND	42	
43	SPI_CS	44	TGPIO_02	45	TGPIO_03	46	SPI_MISO	47		48	
49	VAUX/PWRMON	50	VAUX/PWRMON	51		52	SPI_CLK	53		54	
55	TGPIO_08	56	TGPIO_07	57	TGPIO_01	58	TGPIO_09	59		60	
61		62	TGPIO_10	63		64	TGPIO_20	65		66	
67	VMMC	68	VMMC	69	MMC_CD	70	MMC_DAT3	71		72	
73	MMC_DAT0	74	MMC_DAT2	75	MMC_CLK	76	MMC_DAT1	77		78	
79	GND	80	GND	81	C107/DSR	82	MMC_CMD	83		84	
85		86		87		88		89	TX_AUX	90	
91		92		93		94		95	RX_AUX	96	
97		98		99		100	WCI_TX	101	WCI_RX	102	
103	C125/RING	104	RFCLK2_QCA	105	WLAN_SLEEP_CLK	106	C105/RTS	107		108	
109	C104/RXD	110	C109/DCD	111	C103/TXD	112	C106/CTS	113	C108/DTR	114	
115		116		117		118		119		120	

Table 4: Board to Board Connector J1

1	GPS_LNA_BIAS	2	GND	3	GPS_LNA_EN	4		5	GND	6	
7	GND	8	GND	9	GND	10	GND	11	GND	12	
13		14		15	GND	16		17		18	
19	GND	20	GND	21	GND	22	GND	23	GND	24	GND
25		26		27	GND	28		29		30	GND
31		32		33		34		35		36	
37	GND	38	GND	39		40		41	GND	42	GND
43		44	GND	45	GND	46	GND	47	GND	48	GND
49		50	GND	51	GND	52	ADC_IN3	53	ADC_IN2	54	ADC_IN1
55		56		57		58		59		60	
61	DVI_RX	62	DVI_TX	63	DVI_CLK	64	DVI_WAO	65	REF_CLK	66	GND
67	GND	68	GND	69	GND	70	GND	71	GND	72	
73	GND	74	GND	75	GND	76	GND	77	SIMVCC1	78	SIMVCC1
79	HSIC_STB	80	HSIC_DATA	81	SIMCLK1	82	SIMIN1	83	SIMIO1	84	SIMRST1
85		86	VRTC	87		88		89	SIMVCC2	90	SIMVCC2
91	USB_VBUS	92	USB_ID	93	SIMIN2	94	SIMIO2	95	SIMRST2	96	SIMCLK2
97	GND	98	GND	99		100		101		102	
103	USB_D+	104	GND	105		106		107		108	
109	USB_D-	110	GND	111		112		113		114	
115	GND	116	GND	117		118		119		120	

Table 5: Board to Board Connector J2

1	VBATT	2	VBATT	3	VBATT	4	VBATT_PA	5	VBATT_PA	6	VBATT_PA
7	VBATT	8	VBATT	9	VBATT	10	VBATT_PA	11	VBATT_PA	12	VBATT_PA
13	VBATT	14	VBATT	15	VBATT	16	VBATT_PA	17	VBATT_PA	18	VBATT_PA
19		20		21		22	VBATT_PA	23	VBATT_PA	24	VBATT_PA
25		26		27		28		29		30	
31		32		33		34		35		36	
37		38		39		40		41		42	
43		44		45		46		47		48	
49		50		51		52		53		54	
55		56		57		58		59		60	
61		62		63		64		65		66	D8_THERM_ASTAR
67		68		69		70		71		72	
73		74		75		76		77		78	
79	GND	80	GND	81	GND	82	GND	83	GND	84	GND
85	GND	86	GND	87	GND	88	GND	89	GND	90	GND
91	RESET	92	ON_OFF	93	STAT_LED	94		95	SW_RDY	96	SHDN
97	GND	98	GND	99	GND	100	GND	101		102	
103	GPS_SYNC	104	GPS_RFPAON	105	GPS_CLK	106	GND	107		108	
109	GND	110	GND	111	GND	112	GND	113	JTAG_TDI	114	JTAG_PS_HOLD
115	JTAG_TMS	116	JTAG_TDO	117	JTAG_TRST	118	JTAG_TCK	119	JTAG_RTCK	120	JTAG_RESOUT

Table 6: Board to Board Connector J3

5. Component Assembly Diagram

Searchable Layout:

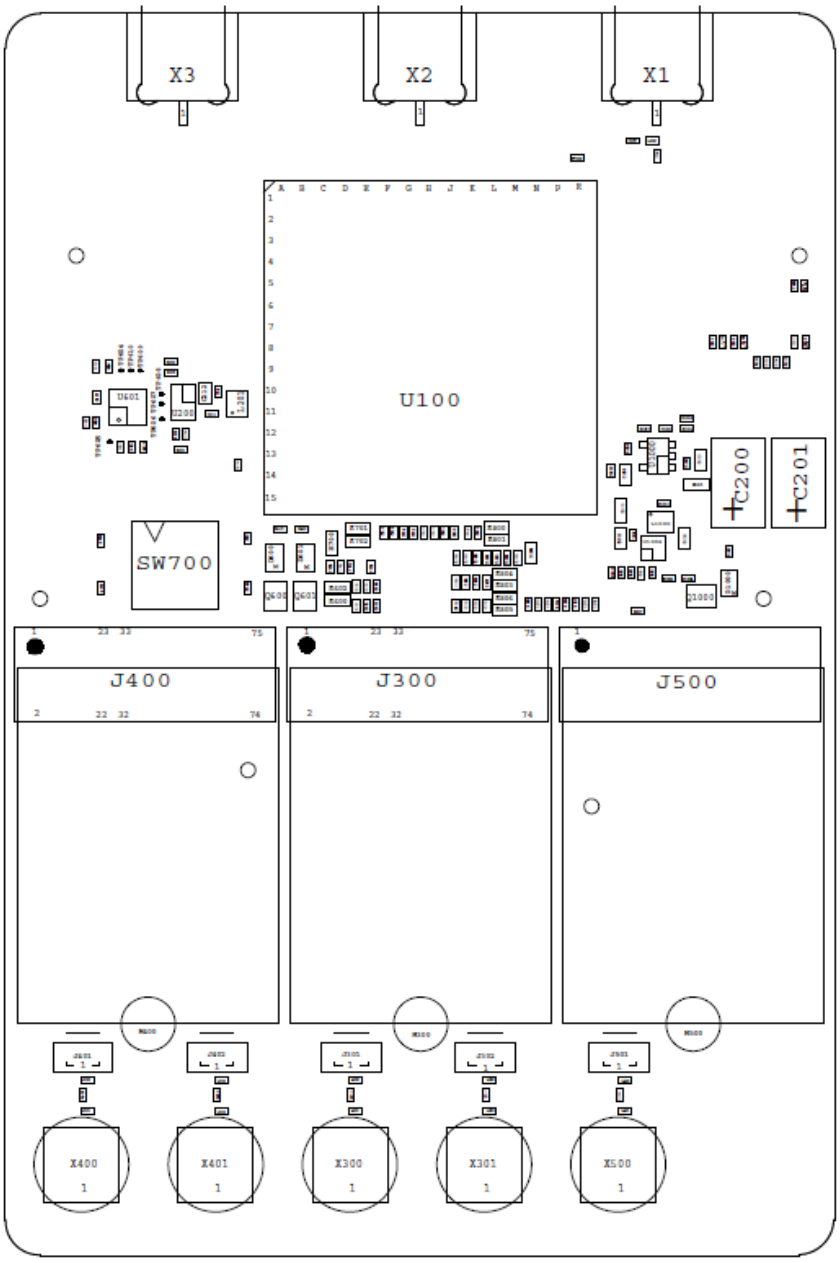


Figure 5 Component Diagram TOP View

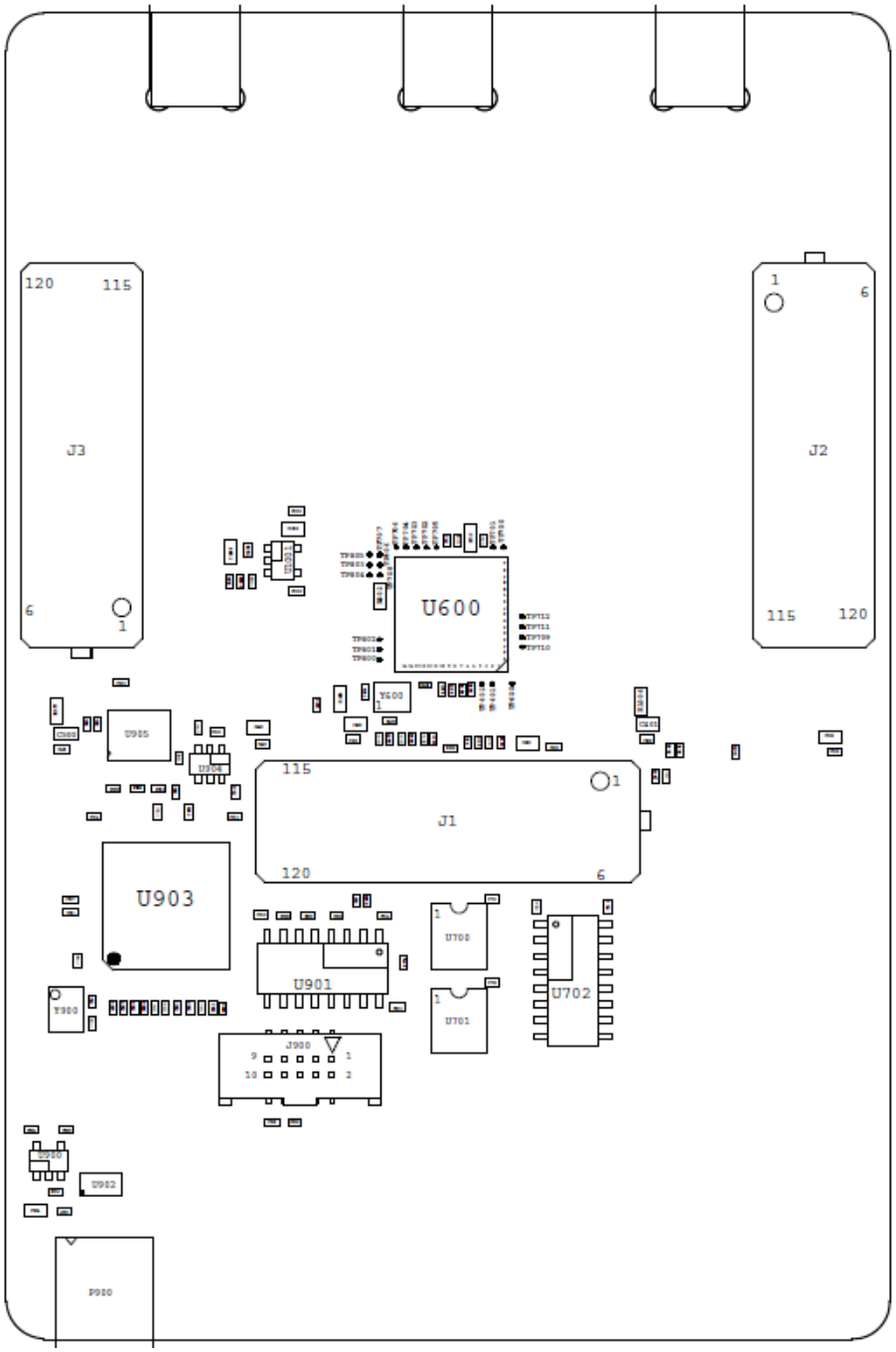


Figure 6 Component Diagram BOTTOM View

6. Schematics

Searchable PDF:

7. Revision History

REV	DATE	CHANGES
1	2018-02-27	Initial Version

Table 7: Revision History

SUPPORT INQUIRIES

Link to **www.telit.com** and contact our technical support team for any questions related to technical issues.

www.telit.com

Telit Communications S.p.A.
Via Stazione di Prosecco, 5/B
I-34010 Sgonico (Trieste), Italy

Telit IoT Platforms LLC
5300 Broken Sound Blvd, Suite 150
Boca Raton, FL 33487, USA

Telit Wireless Solutions Inc.
3131 RDU Center Drive, Suite 135
Morrisville, NC 27560, USA

Telit Wireless Solutions Co., Ltd.
8th Fl., Shinyoung Securities Bld.
6, Gukjegeumyung-ro8-gil, Yeongdeungpo-gu
Seoul, 150-884, Korea

Telit Wireless Solutions Ltd.
10 Habarzel St.
Tel Aviv 69710, Israel

Telit Wireless Solutions
Technologia e Servicos Ltda
Avenida Paulista, 1776, Room 10.C
01310-921 São Paulo, Brazil