NL865B1
HW Design Guide

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APPLICABILITY TABLE

PRODUCTS

- NL865B1-E1

Contents

1. INTRODUCTION

1.1. Scope

This document introduces the Telit NL865B1 module and presents possible and recommended hardware solutions for developing a product based on this module. All the features and solutions detailed in this document are applicable to all NL865B1 variants, where NL865B1 refers to the variants listed in the applicability table.

Obviously, this document cannot embrace every hardware solution or every product that can be designed. Where the suggested hardware configurations need not be considered mandatory, the information given should be used as a guide and a starting point for properly developing your product with the Telit module.

1.2. Audience

This document is intended for Telit customers, especially system integrators, about to implement their applications using the Telit module.

1.3. Contact Information, Support

For general contact, technical support services, technical questions and report documentation errors contact Telit Technical Support at:

- TS-EMEA@telit.com
- TS-AMERICAS@telit.com
- TS-APAC@telit.com
- TS-SRD@telit.com

Alternatively, use:

http://www.telit.com/support

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

http://www.telit.com

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

1.4. Text Conventions

Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

1.5. Related Documents

- SIM INTEGRATION DESIGN GUIDE 80000NT10001A
- NE866B1 AT Commands Reference Guide 80534ST10817A
- Telit EVB User Guide 1VV0301249
- NL865 IFBD User Guide 1VV0301451

2. GENERAL PRODUCT DESCRIPTION

2.1. Overview

The NL865B1 is the Category NB1 - aka Narrowband IoT (NB-IoT) - evolution in the widely deployed Telit xL865 product family. Specified in the Release 13 of the 3GPP standard, Cat NB1 devices are specifically tailored for IoT applications, offering optimized power consumption and enhanced coverage. In addition, with its square 24.4 x 24.4 mm VQFN footprint, the NE865B1 is designed for size sensitive applications.

This next generation of products supports the new features specified by 3GPP to boost IoT applications, such as the Power Saving Mode (PSM) and the extended Discontinuous Reception (eDRX), which allow the devices to wake up periodically to deliver only very small amounts of data to the network and then go back to sleep for most of the time, thus allowing longer battery operation. Enhanced coverage, with up to +20dB in maximum coupling loss (MCL) compared to the other cellular technologies, is also one of the key benefits of this new LTE flavour. LTE Cat NB1 devices are therefore optimized in cost, size and power consumption compared to higher UE categories. These advantages make the NL865B1 the perfect platform to enable a quick implementation of LTE technology in IoT/M2M where low cost and low power are more relevant than high speed.

The NL865B1 helps increase the addressable market for LTE technology to include a broad range of new applications and use cases best served with lower maximum data rate, ultra-low power, reduced complexity and cost. Some examples are smart metering, smart parking, smart agriculture, waste collection, industrial sensors, healthcare monitors, home automation, and many more low data rate IoT devices. The NL865B1 is offered in a dual-band configuration for deployment in the European and Chinese NB-IoT networks, either in in-band, guard-band or standalone mode; additional regional variants will follow. It is highly recommended for new designs, but also in particular as a migration path for existing GPRS devices, both new and updated designs benefit from a significant extension in life-cycle with LTE Cat NB1.

The NL865B1 supports embedded SIM chip as a mounting option, making it the ideal solution for durable and rugged designs, and reducing BOM cost and size on the customer’s application.

2.2. Product Variants and Frequency Bands

NL865B1 bands combinations are listed below:

Product	2G Band (MHz)	3G Band (MHz)	4G Band (MHz)	Region
NL865B1-E1			B20 (800) B8 (900)	Europe

Refer to Chapter 13 for details information about frequencies and bands.

2.3. Target market

The NL865B1 can be used for IoT applications, where low power consumption and enhanced coverage are required rather than high speed data, for example:

- Smart metering
- Smart parking
- Smart agriculture
- Waste collection
- Industrial sensors
- Healthcare monitors
- Home automation

2.4. Main features

Function	Features
Modem	• NB-IoT cellular modem for low BW data communication • Real Time Clock • Internal IP stack
Interfaces	• Main UART for AT commands • Auxilary UART TX for logging • I2C • SPI • GPIOs • ADC • Antenna ports

2.5. TX Output Power

Band	Power class
LTE All Bands	Class 3 (23dBm), Class 5 (20dBm)

2.6. RX Sensitivity

Product	Band	Sensitivity (dBm)
NL865-B1-E1	B8, B20	-113

2.7. Mechanical specifications

2.7.1. Dimensions

The overall dimensions of NL865 family are:

- Length: 24.4 mm
- Width: 24.4 mm
- Thickness: 2.45 mm

	NOTE: A typical label height of 0.1 mm needs to be considered additionally to the module heights.

2.7.2. Weight

The nominal weight of the module is 2.5 grams.

2.8. Temperature range

Case	Range	Note
Operating Temperature Range	–20°C ÷ +55°C	The module is fully functional(*) in all the temperature range, and it fully meets the 3GPP specifications.
	–40°C ÷ +85°C	The module is fully functional (*) in all the temperature range.
Storage and non-operating Temperature Range	–40°C ÷ +85°C	

(*) Functional: the module is able to make and receive data calls and SMS.

3. PINS ALLOCATION

3.1. Pin-out

Pin	Signal	I/O	Function	Type	Comment
Asynchronous Serial Port - Prog. / Data					
7	TXD	I	Serial data input from DTE	CMOS 1.8V	
8	RXD	O	Serial data output to DTE	CMOS 1.8V	

Asynchronous Auxiliary Serial Port 2 / I2C					
45	TX_AUX	O	Auxiliary UART (TX Data to DTE)	CMOS 1.8V	Primary Logging Port
44	I2C_SCL	I/O	I2C Clock	CMOS 1.8V	
6	I2C_SDA	I/O	I2C Data	CMOS 1.8V	

SIM card interface					
9	SIMVCC	-	External SIM signal – Power supply for the SIM	1.8V Only	See next chapters
10	SIMRST	O	External SIM signal – Reset	CMOS 1.8	
11	SIMCLK	O	External SIM signal – Clock	CMOS 1.8	
12	SIMIO	I/O	External SIM– Data I/O	CMOS 1.8	
29	SIMIN/GPIO_05(*)	I	SIM Presence input	CMOS 1.8	See next chapters
ADC					
13	ADC_IN1	AI	Analog/Digital converter input	A/D	Accepted values 0 to 1.8V DC
RF Section					
34	ANT	I/O	LTE Main Antenna (50 ohm)	RF	
General Purpose I/O's					
42	GPIO01	I/O	General purpose I/O 1	CMOS 1.8	
41	GPIO_02	I/O	General purpose I/O 2	CMOS 1.8	
40	GPIO_03	I/O	General purpose I/O 3	CMOS 1.8	
39	GPIO_04	I/O	General purpose I/O 4	CMOS 1.8	

29	(*)GPIO_05/SIM_IN	I/O	General purpose I/O 5 SIM Presence input	CMOS 1.8	Default is SIMIN
28	GPIO_06	I/O	General purpose I/O 6	CMOS 1.8	
27	GPIO_07	I/O	General purpose I/O 7	CMOS 1.8	
26	GPIO08	I/O	General purpose I/O 08	CMOS 1.8	
Miscellaneous Functions					
47	RESET*	I	Reset Input	VBATT	Pull up to VBATT (10Kohm)
48	SLP_IND	O	Sleep Indication	CMOS 1.8	Do not Drive this pad
43	VAUX/POWERMON	O	1.8V stabilized output	Power	
19	LP_WAKE	I	Low Power Wake Up	Analog	
Power Supply					
38	VBATT	-	Main power supply (Baseband)	Power	
37	VBATT_PA	-	Main power supply (RF)	Power	
23	GND	-	Ground	Power	
32	GND	-	Ground	Power	
33	GND	-	Ground	Power	

35	GND	-	Ground	Power	
36	GND	-	Ground	Power	
46	GND	-	Ground	Power	
Reserved pins					
1	RESERVED	-	RESERVED		
2	RESERVED	-	RESERVED		
3	RESERVED	-	RESERVED		
4	RESERVED	-	RESERVED		
5	RESERVED	-	RESERVED		
14	RESERVED	-	RESERVED		
15	RESERVED	-	RESERVED		
16	RESERVED	-	RESERVED		
17	RESERVED	-	RESERVED		
18	RESERVED	-	RESERVED		
20	RESERVED	-	RESERVED		
21	RESERVED	-	RESERVED		
22	RESERVED	-	RESERVED		
24	RESERVED	-	RESERVED		
25	RESERVED	-	RESERVED		
30	RESERVED	-	RESERVED		
31	RESERVED	-	RESERVED		

WARNING:

Reserved pins must not be connected

	NOTE: The functions marked with (*) are not avalable on early samples and will be supported on future release. For more information, please refer to the related SW documentation

3.2. LGA Pads Layout

		48	47	46	45	44	43	42	41	40	39	38	37		
		SLP_IND	RESET*	GND	TX AUX	I2C_SCL	VAUX/PWR MON	GPIO_01	GPIO_02	GPIO_03	GPIO_04	VBATT	VBATT_PA		
1	RFU													GND	36
2	RFU													GND	35
3	RFU													ANT	34
4	RFU													GND	33
5	RFU													GND	32
6	I2C_SDA													RFU	31
7	TXD													RFU	30
8	RXD													(*)GPIO_05/ SIMIN	29
9	SIMVCC													GPIO_06	28
10	SIMRST													GPIO_07	27
11	SIMCLK													GPIO_08	26
12	SIMIO													RFU	25
		ADC_IN1	RFU	RFU	RFU	RFU	RFU	LP_WAKE	RFU	RFU	RFU	GND	RFU		
		13	14	15	16	17	18	19	20	21	22	23	24		

TOP VIEW

WARNING

Reserved pins must not be connected.

4. POWER SUPPLY

The power supply circuitry and board layout are a very important part in the full product design and they strongly reflect on the product overall performances, hence read carefully the requirements and the guidelines that will follow for a proper design.

4.1. Power Supply Requirements

The external power supply must be connected to VBATT and VBATT_PA pins and must fulfil the following requirements:

Power Supply	Value	Power Supply
Nominal Supply Voltage	3.8V	Nominal Supply Voltage
Normal Operating Voltage Range	3.40 V÷ 4.20 V	Normal Operating Voltage Range
Extended Operating Voltage Range	3.10 V÷ 4.20 V	Extended Operating Voltage Range

NOTE:
The Operating Voltage Range MUST never be exceeded; care must be taken when designing the application's power supply section to avoid having an excessive voltage drop.
If the voltage drop is exceeding the limits it could cause a Power Off of the module.
Overshoot voltage (regarding MAX Extended Operating Voltage) and drop in voltage (regarding MIN Extended Operating Voltage) MUST never be exceeded;
The "Extended Operating Voltage Range" can be used only with completely assumption and application of the HW User guide suggestions.

4.2. Power Consumption

Mode	Typical	Mode Description
AT+CFUN=1	5.3 mA	Normal mode - Full functionality with power saving disabled
AT+CFUN=0	< 4.6 µA	TX/RX disabled, module is not registered to the network
DRX paging modes(Full functionality with power saving enabled)	377.8 µA	TX=22dBm, T3324 = 30sec, T3412 = 2621.44 s (~44min)
	95.2 µA	TX=22dBm, T3324 = 30sec, T3412 = 10485.76s (~175 min)
	246.3 µA	C-eDRX = 10.24 sec
AT#PSM = 1	< 4.6 µA	Power Saving Enabled
NB-IoT Data Call	90mA	BW=3.75KHz, Single tone data call (TX=0dBm)
	90mA	BW=15KHz, Single tone data call (TX=0dBm)
	155 mA	BW=3.75KHz, Single tone data call (TX=20dBm)
	155 mA	BW=15KHz, Single tone data call (TX=20dBm)
	195 mA	BW=3.75KHz, Single tone data call (TX=23dBm)
	195 mA	BW=3.75KHz, Single tone data call (TX=23dBm)

Current consumptions specification refers to typical samples and are only indicative at this stage. Consumptions obtained with VBATT = VBATT_PA = 3.8V

4.3. General Design Rules

The principal guidelines for the Power Supply Design embrace three different design steps:

- The electrical design
- The thermal design
- The PCB layout.

4.3.1. Electrical Design Guidelines

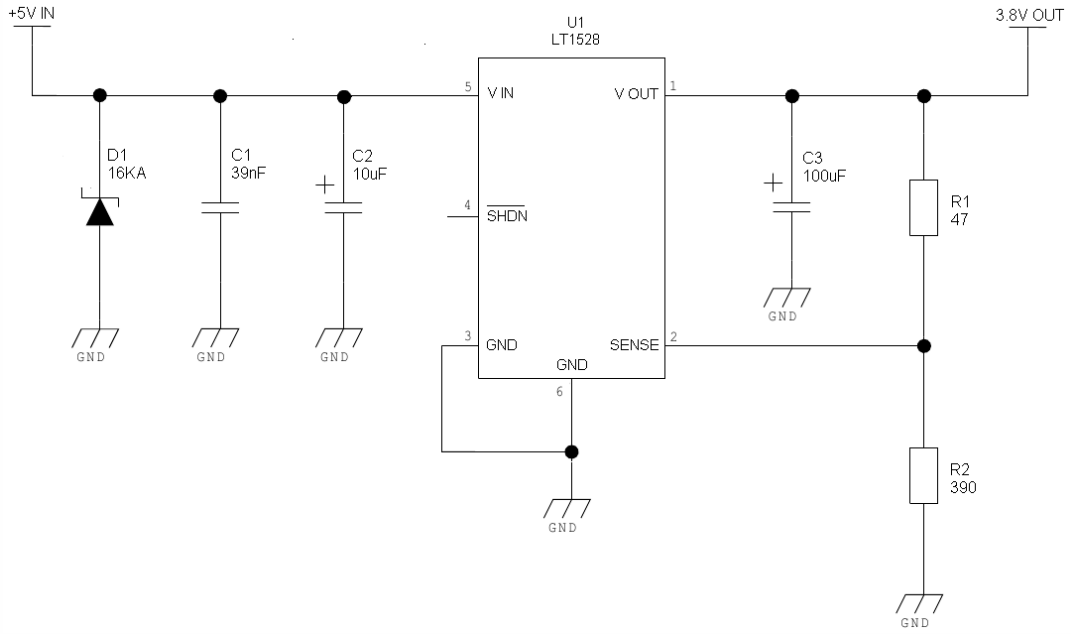
The electrical design of the power supply depends strongly from the power source where this power is drained. We will distinguish them into three categories:

- +5V input (typically PC internal regulator output)
- +12V input (typically automotive)
- Battery

4.3.1.1. +5V Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, hence there's not a big difference between the input source and the desired output and a linear regulator can be used. A switching power supply will not be suited because of the low drop out requirements.
- When using a linear regulator, a proper heat sink shall be provided in order to dissipate the power generated.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks close to the Module, a 100µF capacitor is usually suited.
- Make sure the low ESR capacitor on the power supply output rated at least 10V.

An example of linear regulator with 5V input is:

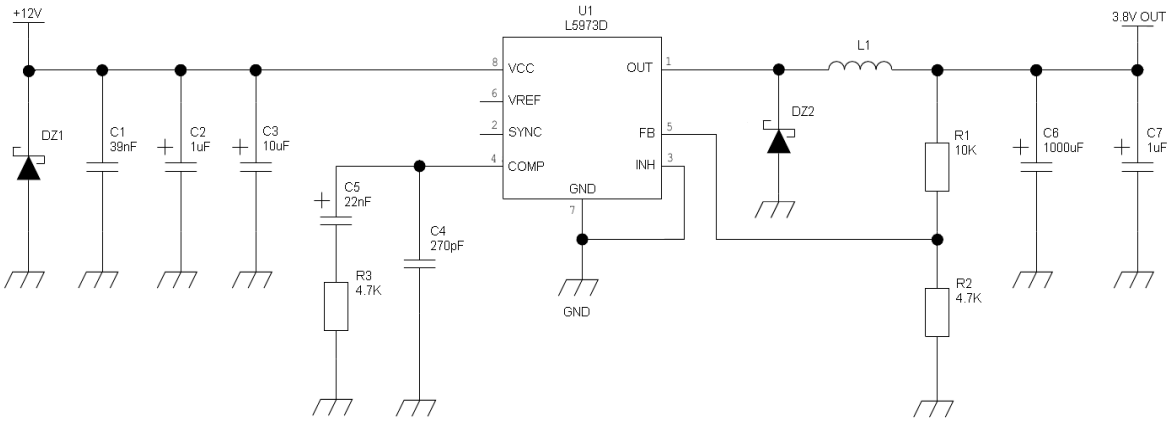


4.3.1.2. +12V Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, hence due to the big difference between the input source and the desired output, a linear regulator is not suited and shall not be used. A switching power supply will be preferable because of its better efficiency.
- When using a switching regulator, a 500kHz or more switching frequency regulator is preferable because of its smaller inductor size and its faster transient response. This allows the regulator to respond quickly to the current peaks absorption.
- In any case the frequency and Switching design selection is related to the application to be developed due to the fact the switching frequency could also generate EMC interferences.
- For car PB battery the input voltage can rise up to 15,8V and this should be kept in mind when choosing components: all components in the power supply must withstand this voltage.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100µF capacitor is usually suited.
- Make sure the low ESR capacitor on the power supply output is rated at least 10V.

  For Car applications, a spike protection diode should be inserted close to the power input, in order to clean the supply from spikes.

An example of switching regulator with 12V input is in the below schematic:



4.3.1.3. Battery Source Power Supply Design Guidelines

The desired nominal output for the power supply is 3.8V and the maximum voltage allowed is 4.2V, hence a single 3.7V Li-Ion cell battery type is suited for supplying the power to the Telit NL865B1 module.

- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100µF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor (usually a tantalum one) is rated at least 10V.
- A protection diode should be inserted close to the power input, in order to save the NL865B1 from power polarity inversion. Otherwise the battery connector should be done in a way to avoid polarity inversions when connecting the battery.
- The selected battery should be capable of supporting the max peak currents of ~0.5A.

NOTE:

DON'T USE any Ni-Cd, Ni-MH, and Pb battery types directly connected with NL865B1. Their use can lead to overvoltage on the NL865B1 and damage it. USE ONLY Li-Ion battery types.

4.3.2. Thermal Design Guidelines

The thermal design for the power supply heat sink should be done with the following specifications:

- Average current consumption during NB-IoT transmission @ Max PWR level at min battery level : 195 mA
- Average current during idle: 5.3 mA

Considering the very low current during idle, especially if Power Saving function is enabled, it is possible to consider from the thermal point of view that the device absorbs current significantly only during transmission .

If we assume that the device stays into transmission for short periods of time (let's say few minutes) and then remains for a quite long time in idle (let's say one hour), then the power supply has always the time to cool down between the paging cycles and the heat sink could be smaller than the calculated one for 300mA maximum RMS current, or even could be the simple chip package (no heat sink).

Moreover in the average network conditions the device is requested to transmit at a lower power level than the maximum and hence the current consumption will be less than the 195mA (@23dBm), being usually around 150 mA (@20dBm).

For these reasons the thermal design is rarely a concern and the simple ground plane where the power supply chip is placed can be enough to ensure a good thermal condition and avoid overheating.

The generated heat will be mostly conducted to the ground plane under the NL865B1; you must ensure that your application can dissipate it.

NOTE:

The average consumption during transmissions depends on the power level at which the device is requested to transmit by the network. The average current consumption hence varies significantly.

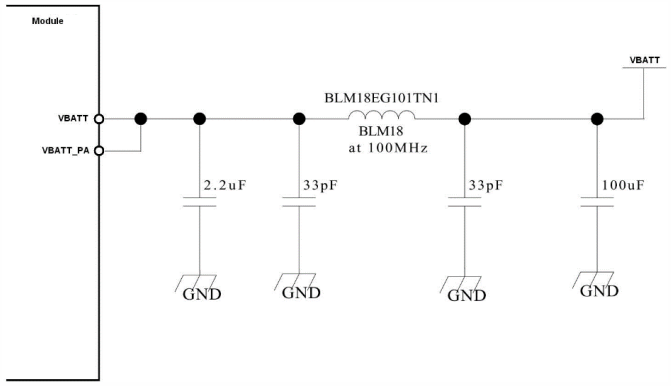
4.3.3. Power Supply PCB layout Guidelines

As seen on the electrical design guidelines the power supply shall have a low ESR capacitor on the output to cut the current peaks on the input to protect the supply from spikes. The placement of this component is crucial for the correct working of the circuitry. A misplaced component can be useless or can even decrease the power supply performances.

- The Bypass low ESR capacitor must be placed close to the Telit NL865B1 power input pads or in the case the power supply is a switching type it can be placed close to the inductor to cut the ripple provided the PCB trace from the capacitor to the NL865B1 is wide enough to ensure a dropless connection even during an 1A current peak.
- The protection diode must be placed close to the input connector where the power source is drained.
- The PCB traces from the input connector to the power regulator IC must be wide enough to ensure no voltage drops occur when a 500mA current peak is absorbed.
- The PCB traces to the NL865B1 and the Bypass capacitor must be wide enough to ensure no significant voltage drops occur. This is for the same reason as previous point. Try to keep this trace as short as possible.
- To reduce the EMI due to switching, it is important to keep very small the mesh involved; thus the input capacitor, the output diode (if not embodied in the IC) and the regulator have to form a very small loop. This is done in order to reduce the radiated field (noise) at the switching frequency (100-500 kHz usually).
- A dedicated ground for the Switching regulator separated by the common ground plane is suggested.
- The placement of the power supply on the board should be done in such a way to guarantee that the high current return paths in the ground plane are not overlapped to any noise sensitive circuitry as the microphone amplifier/buffer or earphone amplifier.
- The power supply input cables should be kept separate from noise sensitive lines such as microphone/earphone cables.
- VBATT and VBATT_PA can be connected together
- The insertion of EMI filter on VBATT pins is suggested in those designs where antenna is placed close to battery or supply lines.

  A ferrite bead like Murata BLM18EG101TN1 or Taiyo Yuden P/N FBMH1608HM101 can be used for this purpose.

The below figure shows the recommended circuit:



4.4. VAUX/PWRMON Power Output

A 1.8V regulated power supply output is provided in order to supply small devices from the module. The signal is present on Pad 43

This output is always active as long as the module is powered (VBATT applied). It is also active during module sleep mode/ PSM mode.

The operating range characteristics of the supply are:

Item	Min	Typical	Max
Output voltage	1.7V	1.80V	1.9V
Output current	-	-	50mA
Output bypass capacitor (inside the module)		100nF	

NOTE:
The Output Current MUST never be exceeded; care must be taken when designing the application section to avoid having an excessive current consumption.
If the Current is exceeding the limits it could cause a Power Off of the module.

Warning:
The current consumption from VAUX/PWRMON increases the modem temperature.

4.5. 3GPP Power Saving Mode (PSM)

The NL865 is supporting a new feature introduced in 3GPP Rel.12 that allows the Module to skip idle mode tasks for a longer time period while still maintaining the NAS context. This feature permits to reduce the overall power consumption when there is no required data activity with the network for a long time.

Additional hardware lines are defined to support this feature and to synchronize the activities with the external Host processor.

PINS DESCRIPTION

Signal	Function	I/O	PAD
LP_WAKE	Low power Wake Up. Used to wakeup the NL865 from any of the low power modes	I	19
SLP_IND	PSM/Sleep indication. “0” – NL865B1 is in lowest power mode “1” - NL865B1 is not in lowest power mode	O	48

5. DIGITAL SECTION

5.1. Logic Levels

ABSOLUTE MAXIMUM RATINGS:

Parameter	Min	Max
Input level on any digital pin (CMOS 1.8) with respect to ground	-0.3V	2.1V
Input level on any digital pin (CMOS 1.8) with respect to ground when VBATT is not supplied	-0.3V	0.3V

OPERATING RANGE - INTERFACE LEVELS (1.8V CMOS):

Parameter	Min	Max
Input high level	1.25V	1.95V
Input low level	0V	0.35V
Output high level	1.42V	1.85V
Output low level	0V	0.2V

LEAKAGE CURRENT CHARACTERISTICS:

Parameter	AVG
Input leakage current	±10uA
Output leakage current	±10uA

DRIVE STRENGTH

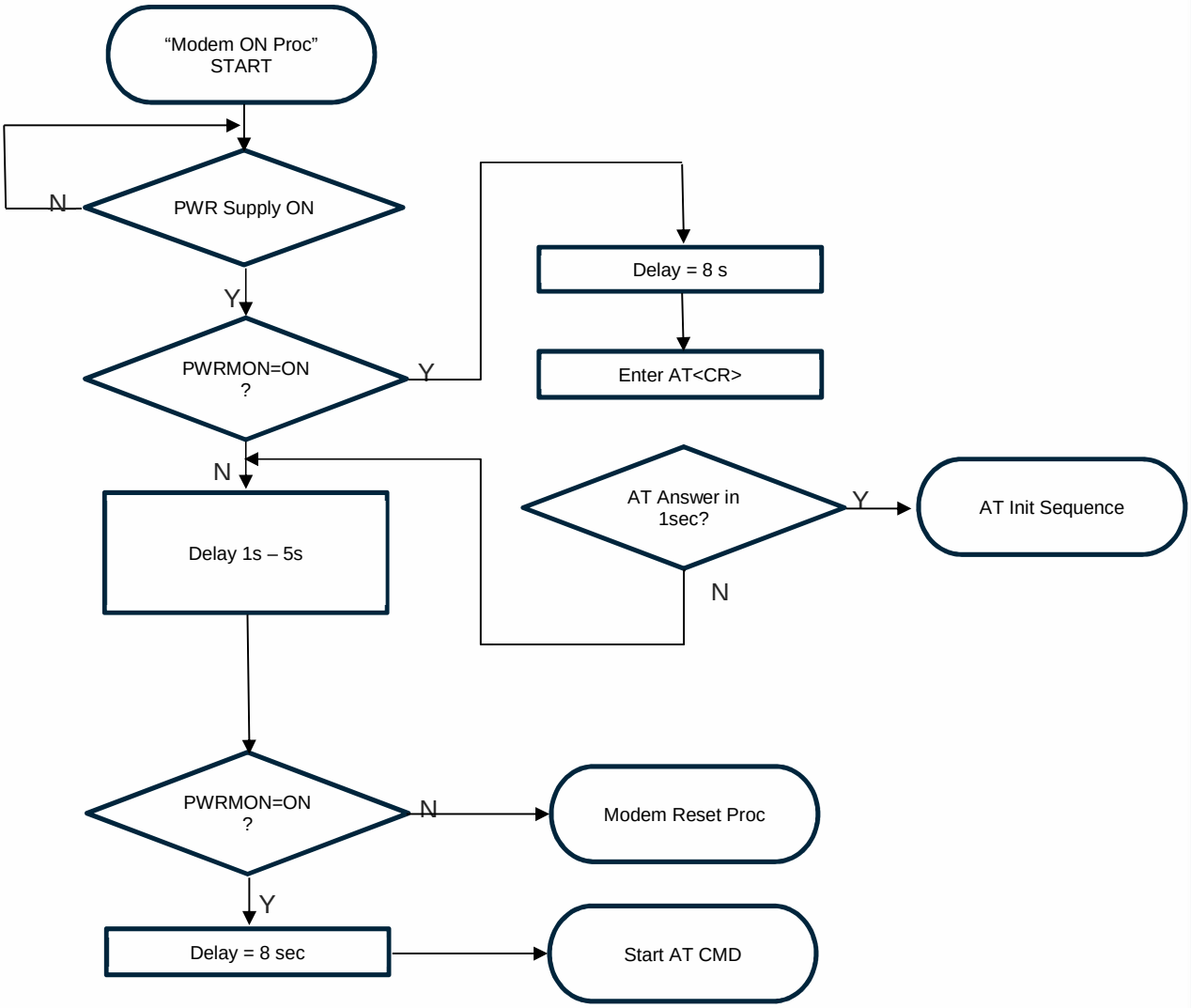
Parameter	AVG
Max drive strength	10mA

5.2. Power On

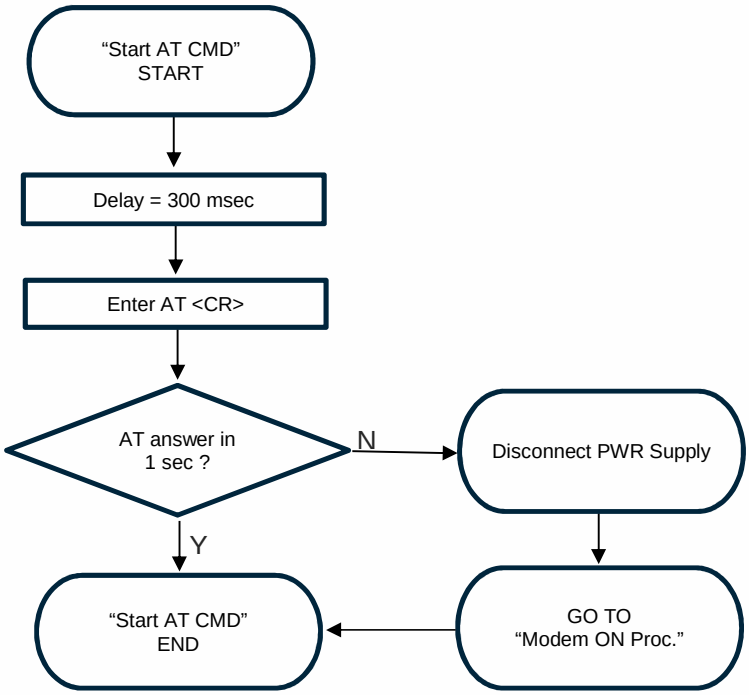
The NL865B1 will automatically power on itself when VBATT is applied to the module.

VAUX / PWRMON pin will be then set at the high logic level.

The following flow chart shows the proper turn on procedure:



A flow chart showing the AT commands managing procedure is displayed below:



5.3. Unconditional Restart

To unconditionally restart the NL865B1, the pad RESET* must be tied low for at least 200 milliseconds and then released.
The maximum current that can be drained from the RESET* pad is 1 mA.
The hardware unconditional Restart must not be used during normal operation of the device since it does not detach the device from the network. It shall be kept as an emergency exit procedure to be done in the rare case that the device gets stuck waiting for some network or SIM responses.

Do not use any pull up resistor on the RESET* line nor any totem pole digital output. Using pull up resistor may bring to latch up problems on the NL865B1 power regulator and improper functioning of the module.
The line RESET* must be connected only in open collector configuration; the transistor must be connected as close as possible to the RESET* pin.

The unconditional hardware restart must always be implemented on the application board as the software must be able to use it as an emergency exit procedure.

PIN DESCRIPTION

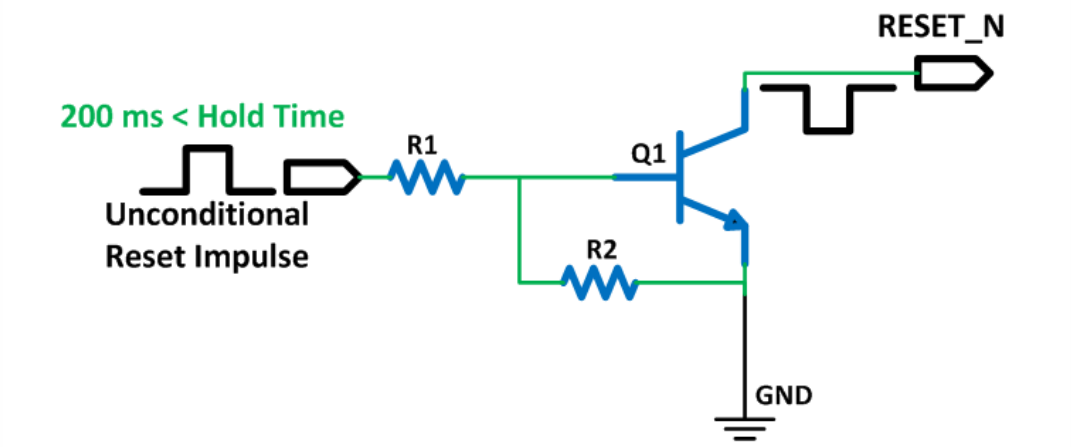
Signal	Function	I/O	PAD
RESET*	Unconditional Reset of the Module	I	47

OPERATING LEVELS

The RESET* line is connected to 1.8V with a Pull Up so the electrical levels are on this pin are aligned with the other CMOS 1.8V digital I/O's.

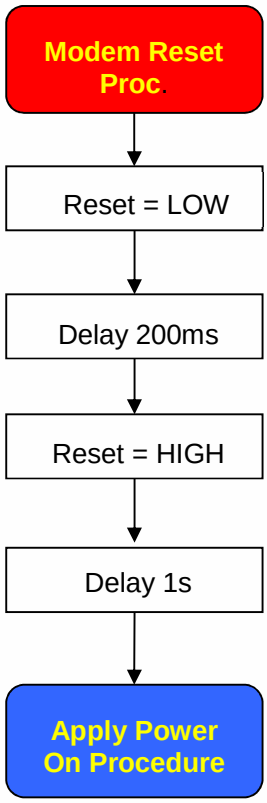
WARNING:
The hardware unconditional Reset must not be used during normal operation of the device since it does not detach the device from the network. It shall be kept as an emergency exit procedure.

A typical circuit for implementing an unconditional RESET is shown below:



NOTE:
In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the NL865B1 when the module is powered off or during a reboot transition.
Using bidirectional level translators which do not support High Z mode during power off is not recommended.

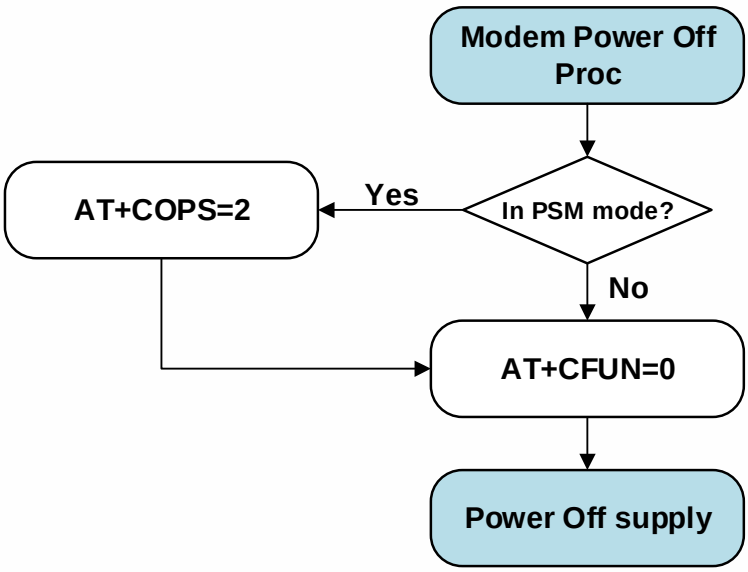
In the following flow chart is detailed the proper restart procedure:



In order to prevent a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the NL865B1 when the module is powered OFF or during an ON/OFF transition.
Using bidirectional level translators which do not support High Z mode during power off is not recommended.

5.4. Power OFF procedure

The NL865B1 does not provide any means of software driven shutdown.
In case that power off is required (for example when modem is not used for a long time), the below procedure should be followed in order to eliminate the posible damage due to unexpected power cut.



5.5. Communication ports

5.5.1. Serial Ports

The NL865B1 module is provided with by 2 Asynchronous serial ports:

- MODEM SERIAL PORT 1 (Main)
- MODEM SERIAL PORT 2 (TX Only, used for logging)

Several configurations can be designed for the serial port on the OEM hardware, but the most common are:

- RS232 PC com port
- microcontroller UART @ 1.8V (Universal Asynchronous Receive Transmit)
- microcontroller UART @ 5V or other voltages different from 1.8V

Depending from the type of serial port on the OEM hardware a level translator circuit may be needed to make the system work.

On the NL865B1 the ports are CMOS 1.8.

5.5.1.1. MODEM SERIAL PORT 1

The serial port 1 on the NL865B1 is a +1.8V UART with only 4 RS232 signals.

It differs from the PC-RS232 in the signal polarity (RS232 is reversed) and levels.

The following table lists the available signals:

RS232 Pin	Signal	Pad	Name	Usage
2	RXD	8	Transmit line *see Note	Output transmit line of NL865B1 UART
3	TXD	7	Receive line *see Note	Input receive of the NL865B1 UART
5	GND	23, 32, 33, 35, 36, 46	Ground	Ground

NOTE:
According to V.24, some signal names are referred to the application side, therefore on the NL865B1 side these signal are on the opposite direction:
TXD on the application side will be connected to the receive line (here named TXD)
RXD on the application side will be connected to the transmit line (here named RXD)
For a minimum implementation, only the TXD, RXD lines can be connected.
In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the NL865B1 when the module is powered off or during a reboot transition.
Using bidirectional level translators which do not support High Z mode during power off is not recommended.

NOTE:
By default, since UART port uses the low power mode, HW flow control is not used

5.5.1.2. MODEM SERIAL PORT 2

The secondary serial port on the NL865B1 is a CMOS1.8V with only TX signal which is used for logging.

The signals of the NL865B1 serial port are:

PAD	Signal	I/O	Function	Type	NOTE
45	TX_AUX	O	Auxiliary UART (TX Data to DTE)	CMOS 1.8V	Main Debug & logging port

NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the NL865B1 when the module is not supplied or during a powerup/reboot transition.

Using bidirectional level translators which do not support High Z mode during power off is not recommended.

5.5.1.3. RS232 LEVEL TRANSLATION

In order to interface the NL865B1 with a PC com port or a RS232 (EIA/TIA-232) application a level translator is required. This level translator must:

- invert the electrical signal in both directions;
- Change the level from 0/1.8V to +15/-15V.

The RS232 UART 16450, 16550, 16650 & 16750 chipsets accept signals with lower levels on the RS232 side (EIA/TIA-562), allowing a lower voltage-multiplying ratio on the level translator. Note that the negative signal voltage must be less than 0V and hence some sort of level translation is always required.

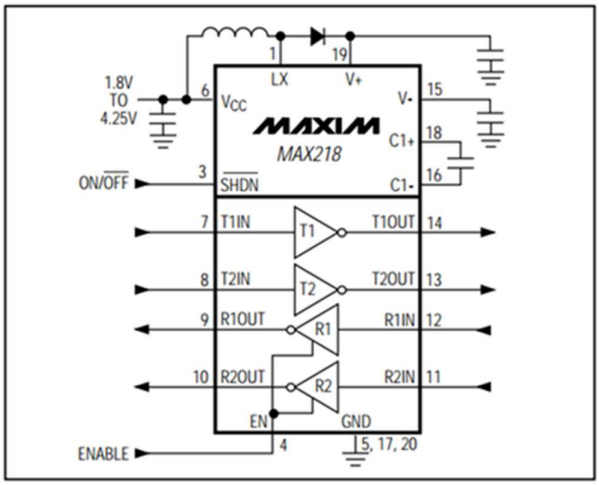
The simplest way to translate the levels and invert the signal is by using a single chip level translator. There are a multitude of them, differing in the number of drivers and receivers and in the levels (be sure to get a true RS232 level translator not a RS485 or other standards).

By convention the driver is the level translator from the 0-1.8V UART to the RS232 level. The receiver is the translator from the RS232 level to 0-1.8V UART.
In order to translate the whole set of control lines of the UART you will need:

- 5 drivers
- 3 receivers

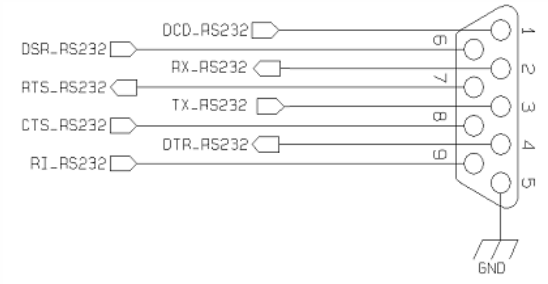
An example of RS232 level adaptation circuitry could be done using a MAXIM transceiver (MAX218).

In this case the chipset is capable to translate directly from 1.8V to the RS232 levels (Example done on 4 signals only).



NOTE:
The digital input lines operating at 1.8V CMOS have an absolute maximum input voltage of 2.2V. The level translator IC outputs on the module side (i.e. module inputs) will cause damage to the module inputs if the level translator is powered by a +3.8V supply. So the level translator IC must be powered from a dedicated +1.8V power supply to match the module I/O level.

The RS232 serial port lines are usually connected to a DB9 connector with the following layout:



5.6. General purpose I/O

The NL865B1 module is provided by a set of Configurable Digital Input / Output pins (CMOS 1.8V)

Input pads can only be read; they report the digital value (high or low) present on the pad at the read time.

Output pads can only be written or queried and set the value of the pad output.

An alternate function pad is internally controlled by the NL865B1 firmware and acts depending on the function implemented.

The following table shows the available GPIO on the NL865B1:

PAD	Signal	I/O	Default State	NOTE
42	GPIO_01	I/O	Input, No Pull	
41	GPIO_02	I/O	Input, No Pull	
40	GPIO_03	I/O	Input, No Pull	
39	GPIO_04	I/O	Input, No Pull	
29	GPIO_05/SIMIN	I/O	Input, Weak PullUp	SIMIN – for modules ordered with eSIM *GPIO_05 – for modules ordered without eSIM
28	GPIO_06	I/O	Input, No Pull	
27	GPIO_07	I/O	Input, No Pull	
26	GPIO_08	I/O	Input, No Pull	

NOTE:
The internal GPIO's pull up/pull down could be set to the preferred status for the application using the AT#GPIO command.
Please refer for the AT Commands User Guide for the detailed command Syntax.

WARNING:

During power up the GPIOs may be subject to transient glitches.

5.6.1. Using a GPIO as INPUT

The GPIO pads, when used as inputs, can be connected to a digital output of another device and report its status, provided this device has interface levels compatible with the 1.8V CMOS levels of the GPIO. If the digital output of the device to be connected with the GPIO input pad has interface levels different from the 1.8V CMOS, then it should be buffered with an open collector transistor with a 47K pull up to VAUX.

Any of the GPIO's 1 => 8 can be used as an interrupt source. User can configure the interrupt for either faling or rising edge

Any of the GPIO's 1 => 8 can be used as a wakeup source thus waking up the module from sleep. User can configure the wakeup for either faling or rising edge

NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the NL865B1 when the module is powered off or during a powerup/reboot transition.

Using bidirectional level translators which do not support High Z mode during power off is not recommended.

The VAUX /PWRMON pin can be used for input pull up reference.

5.6.2. Using a GPIO as OUTPUT

The GPIO pads, when used as outputs, can drive 1.8V CMOS digital devices or compatible hardware. When set as outputs, the pads have a push-pull output and therefore the pull-up resistor may be omitted.

5.7. I2C Port

The NL865B1 supports a dedicated port for I2C communication

I2C speed is limited to 10KHz.

The following table lists the available I2C signals on the NL865B1:

PAD	Signal	I/O	Default State	NOTE
6	I2C_SDA	I/O	Pull Up	
44	I2C_SCL	I/O	Pull Up	

Please refer to the AT command user guide for more information.

5.8. External SIM Holder

Please refer to the related User Guide (SIM Holder Design Guides, 80000NT10001a).

5.8.1. SIMIN Detection

PIN 29 is used as SIM DETECT input.

As long as SIMIN is not pulled low by the application board the module will use the internal eSIM.

For using an external SIM the user must assert SIMIN low

NL865B1 modules ordered without eSIM support will always use the external SIM regardless of the SIMIN state

NL865B1 modules ordered without eSIM support, can use pin 29 as GPIO_05

5.9. ADC Converter

The NL865B1 is provided by one ADC converter. It is able to read a voltage level in the range of 0.2÷1.7 volts applied on the ADC pin input, store and convert it into 10 bit word. The input line is named as **ADC_IN1** and it is available on Pad 13

The following table is showing the ADC characteristics:

Item	Min	Typical	Max	Unit
Input Voltage range	0.2	-	1.7	Volt
AD conversion	-	-	10	bits

6. RF SECTION

6.1. Bands Variants

The following table is listing the supported Bands:

Product	Supported LTE bands
NL865B1E1	*FDD B8, B20*

6.2. TX Output power

Product	Band	Power Class
NL865B1-E1	*FDD B8, B20*	*Class 3 (23dBm), Class 5 (20dBm)*

6.3. RX Sensitivity

Technology	3GPP Compliance
NB-IoT	-108.2dBm

NOTE:

For low data rates sensitivity will be better than 3GPP spec

6.5. Antenna requirements

6.5.1. Main Antenna

The antenna connection and board layout design are the most important aspect in the full product design as they strongly affect the product overall performances, hence read carefully and follow the requirements and the guidelines for a proper design.

The antenna and antenna transmission line on PCB for a Telit NL865B1 device shall fulfil the following requirements:

Item	Value
Frequency range	Depending by frequency band(s) provided by the network operator, the customer shall use the most suitable antenna for that/those band(s)
Bandwidth	LTE Band VIII (900) : 80 MHz LTE Band XX (800) : 71 MHz : 47 MHz
Impedance	50 ohm
Input power	> 23dBm Average power
VSWR absolute max	≤ 10:1 (limit to avoid permanent damage)
VSWR recommended	≤ 2:1 (limit to fulfill all regulatory requirements)

6.5.2. PCB design guidelines

When using the NL865B1, since there's no antenna connector on the module, the antenna must be connected to the NL865B1 antenna pad by means of a transmission line implemented on the PCB.

This transmission line shall fulfil the following requirements:

Item	Value
Characteristic Impedance	50 ohm
Max Attenuation	0.3 dB
Coupling	Coupling with other signals shall be avoided
Ground Plane	Cold End (Ground Plane) of antenna shall be equipotential to the NL865B1 ground pins

The transmission line should be designed according to the following guidelines:

- Ensure that the antenna line impedance is 50 ohm;
- Keep the antenna line on the PCB as short as possible, since the antenna line loss shall be less than 0.3 dB;
- Antenna line must have uniform characteristics, constant cross section; avoid meanders and abrupt curves;
- Keep, if possible, one layer of the PCB used only for the Ground plane;
- Surround (on the sides, over and under) the antenna line on PCB with Ground, avoid having other signal tracks facing directly the antenna line track;
- The ground around the antenna line on PCB has to be strictly connected to the Ground Plane by placing vias every 2mm at least;
- Place EM noisy devices as far as possible from NL865B1 antenna line;
- Keep the antenna line far away from the NL865B1 power supply lines;
- If you have EM noisy devices around the PCB hosting the NL865B1, such as fast switching ICs, take care of the shielding of the antenna line by burying it inside the layers of PCB and surround it with Ground planes, or shield it with a metal frame cover.

- If you don't have EM noisy devices around the PCB of NL865B1, by using a micro strip on the superficial copper layer for the antenna line, the line attenuation will be lower than a buried one;

6.5.3. Antenna installation Guidelines

Install the antenna in a place covered by the LTE signal.

Antenna shall not be installed inside metal cases.

Antenna shall be installed also according to antenna manufacturer instructions.

7. MECHANICAL DESIGN

7.1. Mechanical Dimensions

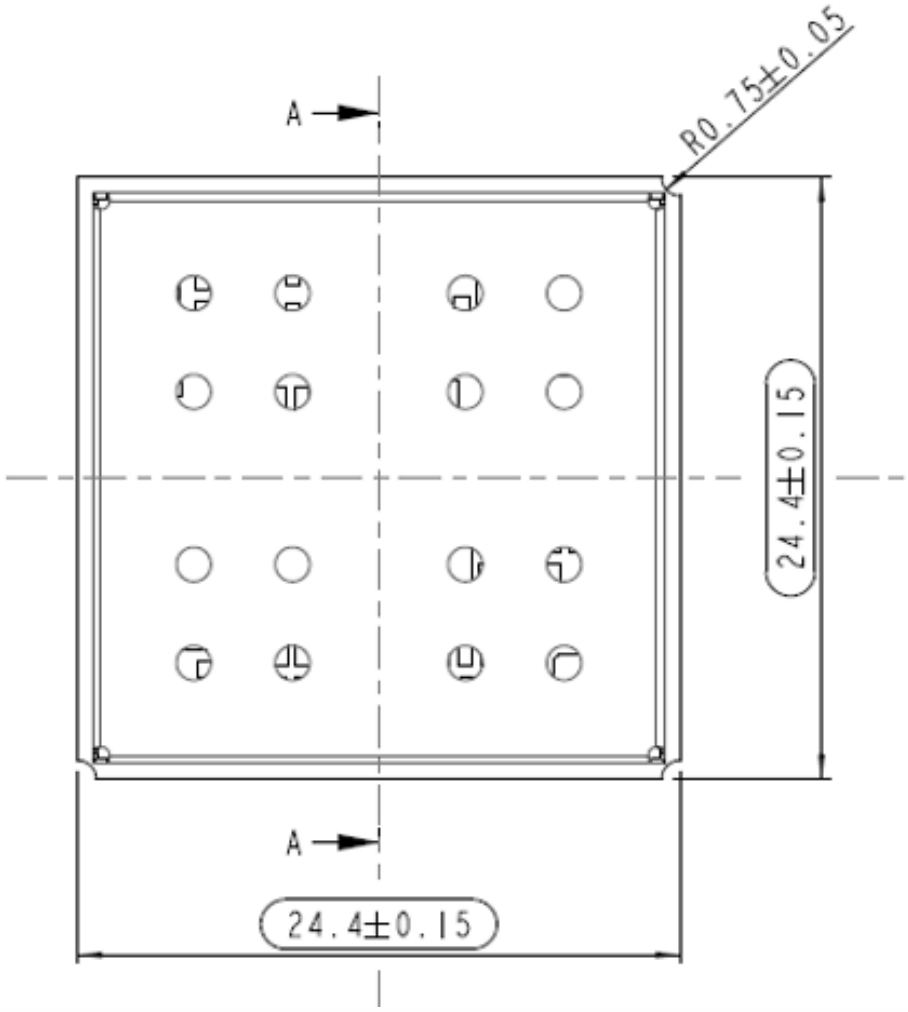
The NL865B1 overall dimensions are:

- Length: 24.4 mm
- Width: 24.4 mm
- Thickness: 2.45 mm (excluding Lable thikness)
- Weight: 2.5 gr

7.1.1. Mechanical Drawing

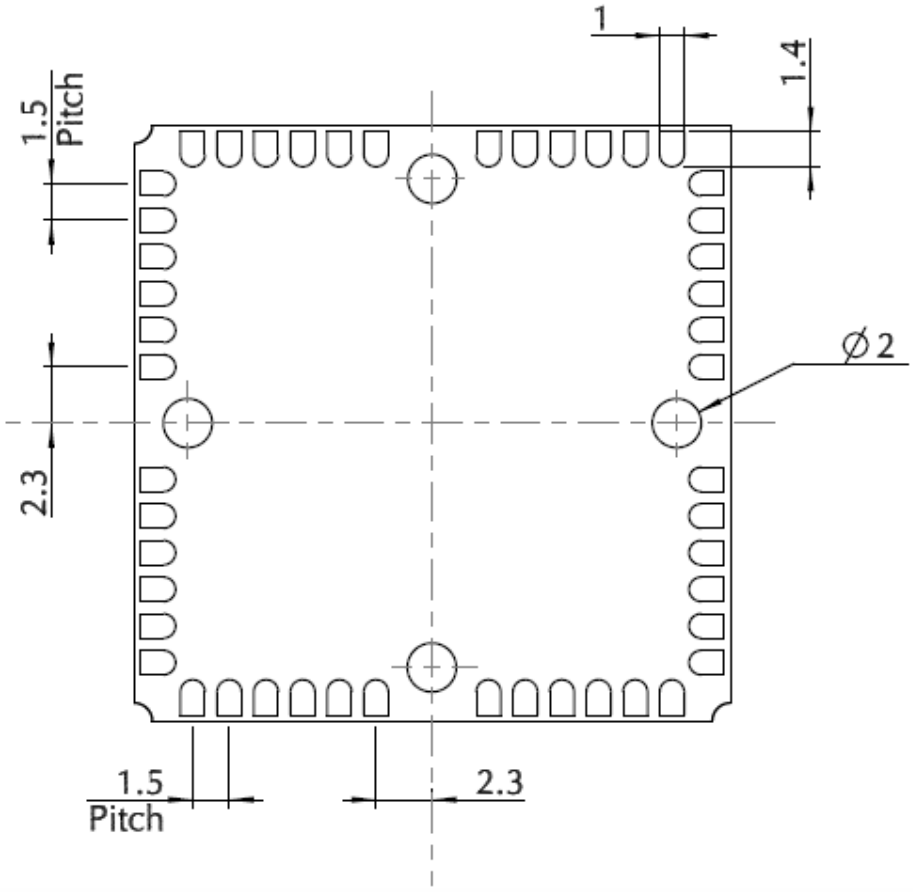
7.1.2. Top View

The figure below shows mechanical top view of the NL865B1

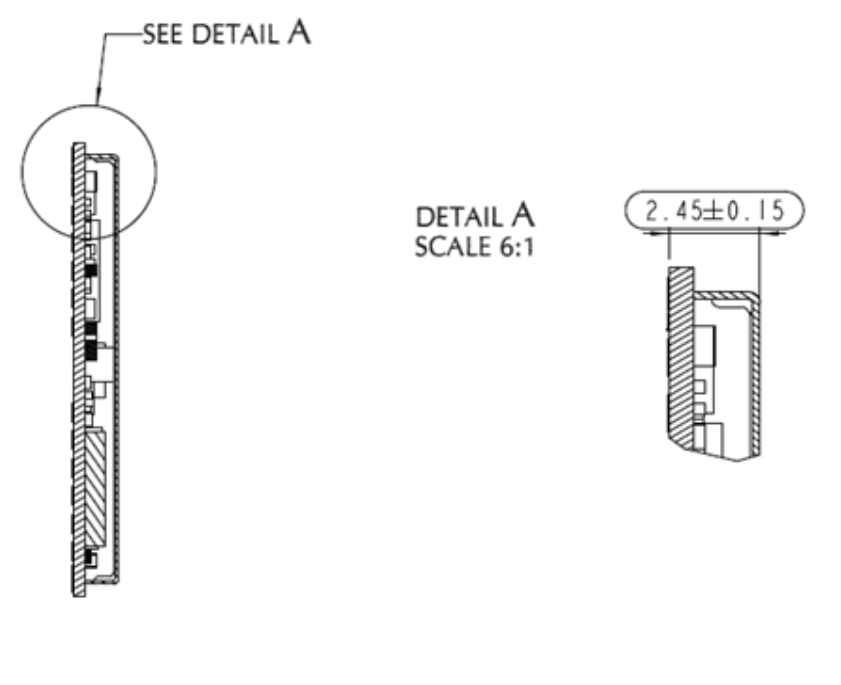


Dimensions are in mm

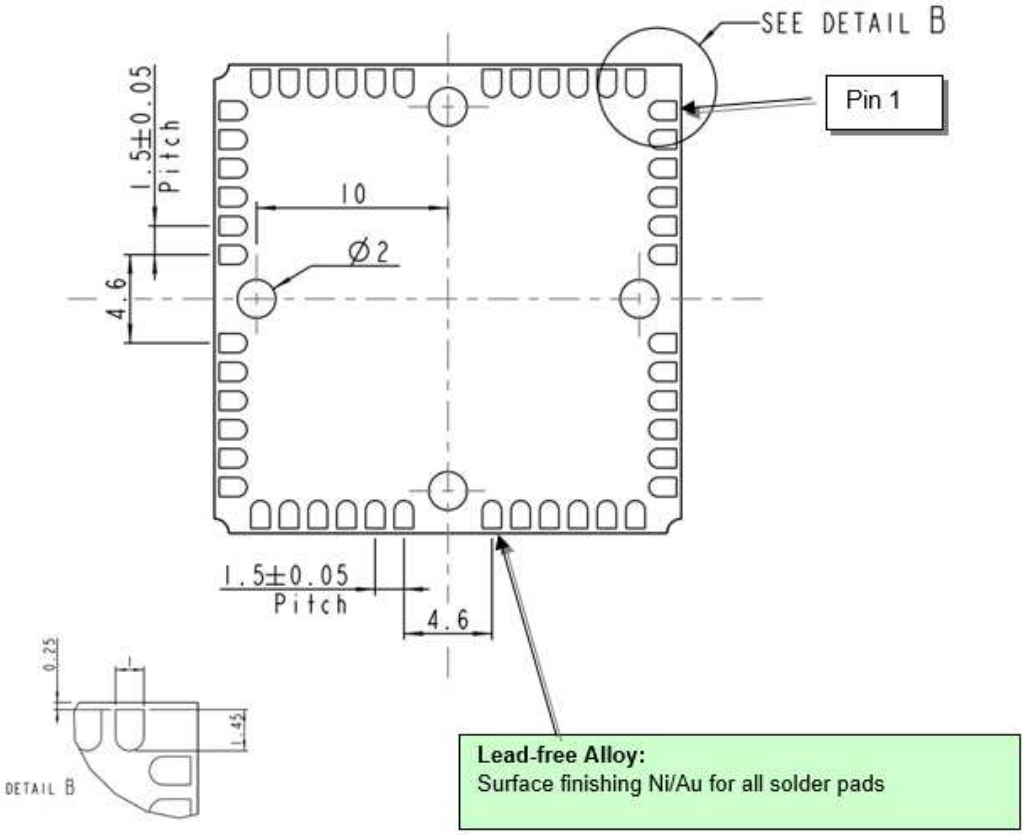
7.1.3. Bottom View (as seen from bottom side)



7.1.4. Side View



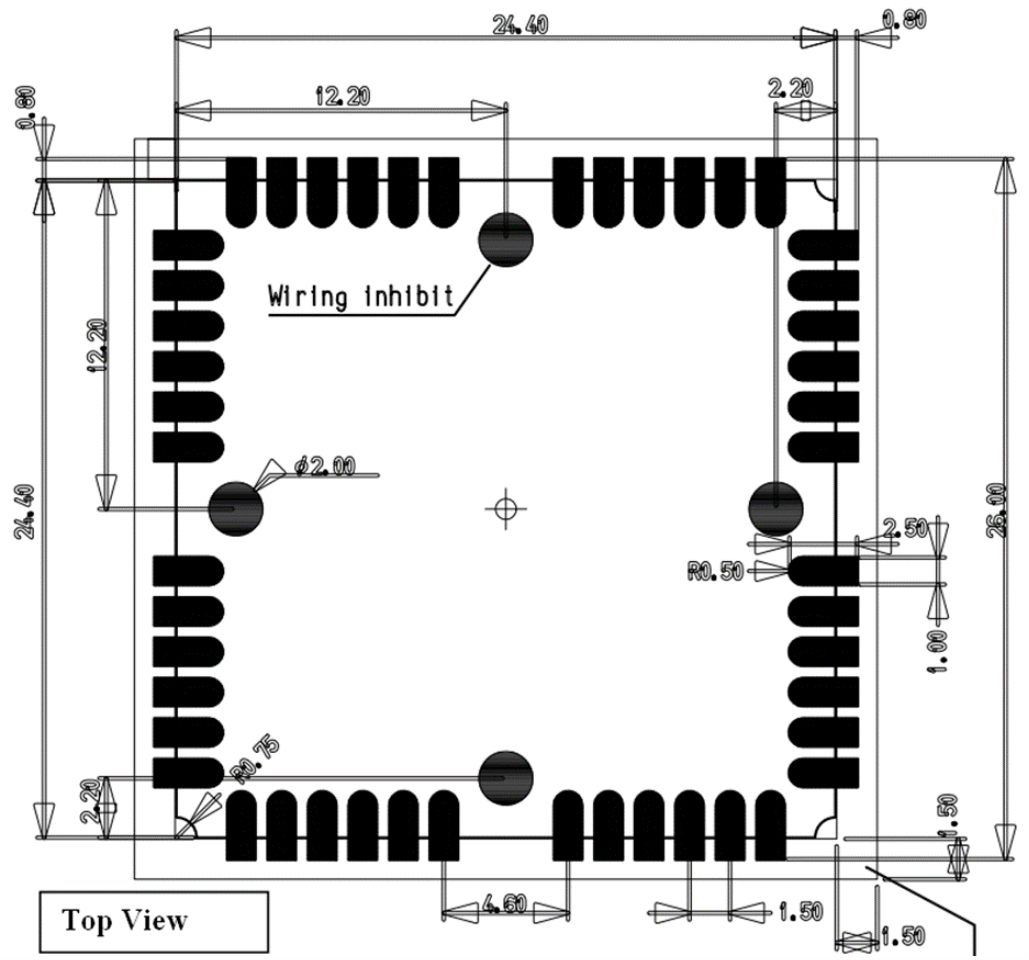
7.1.5. Module finishing & dimensions



8. APPLICATION PCB DESIGN

The NL865B1 modules have been designed in order to be compliant with a standard lead-free SMT process

8.1. Recommended footprint for the application



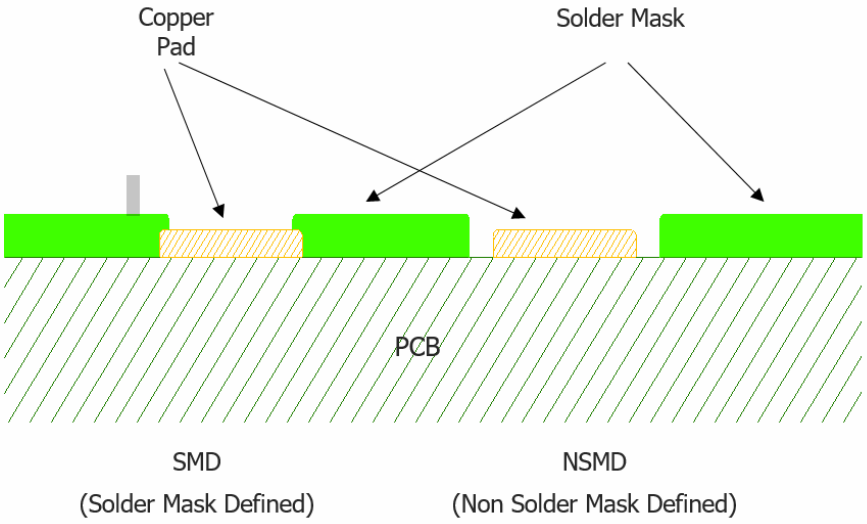
Dimensions are in mm

In order to easily rework the NL865B1 is suggested to consider on the application a 1.5 mm placement inhibit area around the module. It is also suggested, as common rule for an SMT component, to avoid having a mechanical part of the application in direct contact with the module.

The area under WIRING INHIBIT (see figure above) must be clear from signal or ground paths.

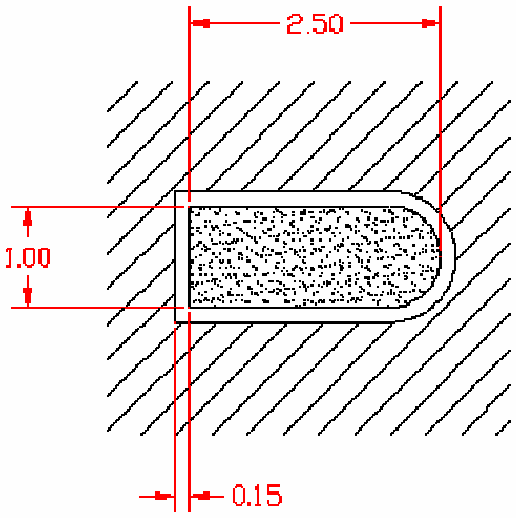
8.2. PCB pad design

Non solder mask defined (NSMD) type is recommended for the solder pads on the PCB.



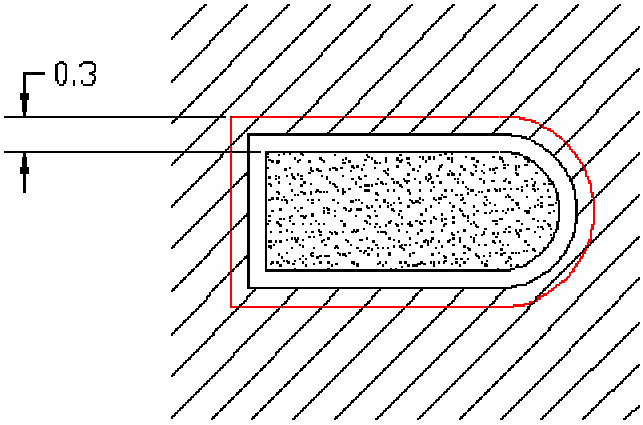
8.3. PCB pad dimensions

The recommendation for the PCB pads dimensions are described in the following image (dimensions in mm)



It is not recommended to place via or micro-via not covered by solder resist in an area of 0.3 mm around the pads unless it carries the same signal of the pad itself (see figure below).

Holes in pad are allowed only for blind holes and not for through holes.



Recommendations for PCB pad surfaces:

Finish	Layer Thickness (um)	Properties
Electro-less Ni / Immersion Au	3 –7 / 0.05 – 0.15	good solder ability protection, high shear force values

The PCB must be able to resist the higher temperatures which are occurring at the lead-free process. This issue should be discussed with the PCB-supplier. Generally, the wettability of tin-lead solder paste on the described surface plating is better compared to lead-free solder paste.

It is not necessary to panel the application's PCB, however in that case it is suggested to use milled contours and predrilled board breakouts; scoring or v-cut solutions are not recommended.

8.4. Stencil

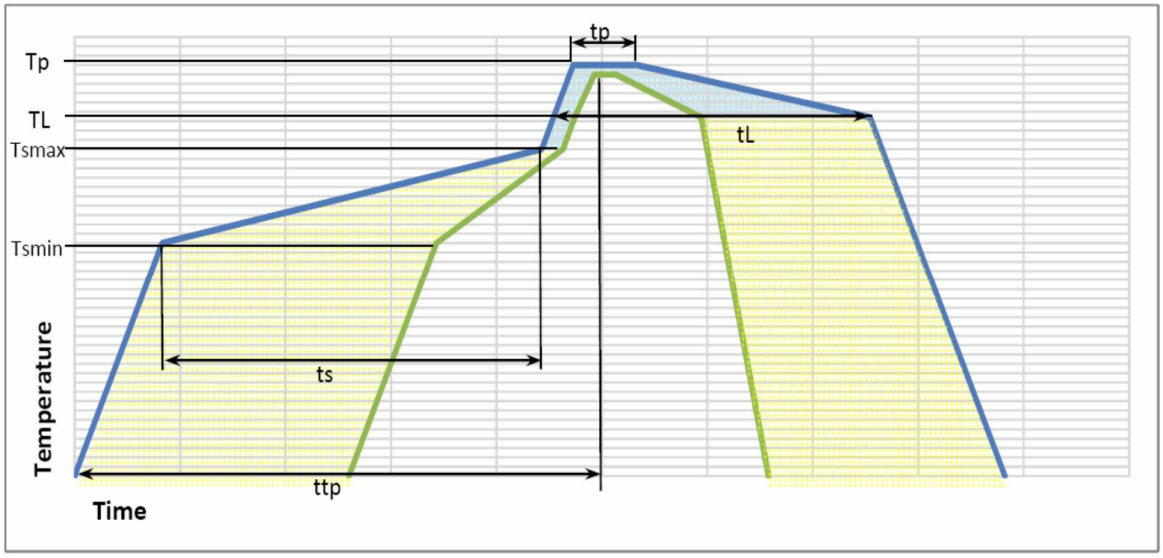
Minimum stencil thickness recommended is 125um

8.5. Solder paste

We recommend using only "no clean" solder paste in order to avoid the cleaning of the modules after assembly.

8.6. NL865B1 Solder reflow

Recommended solder reflow profile



Profile Feature	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max
Preheat – Temperature Min (Tsmin) – Temperature Max (Tsmax) – Time (min to max) (ts)	 150°C 200°C 60-180 seconds
Tsmax to TL – Ramp-up rate	 3°C/second max
Time maintained above: – Temperature (TL) – Time (tL)	 217°C 60-150 seconds
Peak temperature (Tp)	245 +0/-5°C
Time within 5°C of actual peak temperature (tp)	10-30 seconds
Ramp-down rate	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

9. PACKING SYSTEM

9.1. Tray

The NL865B1 modules are packaged on trays

The tray is JEDEC compliant, injection molded antistatic Modified Polyphenylene ether (MPPO). It has good thermal characteristics and can withstand a standard baking temperature of up to 125°C, thereby avoiding handling the modules if baking is required. The trays are rigid, thus providing mechanical protection against transport stress. In addition, they are re-usable and so environmentally sustainable.

There are 2 (two) antistatic rubber bands that enclose each envelope.

The carton box is rigid, offering mechanical protection. The carton box has one flap across the entire top surface. It is sealed with tape along the edges of the box.

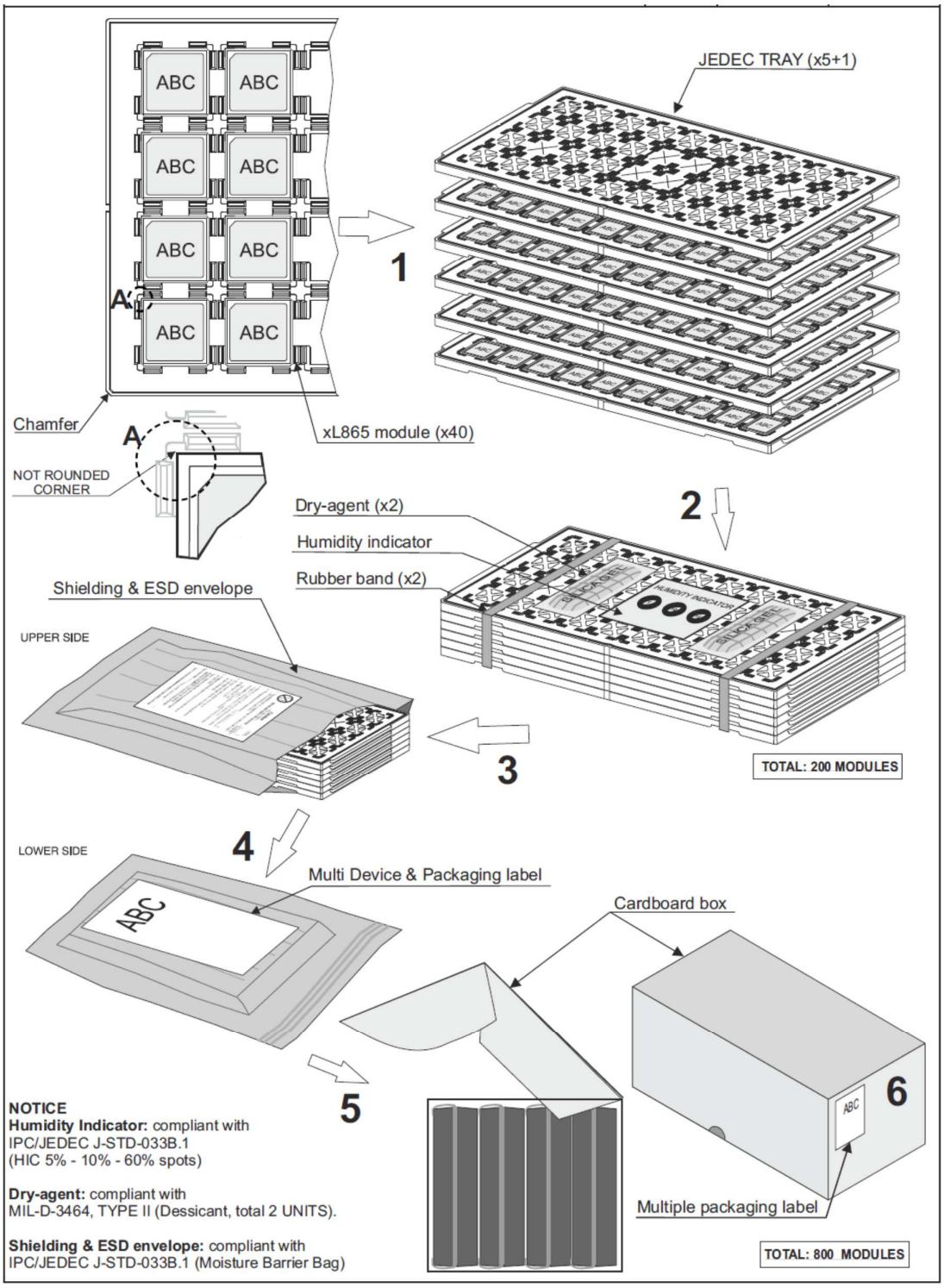
Table 1: Tray Packing

Modules per Tray	Trays per Envelope	Modules per Envelope	Envelopes per Carton Box	Modules per Box
40	5+ 1 empty	200	4	800

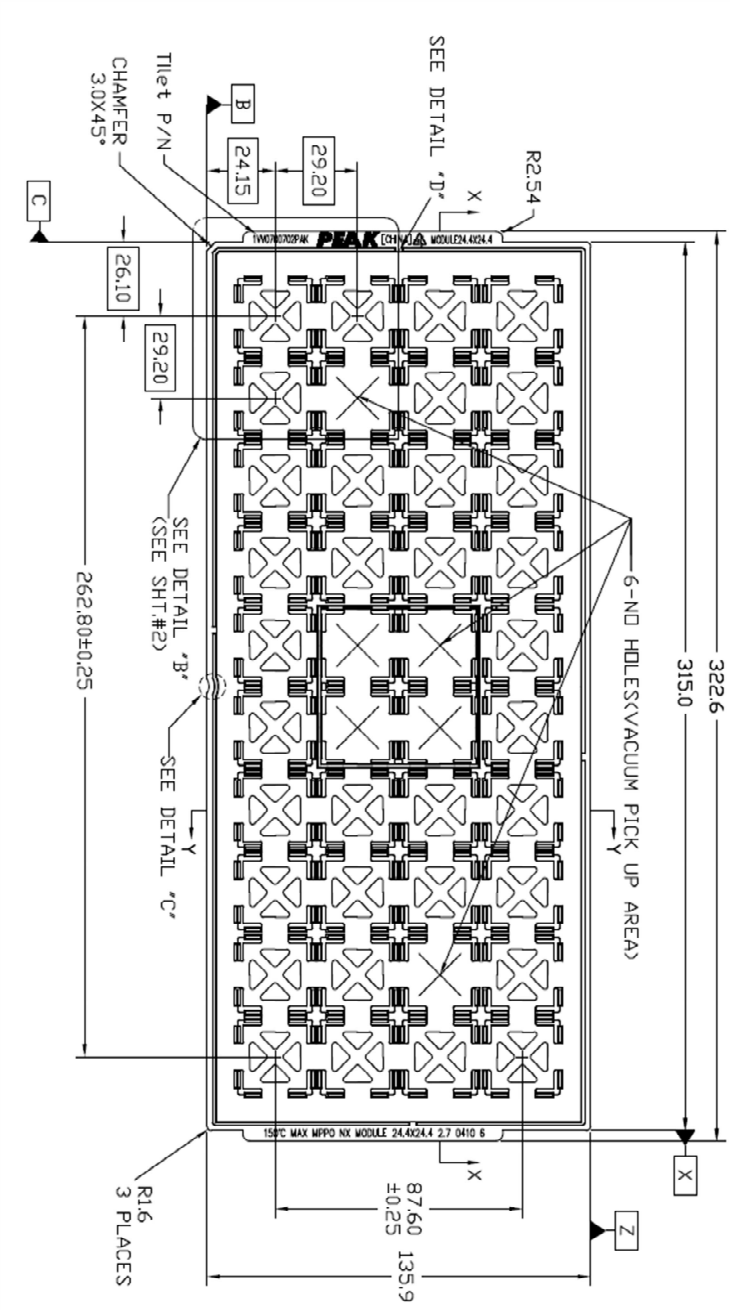
Table 2: Packing Quantities

Order Type	Quantity
Minimum Order Quantity (MOQ)	40
Standard Packing Quantity (SPQ)	200

Tray organization is shown in the figure below



9.2. Tray Drawing

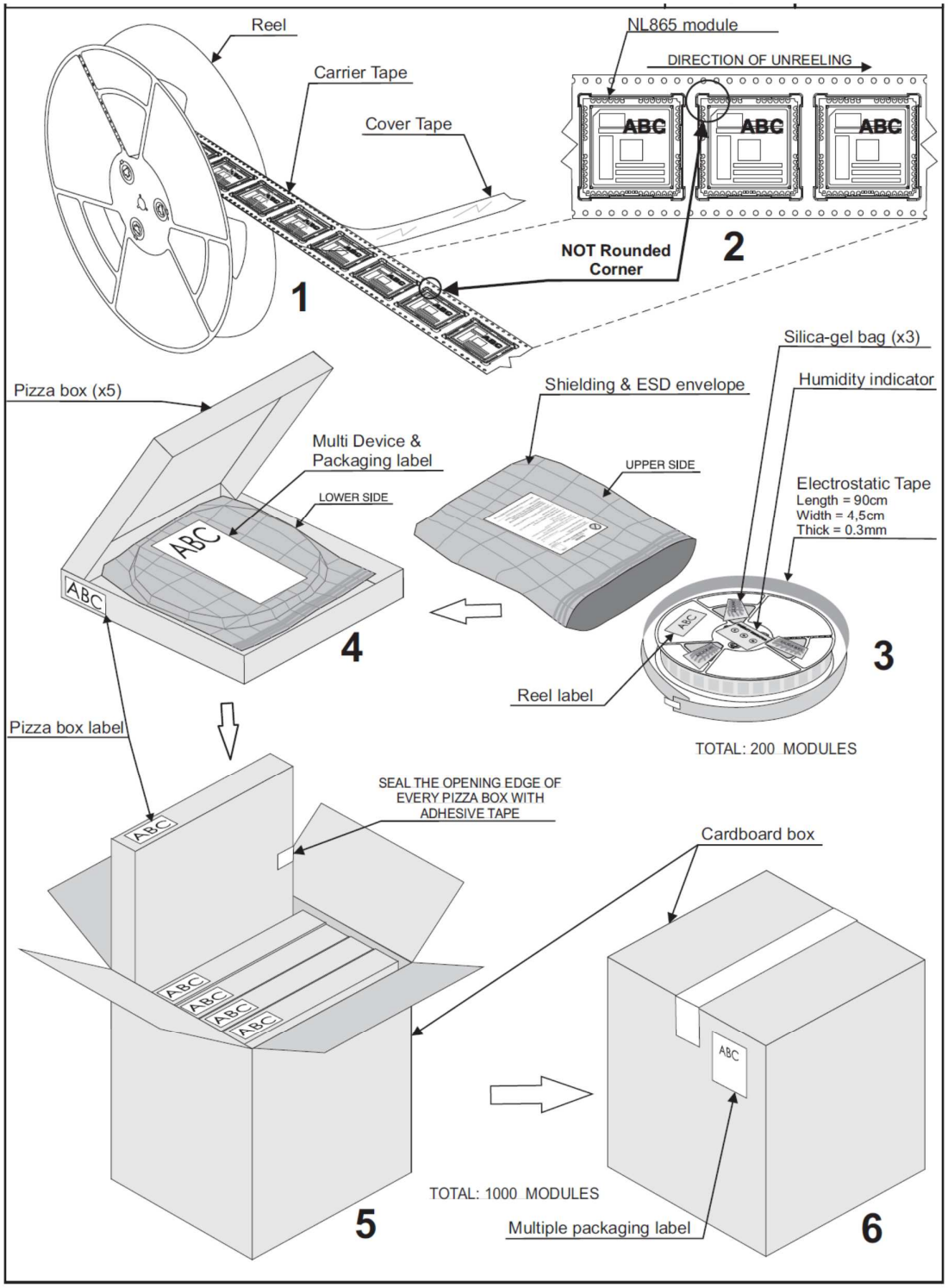


WARNING:
These trays can withstand a maximum temperature of 125℃.

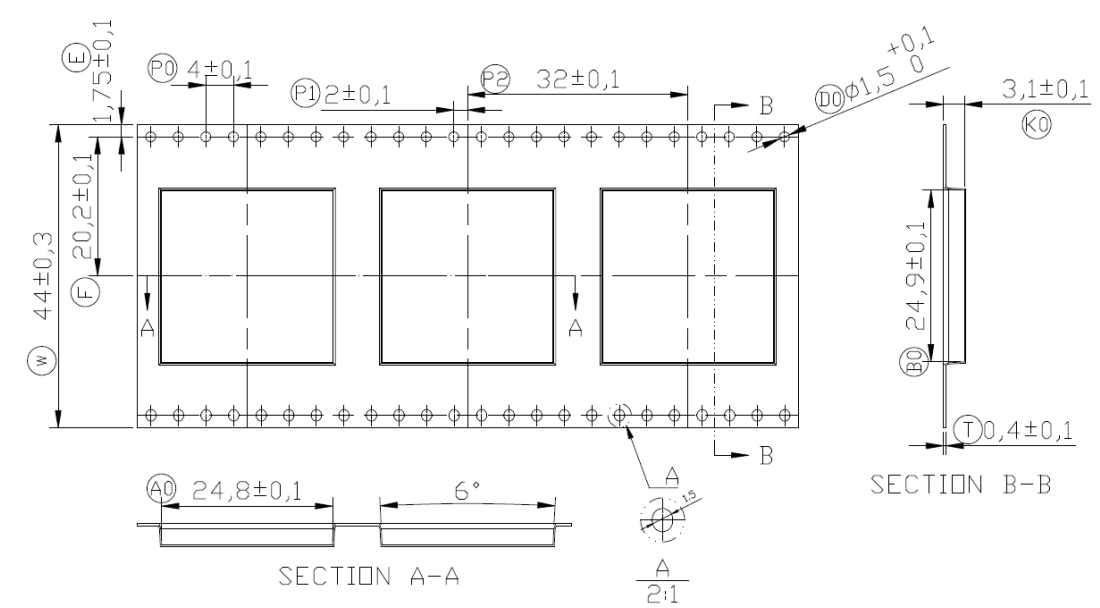
9.3. Tape & Reel

The NL865 modules are available on a T&R packaging as well

NL865B1 is packaged on reels of 200 pieces each as shown in the figure below.



9.4. Carrier Tape Drawing



9.5. Moisture sensitivity

The NL865B1 is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care all the relatives requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH).

b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5.

c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition b) “IPC/JEDEC J-STD-033A paragraph 5.2” is respected

d) Baking is required if conditions b) or c) are not respected

e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more

10. CONFORMITY ASSESSMENT ISSUES

10.1. Declaration of Conformity

The RED (2014/53/EU) DoC will be available here: http://www.telit.com\red

11. SAFETY RECOMMENDATIONS

11.1. READ CAREFULLY

Be sure the use of this product is allowed in the country and in the environment required. The use of this product may be dangerous and has to be avoided in the following areas:

- Where it can interfere with other electronic devices in environments such as hospitals, airports, aircrafts, etc.
- Where there is risk of explosion such as gasoline stations, oil refineries, etc. It is the responsibility of the user to enforce the country regulation and the specific environment regulation.

Do not disassemble the product; any mark of tampering will compromise the warranty validity. We recommend following the instructions of the hardware user guides for correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to be conformed to the security and fire prevention regulations. The product has to be handled with care, avoiding any contact with the pins because electrostatic discharges may damage the product itself. Same cautions have to be taken for the SIM, checking carefully the instruction for its use. Do not insert or remove the SIM when the product is in power saving mode.

The system integrator is responsible for the functioning of the final product; therefore, care has to be taken to the external components of the module, as well as any project or installation issue, because the risk of disturbing the GSM network or external devices or having impact on the security. Should there be any doubt, please refer to the technical documentation and the regulations in force. Every module has to be equipped with a proper antenna with specific characteristics. The antenna has to be installed with care in order to avoid any interference with other electronic devices and has to guarantee a minimum distance from the body (20 cm). In case this requirement cannot be satisfied, the system integrator has to assess the final product against the SAR regulation.

The European Community provides some Directives for the electronic equipment introduced on the market. All of the relevant information is available on the European Community website:

http://ec.europa.eu/enterprise/sectors/rtte/documents/

The text of the Directive 99/05 regarding telecommunication equipment is available,

while the applicable Directives (Low Voltage and EMC) are available at:

http://ec.europa.eu/enterprise/sectors/electrical/

12. REFERENCE TABLE OF RF BANDS CHARACTERISTICS

Mode	Freq. Tx (MHz)	Freq. Rx (MHz)	Channels	Tx-Rx Offset
PCS 1900	1850.2 ~ 1909.8	1930.2 ~ 1989.8	512 ~ 810	80 MHz
DCS 1800	1710 ~ 1785	1805 ~ 1880	512 ~ 885	95 MHz
GSM 850	824.2 ~ 848.8	869.2 ~ 893.8	128 ~ 251	45 MHz
EGSM 900	890 ~ 915	935 ~ 960	0 ~ 124	45 MHz
	880 ~ 890	925 ~ 935	975 ~ 1023	45 MHz
WCDMA 2100 – B1	1920 ~ 1980	2110 ~ 2170	Tx: 9612 ~ 9888 Rx: 10562 ~ 10838	190 MHz
WCDMA 1900 – B2	1850 ~ 1910	1930 ~ 1990	Tx: 9262 ~ 9538 Rx: 9662 ~ 9938	80 MHz
WCDMA 1800 – B3	1710 ~ 1785	1805 ~ 1880	Tx: 937 ~ 1288 Rx: 1162 ~ 1513	95 MHz
WCDMA AWS – B4	1710 ~ 1755	2110 ~ 2155	Tx: 1312 ~ 1513 Rx: 1537 ~ 1738	400 MHz
WCDMA 850 – B5	824 ~ 849	869 ~ 894	Tx: 4132 ~ 4233 Rx: 4357 ~ 4458	45 MHz
WCDMA 900 – B8	880 ~ 915	925 ~ 960	Tx: 2712 ~ 2863 Rx: 2937 ~ 3088	45 MHz
WCDMA 1800 – B9	1750 ~ 1784.8	1845 ~ 1879.8	Tx: 8762 ~ 8912 Rx: 9237 ~ 9387	95 MHz
WCDMA 800 – B19	830 ~ 845	875 ~ 890	Tx: 312 ~ 363 Rx: 712 ~ 763	45 MHz
TDSCDMA 2000 – B34	2010 ~ 2025	2010 ~ 2025	Tx: 10054 ~ 10121 Rx: 10054 ~ 10121	0 MHz
TDSCDMA 1900 – B39	1880 ~ 1920	1880 ~ 1920	Tx: 9404 ~ 9596 Rx: 9404 ~ 9596	0 MHz
LTE 2100 – B1	1920 ~ 1980	2110 ~ 2170	Tx: 18000 ~ 18599 Rx: 0 ~ 599	190 MHz

Mode	Freq. Tx (MHz)	Freq. Rx (MHz)	Channels	Tx-Rx Offset
LTE 1900 – B2	1850 ~ 1910	1930 ~ 1990	Tx: 18600 ~ 19199 Rx: 600 ~ 1199	80 MHz
LTE 1800 – B3	1710 ~ 1785	1805 ~ 1880	Tx: 19200 ~ 19949 Rx: 1200 ~ 1949	95 MHz
LTE AWS – B4	1710 ~ 1755	2110 ~ 2155	Tx: 19950 ~ 20399 Rx: 1950 ~ 2399	400 MHz
LTE 850 – B5	824 ~ 849	869 ~ 894	Tx: 20400 ~ 20649 Rx: 2400 ~ 2649	45 MHz
LTE 2600 – B7	2500 ~ 2570	2620 ~ 2690	Tx: 20750 ~ 21449 Rx: 2750 ~ 3449	120 MHz
LTE 900 – B8	880 ~ 915	925 ~ 960	Tx: 21450 ~ 21799 Rx: 3450 ~ 3799	45 MHz
LTE 1800 – B9	1749.9 ~ 1784.9	1844.9 ~ 1879.9	Tx: 21800 ~ 2149 Rx: 3800 ~ 4149	95 MHz
LTE AWS+ – B10	1710 ~ 1770	2110 ~ 2170	Tx: 22150 ~ 22749 Rx: 4150 ~ 4749	400 MHz
LTE 700a – B12	699 ~ 716	729 ~ 746	Tx : 23010 ~ 23179 Rx : 5010 ~ 5179	30 MHz
LTE 700c – B13	777 ~ 787	746 ~ 756	Tx : 27210 ~ 27659 Rx : 9210 ~ 9659	-31 MHz
LTE 700b – B17	704 ~ 716	734 ~ 746	Tx: 23730 ~ 23849 Rx: 5730 ~ 5849	30 MHz
LTE 800 – B19	830 ~ 845	875 ~ 890	Tx: 24000 ~ 24149 Rx: 6000 ~ 6149	45 MHz
LTE 800 – B20	832 ~ 862	791 ~ 821	Tx: 24150 ~ 24449 Rx: 6150 ~ 6449	-41 MHz
LTE 1500 – B21	1447.9 ~ 1462.9	1495.9 ~ 1510.9	Tx: 24450 ~ 24599 Rx: 6450 ~ 6599	48 MHz
LTE 850+ – B26	814 ~ 849	859 ~ 894	Tx: 26690 ~ 27039 Rx: 8690 ~ 9039	45 MHz

Mode	Freq. Tx (MHz)	Freq. Rx (MHz)	Channels	Tx-Rx Offset
LTE 700 – B28	703 ~ 748	758 ~ 803	Tx : 27210 ~ 27659 Rx : 9210 ~ 9659	45 MHz
LTE TDD 2600 – B38	2570 ~ 2620	2570 ~ 2620	Tx: 37750 ~ 38250 Rx: 37750 ~ 38250	0 MHz
LTE TDD 1900 – B39	1880 ~ 1920	1880 ~ 1920	Tx: 38250 ~ 38650 Rx: 38250 ~ 38650	0 MHz
LTE TDD 2300 – B40	2300 ~ 2400	2300 ~ 2400	Tx: 38650 ~ 39650 Rx: 38650 ~ 39650	0 MHz
LTE TDD 2500 – B41M	2555 ~ 2655	2555 ~ 2655	Tx: 40265 ~ 41215 Rx: 40265 ~ 41215	0 MHz

13. ACRONYMS

TTSC	Telit Technical Support Centre
USB	Universal Serial Bus
HS	High Speed
DTE	Data Terminal Equipment
UMTS	Universal Mobile Telecommunication System
WCDMA	Wideband Code Division Multiple Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
UART	Universal Asynchronous Receiver Transmitter
HSIC	High Speed Inter Chip
SIM	Subscriber Identification Module
SPI	Serial Peripheral Interface
ADC	Analog – Digital Converter
DAC	Digital – Analog Converter
I/O	Input Output
GPIO	General Purpose Input Output
CMOS	Complementary Metal – Oxide Semiconductor
MOSI	Master Output – Slave Input
MISO	Master Input – Slave Output
CLK	Clock
MRDY	Master Ready

SRDY	Slave Ready
CS	Chip Select
RTC	Real Time Clock
PCB	Printed Circuit Board
ESR	Equivalent Series Resistance
VSWR	Voltage Standing Wave Radio
VNA	Vector Network Analyzer
RED	Radio Equipment Directive

14. DOCUMENT HISTORY

Revision	Date	Changes
0	2017-09-03	First issue

SUPPORT INQUIRIES

Link to **www.telit.com** and contact our technical support team for any questions related to technical issues.

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