
# UE910-EU HARDWARE USER GUIDE

# APPLICABILITY TABLE

## PRODUCTS

- UE910-EU

# DISCLAIMER

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# CONTENTS

# 1 INTRODUCTION

## 1.1 Scope

The aim of this document is the description of some hardware solutions useful for developing a product with the Telit UE910-EU module.

## 1.2 Audience

This document is intended for Telit customers, who are integrators, about to implement their applications using our UE910-EU modules.

## 1.3 Contact Information, Support

For general contact, technical support services, technical questions and report documentation errors contact Telit Technical Support at:

TS-EMEA@telit.com

TS-AMERICAS@telit.com

TS-APAC@telit.com

Alternatively, use:

http://www.telit.com/support

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

http://www.telit.com

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

## 1.4 List of acronyms

| Acronym | Description |
|---|---|
| TTSC | Telit Technical Support Centre |
| USB | Universal Serial Bus |
| HS | High Speed |
| DTE | Data Terminal Equipment |
| LTE | Long Term Evolution |
| WCDMA | Wideband Code Division Multiple Access |
| HSDPA | High Speed Downlink Packet Access |
| HSUPA | High Speed Uplink Packet Access |
| UART | Universal Asynchronous Receiver Transmitter |
| HSIC | High Speed Inter Chip |
| SIM | Subscriber Identification Module |
| SPI | Serial Peripheral Interface |
| ADC | Analog – Digital Converter |
| DAC | Digital – Analog Converter |
| I/O | Input Output |
| GPIO | General Purpose Input Output |
| CMOS | Complementary Metal – Oxide Semiconductor |
| MOSI | Master Output – Slave Input |
| MISO | Master Input – Slave Output |
| CLK | Clock |
| MRDY | Master Ready |
| SRDY | Slave Ready |
| CS | Chip Select |
| RTC | Real Time Clock |
| PCB | Printed Circuit Board |
| ESR | Equivalent Series Resistance |
| VSWR | Voltage Standing Wave Radio |
| VNA | Vector Network Analyzer |

## 1.5 Text Conventions


Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

## 1.6. Related Documents

| | |
|---|---|
| • Digital Voice Interface Application Note | 80000NT10050A |
| • SPI Port Application Note | 80000NT10053A |
| • SIM Holder Design Guides | 80000NT10001a |
| • USB HSIC Port Application Note | 80000NT10071A |
| • AT Commands Reference Guide | 80378ST10091A |
| • Telit EVK2 User Guide | 1vv0300704 |

# 2 OVERVIEW

The aim of this document is the description of some hardware solutions useful for developing a product with the Telit UE910-EU module.
In this document all the basic functions of a mobile phone will be taken into account; for each one of them a proper hardware solution will be suggested and eventually the wrong solutions and common errors to be avoided will be evidenced. Obviously this document cannot embrace the whole hardware solutions and products that may be designed. The wrong solutions to be avoided shall be considered as mandatory, while the suggested hardware configurations shall not be considered mandatory, instead the information given shall be used as a guide and a starting point for properly developing your product with the Telit UE910 module. For further hardware details that may not be explained in this document refer to the Telit UE910 Product Description document where all the hardware information is reported.

**NOTICE:**

(EN) The integration of the GSM/GPRS/WCDMA UE910 cellular module within user application shall be done according to the design rules described in this manual.

(IT) L'integrazione del modulo cellulare GSM/GPRS/WCDMA **UE910** all'interno dell'applicazione dell'utente dovrà rispettare le indicazioni progettuali descritte in questo manuale.

(DE) Die Integration des **UE910** GSM/GPRS/WCDMA Mobilfunk-Moduls in ein Gerät muß gemäß der in diesem Dokument beschriebenen Kunstruktionsregeln erfolgen.

(SL) Integracija GSM/GPRS/WCDMA **UE910** modula v uporabniški aplikaciji bo morala upoštevati projektna navodila, opisana v tem priročniku.

(SP) La utilización del modulo GSM/GPRS/WCDMA **UE910** debe ser conforme a los usos para los cuales ha sido deseñado descritos en este manual del usuario.

(FR) L'intégration du module cellulaire GSM/GPRS/WCDMA **UE910** dans l'application de l'utilisateur sera faite selon les règles de conception décrites dans ce manuel.

(HE) האינטגרטור מתבקש ליישם את ההנחיות המפורטות במסמך זה בתהליך האינטגרציה של המודם הסלולרי UE910 עם המוצר.

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# 3 PINS ALLOCATION

## 3.1 Pin-out

| Pin | Signal | I/O | Function | Type | Comment |
|---|---|---|---|---|---|
| **USB HS 2.0 COMMUNICATION PORT** | | | | | |
| **B15** | **USB_D+** | **I/O** | **USB differential Data (+)** | - | |
| **C15** | **USB_D-** | **I/O** | **USB differential Data (-)** | - | |
| **A13** | **VUSB** | **I** | **Power sense for the internal USB transceiver.** | - | |
| **Asynchronous Serial Port (USIF0) - Prog. / Data + HW Flow Control** | | | | | |
| **N15** | C103/TXD | I | Serial data input from DTE | CMOS 1.8V | |
| **M15** | C104/RXD | O | Serial data output to DTE | CMOS 1.8V | |
| **M14** | C108/DTR | I | Input for (DTR) from DTE | CMOS 1.8V | |
| **L14** | C105/RTS | I | Input for Request to send signal (RTS) from DTE | CMOS 1.8V | |
| **P15** | C106/CTS | O | Output for Clear to Send signal (CTS) to DTE | CMOS 1.8V | |
| **N14** | C109/DCD | O | Output for (DCD) to DTE | CMOS 1.8V | |
| **P14** | C107/DSR | O | Output for (DSR) to DTE | CMOS 1.8V | |
| **R14** | C125/RING | O | Output for Ring (RI) to DTE | CMOS 1.8V | |
| **Asynchronous Auxiliary Serial Port (USIF1)** | | | | | |
| **D15** | TX_AUX | O | Auxiliary UART (TX Data to DTE) | CMOS 1.8V | |
| **E15** | RX_AUX | I | Auxiliary UART (RX Data from DTE) | CMOS 1.8V | |
| **USB HSIC** | | | | | |
| **A12** | HSIC_USB_DATA | I/O | USB HSIC data signal | CMOS 1.2V | |
| **A11** | HSIC_USB_STRB | I/O | USB HSIC strobe signal | CMOS 1.2V | |
| **H15** | HSIC_SLAVE_WAKEUP | I | Slave Wake Up | CMOS 1.8V | Shared with SPI_MRDY |
| **F15** | HSIC_HOST_WAKEUP | O | Host Wake Up | CMOS 1.8V | Shared with SPI CLK |
| **K15** | HSIC_SUSPEND_REQUEST | O | Slave Suspend Request | CMOS 1.8V | Shared with GPIO08 |
| **J15** | HSIC_HOST_ACTIVE | I | Active Host Indication | CMOS 1.8V | Shared with SPI_SRDY |
| **SIM card interface** | | | | | |

| | | | | | |
|---|---|---|---|---|---|
| **A6** | SIMCLK | O | External SIM signal – Clock | 1.8 / 3V | |
| **A7** | SIMRST | O | External SIM signal – Reset | 1.8 / 3V | |
| **A5** | SIMIO | I/O | External SIM signal – Data I/O | 1.8 / 3V | |
| **A4** | SIMIN | I | External SIM signal – Presence (active low) | CMOS 1.8 | |
| **A3** | SIMVCC | - | External SIM signal – Power supply for the SIM | 1.8 / 3V | |
| **Digital Voice Interface (DVI)** | | | | | |
| **B9** | DVI_WA0 | I/O | Digital Audio Interface (WA0) | CMOS 1.8V | |
| **B6** | DVI_RX | I/O | Digital Audio Interface (RX) | CMOS 1.8V | |
| **B7** | DVI_TX | I/O | Digital Audio Interface (TX) | CMOS 1.8V | |
| **B8** | DVI_CLK | I/O | Digital Audio Interface (CLK) | CMOS 1.8V | |
| **SPI** | | | | | |
| **D15** | SPI_MOSI | I | SPI MOSI | CMOS 1.8V | Shared with TX_AUX |
| **E15** | SPI_MISO | O | SPI_MISO | CMOS 1.8V | Shared with RX_AUX |
| **F15** | SPI_CLK | I | SPI Clock | CMOS 1.8V | |
| **H15** | SPI_MRDY | I | SPI_MRDY | CMOS 1.8V | |
| **J15** | SPI_SRDY | O | SPI_SRDY | CMOS 1.8V | |
| **DIGITAL IO** | | | | | |
| **C8** | GPIO_01 | I/O | GPIO_01 /STAT LED | CMOS 1.8V | Alternate Function STAT LED |
| **C9** | GPIO_02 | I/O | GPIO_02 | CMOS 1.8V | |
| **C10** | GPIO_03 | I/O | GPIO_03 | CMOS 1.8V | |
| **C11** | GPIO_04 | I/O | GPIO_04 | CMOS 1.8V | |
| **B14** | GPIO_05 | I/O | GPIO_05 | CMOS 1.8V | |
| **C12** | GPIO_06 | I/O | GPIO_06 | CMOS 1.8V | |
| **C13** | GPIO_07 | I/O | GPIO_07 | CMOS 1.8V | |

| | | | | | |
|---|---|---|---|---|---|
| **K15** | GPIO_08 | I/O | GPIO_08 | CMOS 1.8V | |
| **L15** | GPIO_09 | I/O | GPIO_09 | CMOS 1.8V | |
| **G15** | GPIO_10 | I/O | GPIO_10 | CMOS 1.8V | |
| **ADC** | | | | | |
| **B1** | ADC_IN1 | AI | Analog / Digital converter input | A/D | Accepted values 0 to 1.2V DC |
| **RF SECTION** | | | | | |
| **K1** | ANTENNA | I/O | WCDMA Antenna (50 ohm) | RF | |
| **Miscellaneous Functions** | | | | | |
| **R13** | HW_SHUTDOWN* | I | HW Unconditional Shutdown | CMOS 1.8V | Active low |
| **R12** | ON_OFF* | I | Input command for power ON | CMOS 1.8V | Active low |
| **C14** | VRTC | I | VRTC Backup capacitor | Power | backup for the embedded RTC supply |
| **R11** | VAUX/PWRMON | O | Supply Output for external accessories / Power ON Monitor | 1.8V | |
| **Power Supply** | | | | | |
| **M1** | VBATT | - | Main power supply (Baseband) | Power | |
| **M2** | VBATT | - | Main power supply (Baseband) | Power | |
| **N1** | VBATT_PA | - | Main power supply (Radio PA) | Power | |
| **N2** | VBATT_PA | - | Main power supply (Radio PA) | Power | |
| **P1** | VBATT_PA | - | Main power supply (Radio PA) | Power | |
| **P2** | VBATT_PA | - | Main power supply (Radio PA) | Power | |
| **E1** | GND | - | Ground | Power | |
| **G1** | GND | - | Ground | Power | |
| **H1** | GND | - | Ground | Power | |
| **J1** | GND | - | Ground | Power | |

| | | | | |
|---|---|---|---|---|
| **L1** | GND | - | Ground | Power |
| **A2** | GND | - | Ground | Power |
| **E2** | GND | - | Ground | Power |
| **F2** | GND | - | Ground | Power |
| **G2** | GND | - | Ground | Power |
| **H2** | GND | - | Ground | Power |
| **J2** | GND | - | Ground | Power |
| **K2** | GND | - | Ground | Power |
| **L2** | GND | - | Ground | Power |
| **R2** | GND | - | Ground | Power |
| **M3** | GND | - | Ground | Power |
| **N3** | GND | - | Ground | Power |
| **P3** | GND | - | Ground | Power |
| **R3** | GND | - | Ground | Power |
| **D4** | GND | - | Ground | Power |
| **M4** | GND | - | Ground | Power |
| **N4** | GND | - | Ground | Power |
| **P4** | GND | - | Ground | Power |
| **R4** | GND | - | Ground | Power |
| **N5** | GND | - | Ground | Power |
| **P5** | GND | - | Ground | Power |
| **R5** | GND | - | Ground | Power |
| **N6** | GND | - | Ground | Power |
| **P6** | GND | - | Ground | Power |
| **R6** | GND | - | Ground | Power |
| **P8** | GND | - | Ground | Power |
| **R8** | GND | - | Ground | Power |

| | | | | |
|---|---|---|---|---|
| **P9** | GND | - | Ground | Power |
| **P10** | GND | - | Ground | Power |
| **R10** | GND | - | Ground | Power |
| **M12** | GND | - | Ground | Power |
| **B13** | GND | - | Ground | Power |
| **P13** | GND | - | Ground | Power |
| **E14** | GND | - | Ground | Power |
| **RESERVED** | | | | |
| **C1** | RESERVED | - | RESERVED | |
| **D1** | RESERVED | - | RESERVED | |
| **B2** | RESERVED | - | RESERVED | |
| **C2** | RESERVED | - | RESERVED | |
| **D2** | RESERVED | - | RESERVED | |
| **B3** | RESERVED | - | RESERVED | |
| **C3** | RESERVED | - | RESERVED | |
| **D3** | RESERVED | - | RESERVED | |
| **E3** | RESERVED | - | RESERVED | |
| **F3** | RESERVED | - | RESERVED | |
| **G3** | RESERVED | - | RESERVED | |
| **H3** | RESERVED | - | RESERVED | |
| **J3** | RESERVED | - | RESERVED | |
| **K3** | RESERVED | - | RESERVED | |
| **L3** | RESERVED | - | RESERVED | |
| **B4** | RESERVED | - | RESERVED | |
| **C4** | RESERVED | - | RESERVED | |
| **B5** | RESERVED | - | RESERVED | |
| **C5** | RESERVED | - | RESERVED | |

| | | | |
|---|---|---|---|
| **C6** | RESERVED | - | RESERVED |
| **C7** | RESERVED | - | RESERVED |
| **N7** | RESERVED | - | RESERVED |
| **P7** | RESERVED | - | RESERVED |
| **N8** | RESERVED | - | RESERVED |
| **N9** | RESERVED | - | RESERVED |
| **A10** | RESERVED | - | RESERVED |
| **N10** | RESERVED | - | RESERVED |
| **N11** | RESERVED | - | RESERVED |
| **B12** | RESERVED | - | RESERVED |
| **D12** | RESERVED | - | RESERVED |
| **N12** | RESERVED | - | RESERVED |
| **P12** | RESERVED | - | RESERVED |
| **F14** | RESERVED | - | RESERVED |
| **G14** | RESERVED | - | RESERVED |
| **H14** | RESERVED | - | RESERVED |
| **J14** | RESERVED | - | RESERVED |
| **K14** | RESERVED | - | RESERVED |
| **N13** | RESERVED | - | RESERVED |
| **L13** | RESERVED | - | RESERVED |
| **J13** | RESERVED | - | RESERVED |
| **M13** | RESERVED | - | RESERVED |
| **K13** | RESERVED | - | RESERVED |
| **H13** | RESERVED | - | RESERVED |
| **G13** | RESERVED | - | RESERVED |
| **F13** | RESERVED | - | RESERVED |
| **B1** | RESERVED | - | RESERVED |

| | | | |
|---|---|---|---|
| **B11** | RESERVED | - | RESERVED |
| **B10** | RESERVED | - | RESERVED |
| **A9** | RESERVED | - | RESERVED |
| **A8** | RESERVED | - | RESERVED |
| **D14** | RESERVED | - | RESERVED |
| **A14** | RESERVED | - | RESERVED |
| **D13** | RESERVED | - | RESERVED |
| **E13** | RESERVED | - | RESERVED |
| **F1** | RESERVED | - | RESERVED |
| **R9** | RESERVED | - | RESERVED |
| **R7** | RESERVED | - | RESERVED |
| **P11** | RESERVED | - | RESERVED |

WARNING:

Reserved pins must not be connected

If not used, almost all pins should be left disconnected. The only exceptions are the following pins:

| PAD | Signal | Note |
|---|---|---|
| M1,M2,N1,N2,P1,P2 | VBATT & VBATT_PA | |
| E1, G1, H1, J1, L1, A2, E2, F2, G2, H2 J2,K2,L2,R2,M3,N3,P3,R3,D4,M4, N4,P4,R4,N5,P5,R5,N6,P6,R6,P8, R8,P9,P10,R10,M12,B13,P13,E14 | GND | |
| R12 | ON/OFF* | |
| R13 | HW_SHUTDOWN* | |
| B15 | USB_D+ | If not used should be connected to a Test Point or an USB connector |
| C15 | USB_D- | If not used should be connected to a Test Point or an USB connector |
| A13 | VUSB | If not used should be connected to a Test Point or an USB connector |
| N15 | C103/TXD | If not used should be connected to a Test Point |
| M15 | C104/RXD | If not used should be connected to a Test Point |
| L14 | C105/RTS | If the flow control is not used it should be connected to GND |
| P15 | C106/CTS | If not used should be connected to a Test Point |
| D15 | TXD_AUX | If not used should be connected to a Test Point |
| E15 | RXD_AUX | If not used should be connected to a Test Point |
| K1 | MAIN ANTENNA | |
| A6 | SIMCLK | |
| A7 | SIMRST | |
| A5 | SIMIO | |
| A4 | SIMIN | |

RTS pin should be connected to the GND (on the module side) if flow control is not used.

The above pins are also necessary to debug the application when the module is assembled on it so we recommend connecting them also to dedicated test point.

### 3.1.1 LGA Pads Layout

**TOP VIEW**

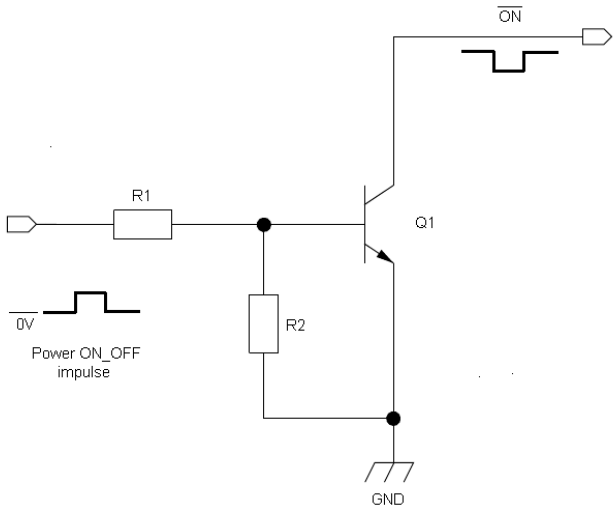
| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | | ADC_IN1 | RES | RES | GND | RES | GND | GND | GND | ANT | GND | VBATT | VBATT_PA | VBATT_PA | |
| 2 | GND | RES | RES | RES | GND | GND | GND | GND | GND | GND | GND | VBATT | VBATT_PA | VBATT_PA | GND |
| 3 | SIMVCC | RES | RES | RES | RES | RES | RES | RES | RES | RES | RES | GND | GND | GND | GND |
| 4 | SIMIN | RES | RES | GND | | | | | | | | GND | GND | GND | GND |
| 5 | SIMIO | RES | RES | | | | | | | | | | GND | GND | GND |
| 6 | SIMCLK | DVI_RX | RES | | | | | | | | | | GND | GND | GND |
| 7 | SIMRST | DVI_TX | RES | | | | | | | | | | RES | RES | RES |
| 8 | RES | DVI_CLK | GPIO_01 | | | | | | | | | | RES | GND | GND |
| 9 | RES | DVI_WA0 | GPIO_02 | | | | | | | | | | RES | GND | RES |
| 10 | RES | RES | GPIO_03 | | | | | | | | | | RES | GND | GND |
| 11 | HSIC_USB_STRB | RES | GPIO_04 | | | | | | | | | | RES | RES | VAUX/PWRMON |
| 12 | HSIC_USB_DATA | RES | GPIO_06 | RES | | | | | | | | GND | RES | RES | ON_OFF* |
| 13 | VUSB | GND | GPIO_07 | RES | RES | RES | RES | RES | RES | RES | RES | RES | RES | GND | HW_SHUTDOWN* |
| 14 | RES | GPIO_05 | VRTC | RES | GND | RES | RES | RES | RES | RES | C105/RTS | C108/DTR | C109/DCD | C107/DSR | C125/RING |
| 15 | | USB_D+ | USB_D- | TX AUX | RX AUX | SPI_CLK | GPIO_10 | SPI_MRDY | SPI_SRDY | GPIO_08 | GPIO_09 | C104/RXD | C103/TXD | C106/CTS | |

# 4 HARDWARE COMMANDS

## 4.1 Turning ON the UE910

To turn on the UE910 the pad ON_OFF* must be tied low for at least 5 seconds and then released.

The maximum current that can be drained from the ON_OFF* pad is 0,1 mA.




**NOTE:**

Don't use any pull up resistor on the ON_OFF* line, it is internally pulled up. Using pull up resistor may bring to latch up problems on the UE910 power regulator and improper power on/off of the module. The line ON_OFF* must be connected only in open collector or open drain configuration.

**NOTE:**

In this document all the lines that are inverted, hence have active low signals are labelled with a name that ends with"#","*" or with a bar over the name.

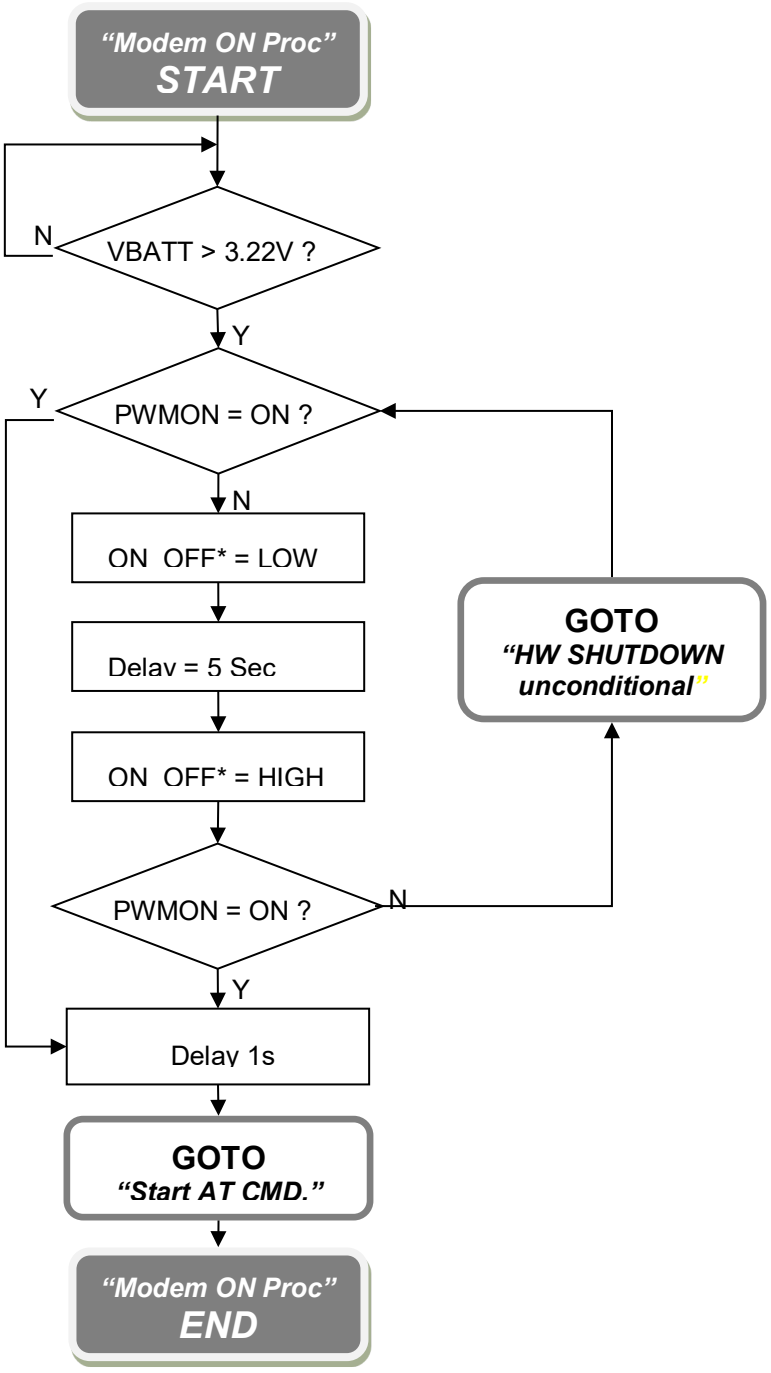
**TIP:**

To check if the device has powered on, the hardware line PWRMON should be monitored.

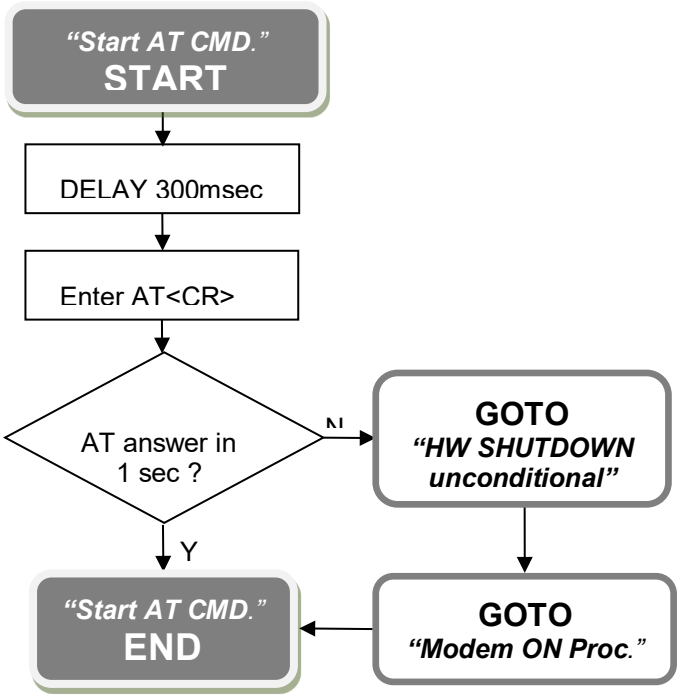
**NOTE:**

It is mandatory to avoid sending data to the serial ports during the first 200ms of the module start-up.

A flow chart showing the proper turn on procedure is displayed below:



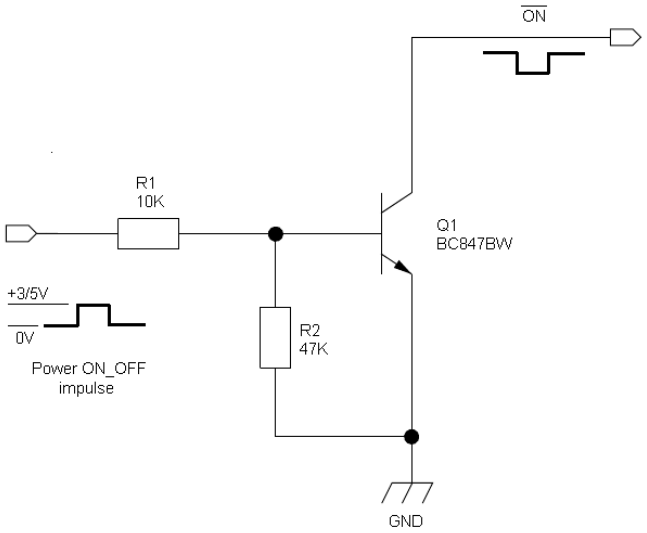
A flow chart showing the AT commands managing procedure is displayed below:



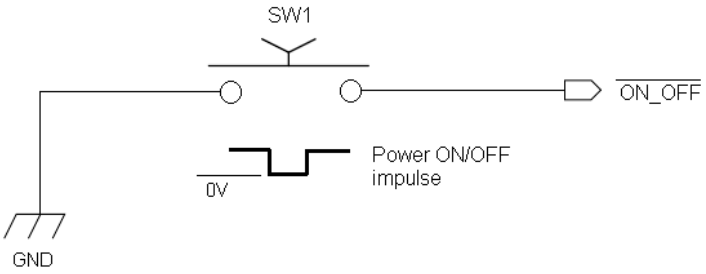

**NOTE:**

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the UE910 when the module is powered off or during an ON/OFF transition.

For example:
1- Let's assume you need to drive the ON_OFF* pad with a totem pole output of a +3/5 V microcontroller (uP_OUT1):

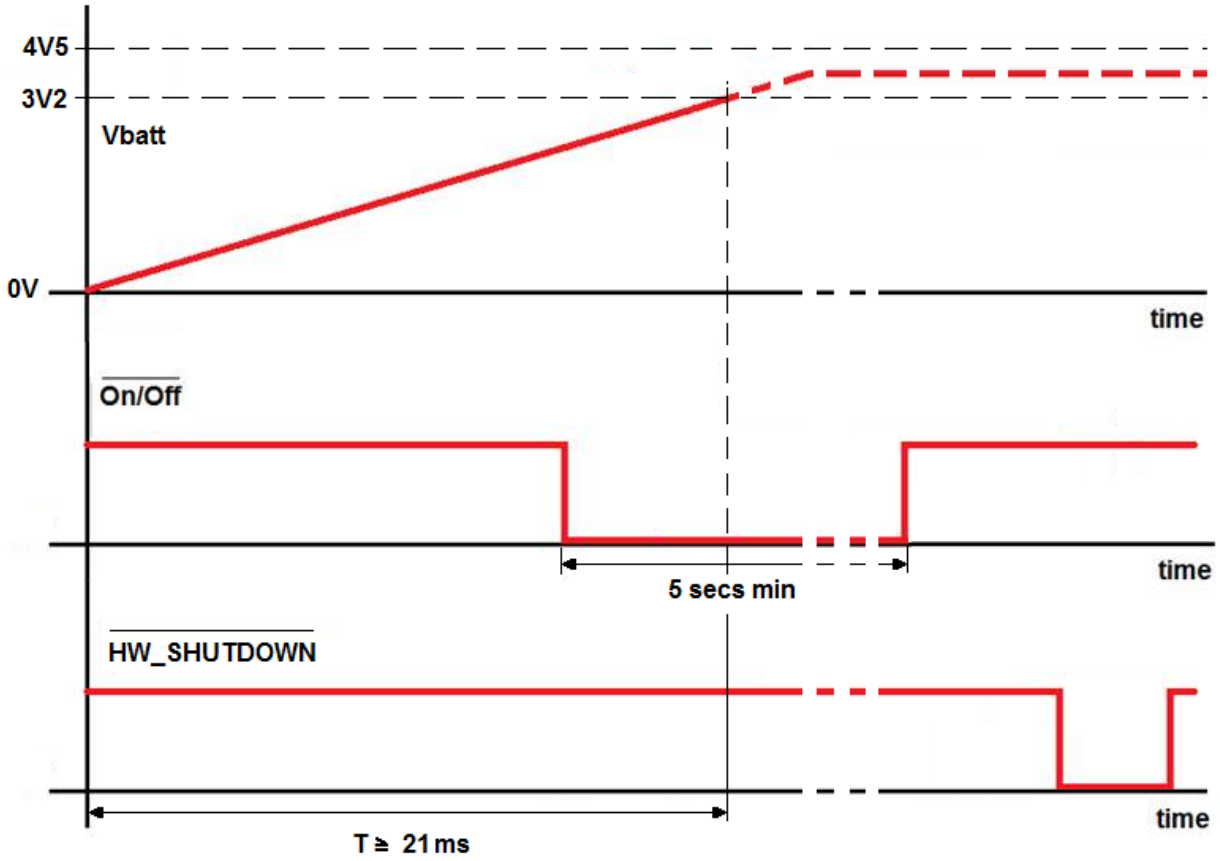



2- Let's assume you need to drive the ON_OFF* pad directly with an ON/OFF button:




**WARNING**
It is recommended to set the ON_OFF* line LOW to power on the module only after VBATT is higher than 3.22V.
In case this condition it is not satisfied you could use the HW_SHUTDOWN* line to recover it and then restart the power on activity using the ON_OFF * line.

An example of this is described in the following diagram:




After HW_SHUTSDOWN* is released you could again use the ON_OFF* line to power on the module.

## 4.2 Turning OFF the UE910

Turning off of the device can be done in two ways:

- via AT command (see UE910 Software User Guide, AT#SHDN)
- by tying low pin ON_OFF*

Either ways, the device issues a detach request to network informing that the device will not be reachable any more.
To turn OFF the UE910 the pad ON_OFF* must be tied low for at least 3 seconds and then released.

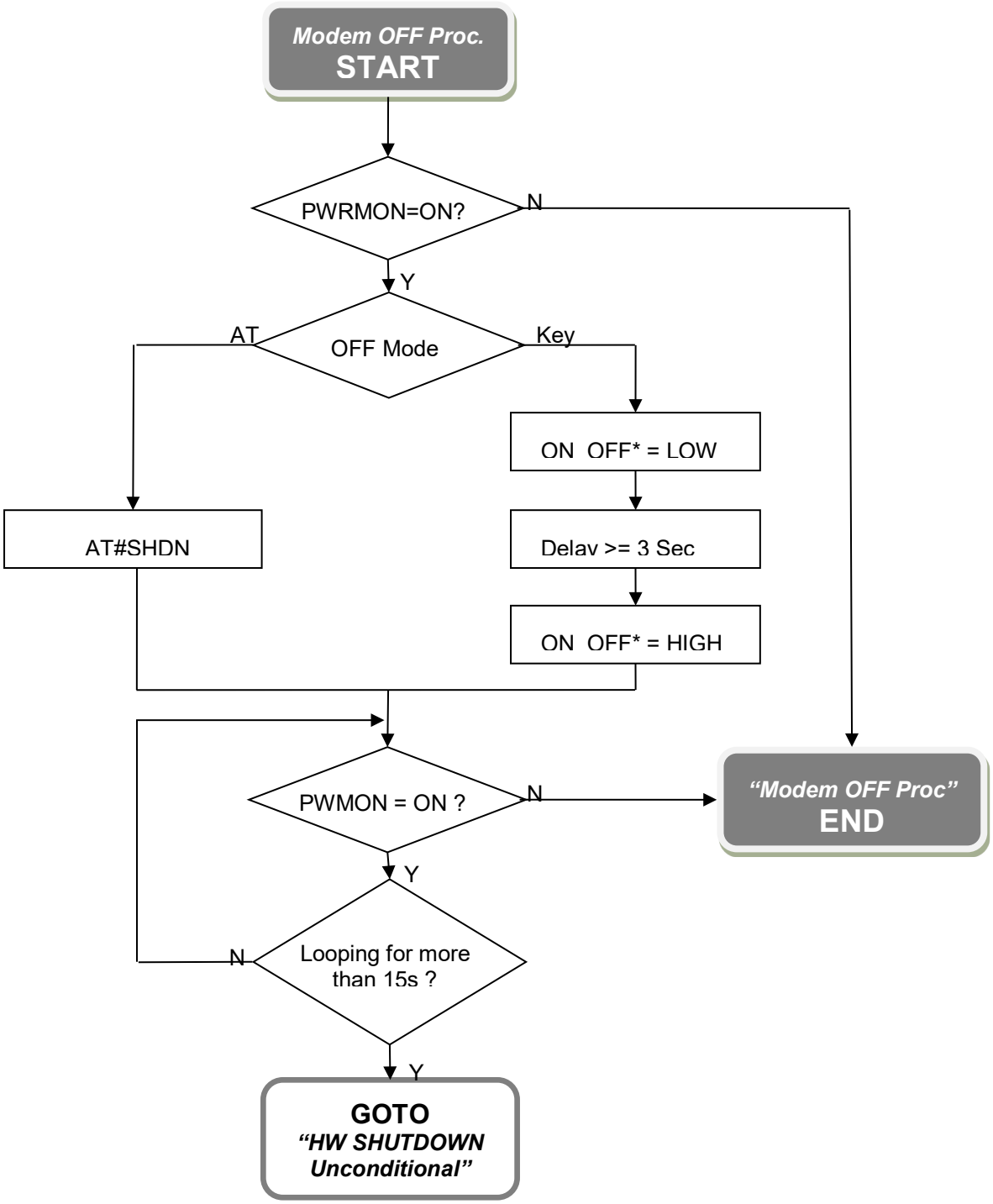
**TIP:**

To check if the device has been powered off, the hardware line PWRMON must be monitored. The device is powered off when PWRMON goes low.

**NOTE:**

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the UE910 when the module is powered off or during an ON/OFF transition.

The following flow chart shows the proper turn off procedure:



## 4.3 UE910 Unconditional Shutdown

The Unconditional Shutdown of the module could be activated using the HW_SHUTDOWN* line (pad R13).

**WARNING:**

The hardware unconditional Shutdown must not be used during normal operation of the device since it does not detach the device from the network. It shall be kept as an emergency exit procedure.

To unconditionally shutdown the UE910, the pad HW_SHUTDOWN* must be tied low for at least 200 milliseconds and then released.

**NOTE:**

Do not use any pull up resistor on the HW_SHUTDOWN* line nor any totem pole digital output. Using pull up resistor may bring to latch up problems on the UE910 power regulator and improper functioning of the module. The line HW_SHUTDOWN* must be connected only in open collector configuration.

The HW_SHUTDOWN* is generating an unconditional shutdown of the module without an automatic restart.

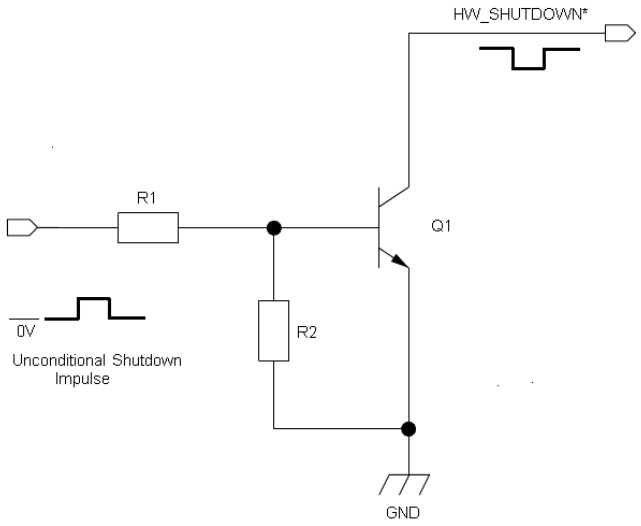
The module will shutdown, but will NOT perform the detach from the cellular network.

To proper power on again the module please refer to the related paragraph (“Powering ON the UE910”)

**TIP:**

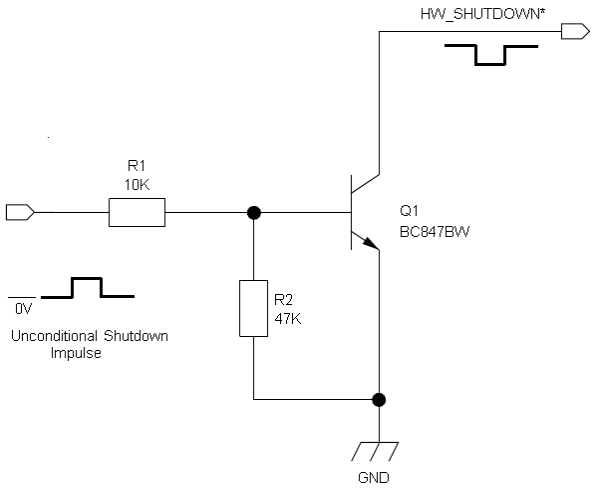
The unconditional hardware shutdown must always be implemented on the boards and should be used only as an emergency exit procedure.

A typical circuit is the following:




For example:

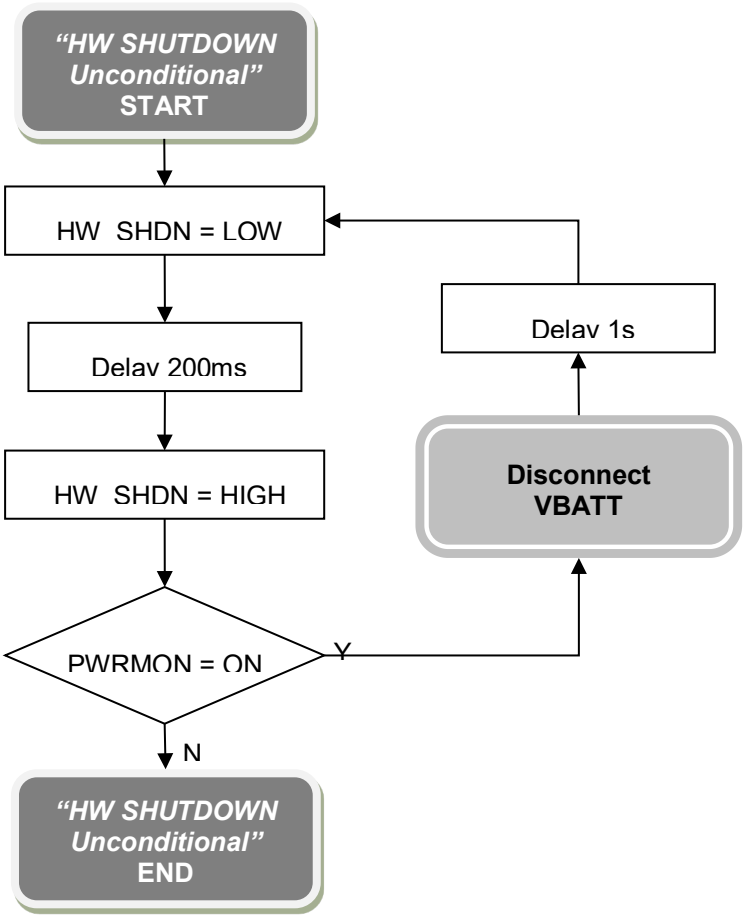
1- Let us assume you need to drive the HW_SHUTDOWN* pad with a totem pole output of a +3/5 V microcontroller (uP_OUT2):




**NOTE:**

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the UE910 when the module is powered off or during an ON/OFF transition.

In the following flow chart is detailed the proper restart procedure:



# 5 POWER SUPPLY

The power supply circuitry and board layout are a very important part in the full product design and they strongly reflect on the product overall performances, hence read carefully the requirements and the guidelines that will follow for a proper design.

## 5.1 Power Supply Requirements

The external power supply must be connected to VBATT & VBATT_PA signals and must fulfil the following requirements:

| Power Supply | Value |
|---|---|
| Nominal Supply Voltage | 3.8V |
| Normal Operating Voltage Range | 3.40 V÷ 4.20 V |
| Extended Operating Voltage Range | 3.10 V÷ 4.50 V |

NOTE:
The Operating Voltage Range MUST never be exceeded; care must be taken when designing the application's power supply section to avoid having an excessive voltage drop.
If the voltage drop is exceeding the limits it could cause a Power Off of the module.
The Power supply must be higher than 3.22 V to power on the module

Overshoot voltage (regarding MAX Extended Operating Voltage) and drop in voltage (regarding MIN Extended Operating Voltage) MUST never be exceeded;
The "Extended Operating Voltage Range" can be used only with completely assumption and application of the HW User guide suggestions.

## 5.2 Power Consumption

| Mode | Average (mA) | Mode description |
|---|---|---|
| **SWITCHED OFF** | | Module supplied but Switched Off |
| Switched Off | 180 uA | |
| | **IDLE mode (WCDMA)** | |
| AT+CFUN=1 | 12.2 | Normal mode: full functionality of the module |
| AT+CFUN=5 | 1.6 | Full functionality with power saving; DRX7; Module registered on the network can receive incoming calls and SMS |
| | **IDLE mode (GSM/EDGE)** | |
| AT+CFUN=1 | 19 | Normal mode: full functionality of the module |
| AT+CFUN=4 | 16.5 | Module is not registered on the network |
| AT+CFUN=5 | 1.2 | Full functionality with power saving; DRX9 (1.3mA in case of DRX5). |
| | **Operative mode (WCDMA)** | |
| WCDMA Voice | 170 | WCDMA voice call (TX = 10dBm) |
| WCDMA HSDPA (0dBm) | 187 | WCDMA data call (Cat 8, TX = 0dBm) |
| WCDMA HSDPA (22dBm) | 538 | WCDMA data call (Cat 8, TX = 22dBm) |
| | **Operative mode (GSM)** | |
| **CSD TX and RX mode** | | GSM VOICE CALL |
| GSM 850/900 CSD PL5 | 220 | |
| DCS1800/ PCS1900 CSD PL0 | 167 | |
| **GPRS 4TX+1RX** | | GPRS Sending data mode |
| GSM 850/900 PL5 | 580 | |
| DCS1800/ PCS1900 PL0 | 438 | |

NOTE:
The electrical design for the Power supply should be made ensuring it will be capable of a peak current output of at least 2 A.

The GSM system is made in a way that the RF transmission is not continuous, else it is packed into bursts at a base frequency of about 216 Hz, and the relative current peaks can be as high as about 2A. Therefore the power supply has to be designed in order to withstand with these current peaks without big voltage drops; this means that both the electrical design and the board layout must be designed for this current flow. If the layout of the PCB is not well designed a strong noise floor is generated on the ground and the supply; this will reflect on all the audio paths producing an audible annoying noise at 216 Hz; if the voltage drop during the peak current absorption is too much, then the device may even shutdown as a consequence of the supply voltage drop.

# 5.3 General Design Rules

The principal guidelines for the Power Supply Design embrace three different design steps:

- the electrical design
- the thermal design
- the PCB layout.

## 5.3.1 Electrical Design Guidelines

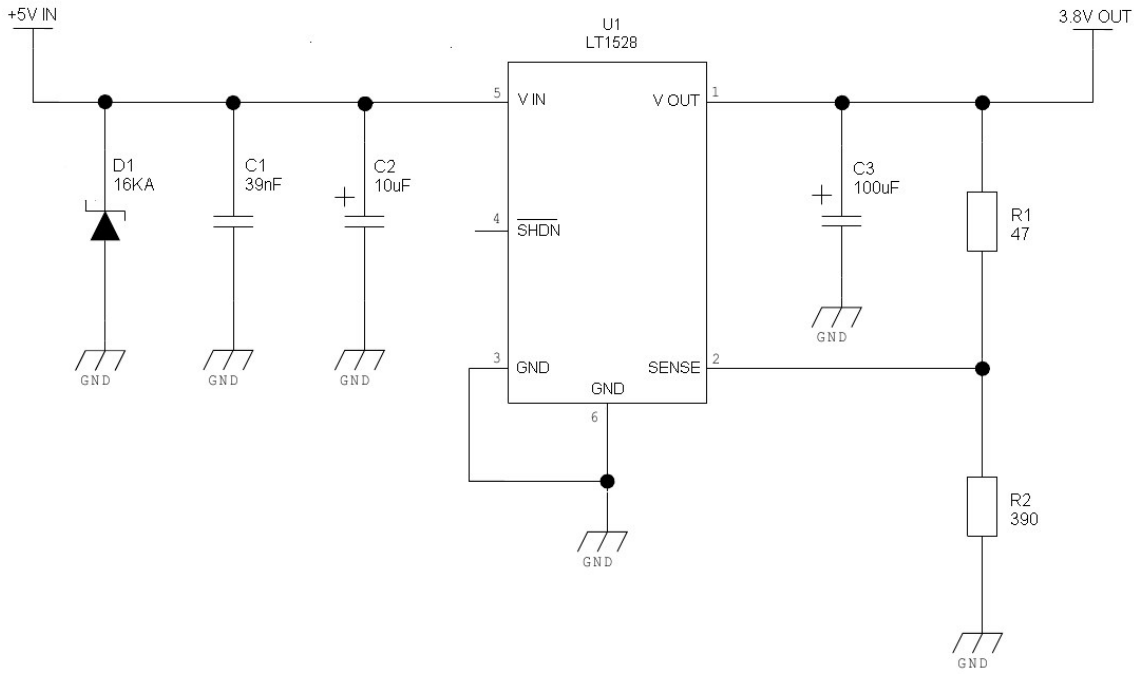
The electrical design of the power supply depends strongly from the power source where this power is drained. We will distinguish them into three categories:

- +5V input (typically PC internal regulator output)
- +12V input (typically automotive)
- Battery

### 5.3.1.1 *+5V Source Power Supply Design Guidelines*

- The desired output for the power supply is 3.8V, hence there's not a big difference between the input source and the desired output and a linear regulator can be used. A switching power supply will not be suited because of the low drop out requirements.
- When using a linear regulator, a proper heat sink shall be provided in order to dissipate the power generated.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks close to the Module, a 100µF capacitor is usually suited.
- Make sure the low ESR capacitor on the power supply output rated at least 10V.
- A protection diode should be inserted close to the power input, in order to save the UE910 from power polarity inversion.

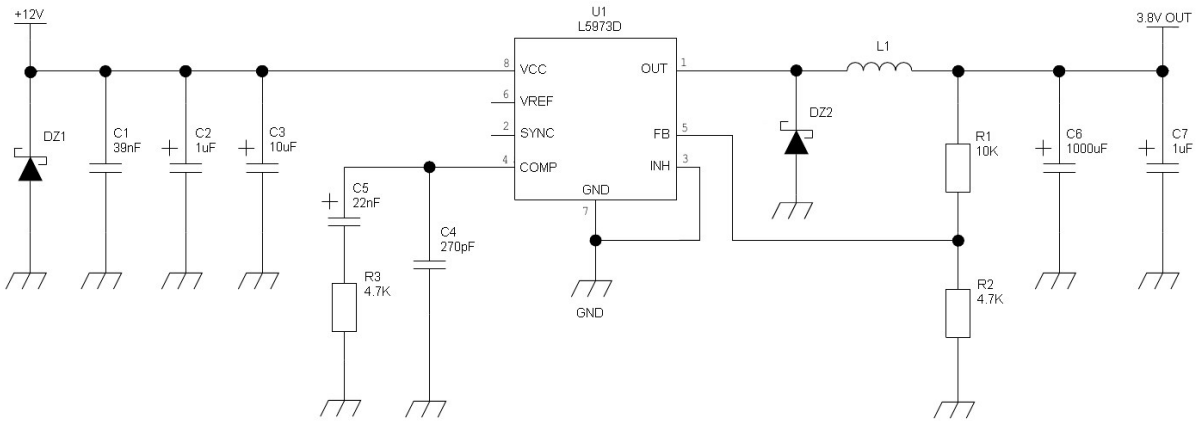
An example of linear regulator with 5V input is:



### 5.3.1.2 *+ 12V input Source Power Supply Design Guidelines*

- The desired output for the power supply is 3.8V, hence due to the big difference between the input source and the desired output, a linear regulator is not suited and shall not be used. A switching power supply will be preferable because of its better efficiency.
- When using a switching regulator, a 500kHz or more switching frequency regulator is preferable because of its smaller inductor size and its faster transient response. This allows the regulator to respond quickly to the current peaks absorption.
- In any case the frequency and Switching design selection is related to the application to be developed due to the fact the switching frequency could also generate EMC interferences.
- For car PB battery the input voltage can rise up to 15,8V and this should be kept in mind when choosing components: all components in the power supply must withstand this voltage.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100µF capacitor is usually suited.
- Make sure the low ESR capacitor on the power supply output is rated at least 10V.
- For Car applications a spike protection diode should be inserted close to the power input, in order to clean the supply from spikes.
- A protection diode should be inserted close to the power input, in order to save the UE910 from power polarity inversion. This can be the same diode as for spike protection.

An example of switching regulator with 12V input is in the below schematic:



#### 5.3.1.3 *Battery Source Power Supply Design Guidelines*

The desired nominal output for the power supply is 3.8V and the maximum voltage allowed is 4.2V, hence a single 3.7V Li-Ion cell battery type is suited for supplying the power to the Telit UE910 module.

- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100µF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor (usually a tantalum one) is rated at least 10V.
- A protection diode should be inserted close to the power input, in order to save the UE910 from power polarity inversion. Otherwise the battery connector should be done in a way to avoid polarity inversions when connecting the battery.
- The battery capacity must be at least 500mAh in order to withstand the current peaks of 2A; the suggested capacity is from 500mAh to 1000mAh.

WARNING:

The three cells Ni/Cd or Ni/MH 3,6 V Nom. battery types or 4V PB types *MUST NOT BE USED DIRECTLY* since their maximum voltage can rise over the absolute maximum voltage for the UE910 and damage it.

NOTE:

DON'T USE any Ni-Cd, Ni-MH, and Pb battery types directly connected with UE910. Their use can lead to overvoltage on the UE910 and damage it. USE ONLY Li-Ion battery types.

#### 5.3.1.4 *Thermal Design Guidelines*

The thermal design for the power supply heat sink should be done with the following specifications:

- Average current consumption during HSDPA transmission @PWR level max : 700 mA
- *Average current during idle:* 1.8 *mA*

Considering the very low current during idle, especially if Power Saving function is enabled, it is possible to consider from the thermal point of view that the device absorbs current significantly only during calls.

If we assume that the device stays into transmission for short periods of time (let's say few minutes) and then remains for a quite long time in idle (let's say one hour), then the power supply has always the time to cool down between the calls and the heat sink could be smaller than the calculated one for 700mA maximum RMS current, or even could be the simple chip package (no heat sink).
Moreover in the average network conditions the device is requested to transmit at a lower power level than the maximum and hence the current consumption will be less than the 700mA, being usually around 150mA.

For these reasons the thermal design is rarely a concern and the simple ground plane where the power supply chip is placed can be enough to ensure a good thermal condition and avoid overheating. The generated heat will be mostly conducted to the ground plane under the UE910; you must ensure that your application can dissipate it.
For the heat generated by the UE910-EU, you can consider it to be during transmission 1W max during CSD/VOICE calls and 2W max during class12 GPRS upload.
This generated heat will be mostly conducted to the ground plane under the UE910-EU; you must ensure that your application can dissipate it.

NOTE:

The average consumption during transmissions depends on the power level at which the device is requested to transmit by the network. The average current consumption hence varies significantly.

### 5.3.1.5 *Power Supply PCB layout Guidelines*

As seen on the electrical design guidelines the power supply shall have a low ESR capacitor on the output to cut the current peaks on the input to protect the supply from spikes The placement of this component is crucial for the correct working of the circuitry. A misplaced component can be useless or can even decrease the power supply performances.

- The Bypass low ESR capacitor must be placed close to the Telit UE910 power input pads or in the case the power supply is a switching type it can be placed close to the inductor to cut the ripple provided the PCB trace from the capacitor to the UE910 is wide enough to ensure a dropless connection even during an 1A current peak.

- The protection diode must be placed close to the input connector where the power source is drained.

- The PCB traces from the input connector to the power regulator IC must be wide enough to ensure no voltage drops occur when an 1A current peak is absorbed.

- The PCB traces to the UE910-EU and the Bypass capacitor must be wide enough to ensure no significant voltage drops occur. This is for the same reason as previous point. Try to keep this trace as short as possible.

- To reduce the EMI due to switching, it is important to keep very small the mesh involved; thus the input capacitor, the output diode (if not embodied in the IC) and the regulator have to form a very small loop.This is done in order to reduce the radiated field (noise) at the switching frequency (100-500 kHz usually).

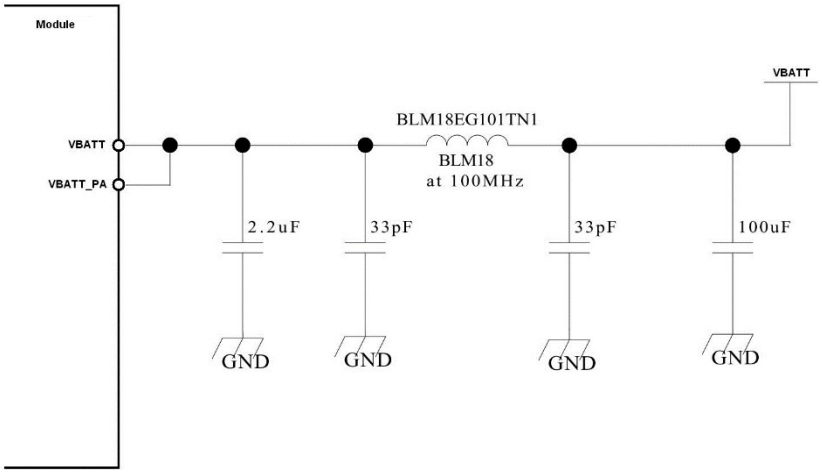
- A dedicated ground for the Switching regulator separated by the common ground plane is suggested.

- The placement of the power supply on the board should be done in such a way to guarantee that the high current return paths in the ground plane are not overlapped to any noise sensitive circuitry as the microphone amplifier/buffer or earphone amplifier.

- The power supply input cables should be kept separate from noise sensitive lines such as microphone/earphone cables.

- The insertion of EMI filter on VBATT pins is suggested in those designs where antenna is placed close to battery or supply lines.
  A ferrite bead like Murata BLM18EG101TN1 or Taiyo Yuden P/N FBMH1608HM101 can be used for this purpose.

The below figure shows the recommended circuit:



## 5.4 RTC Bypass out

The VRTC pin brings out the Real Time Clock supply, which is separate from the rest of the digital part, allowing having only RTC going on when all the other parts of the device are off.
To this power output a backup capacitor can be added in order to increase the RTC autonomy during power off of the battery. NO Devices must be powered from this pin.

In order to keep the RTC active when VBATT is not supplied it is possible to back up the RTC section connecting a **backup circuit** to the related VRTC signal (pad C14 on module's Pinout).

For additional details on the Backup solutions please refer to the related application note (xE910 RTC Backup Application Note).

## 5.5 VAUX Power Output

A regulated power supply output is provided in order to supply small devices from the module. The signal is present on Pad R11 and it is in common with the PWRMON (module powered ON indication) function.

This output is always active when the module is powered ON.

The operating range characteristics of the supply are:

| Item | Min | Typical | Max |
|---|---|---|---|
| Output voltage | 1.78V | 1.80V | 1.82V |
| Output current | - | - | 60mA |
| Output bypass capacitor (inside the module) | | 1uF | |

# 6 DIGITAL SECTION

## 6.1 Logic Levels Specification

**ABSOLUTE MAXIMUM RATINGS – NOT FUNCTIONAL:**

| Parameter | Min | Max |
|---|---|---|
| Input level on any digital pin (CMOS 1.8) with respect to ground | -0.3V | 2.1V |
| Input level on any digital pin (CMOS 1.2) with respect to ground | -0.3V | 1.4V |

**OPERATING RANGE - INTERFACE LEVELS (1.8V CMOS):**

| Parameter | Min | Max |
|---|---|---|
| Input high level | 1.5V | 1.9V |
| Input low level | 0V | 0.35V |
| Output high level | 1.6V | 1.9V |
| Output low level | 0V | 0.2V |

**OPERATING RANGE - INTERFACE LEVELS (1.2V CMOS):**

| Parameter | Min | Max |
|---|---|---|
| Input high level | 0.9V | 1.3V |
| Input low level | 0V | 0.3V |
| Output high level | 1V | 1.3V |
| Output low level | 0V | 0.1V |

## CURRENT CHARACTERISTICS:

| Parameter | AVG |
|---|---|
| Output Current | 1mA |
| Input Current | 1uA |

# 6.2 Communication ports

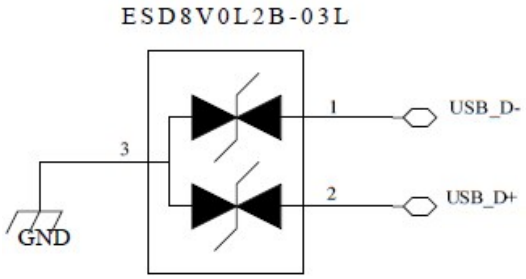
## 6.2.1 USB 2.0 HS

The UE910 includes one integrated universal serial bus (USB 2.0 HS) transceiver.
The following table is listing the available signals:

| PAD | Signal | I/O | Function | Type | NOTE |
|---|---|---|---|---|---|
| **B15** | USB_D+ | I/O | USB differential Data (+) | 3.3V | |
| **C15** | USB_D- | I/O | USB differential Data (-) | 3.3V | |
| **A13** | VUSB | AI | Power sense for the internal USB transceiver. | 5V | Accepted range: 4.4V to 5.25V |

The USB_DPLUS and USB_DMINUS signals have a clock rate of 480 MHz.
The signal traces should be routed carefully. Trace lengths, number of vias and capacitive loading should be minimized. The characteristic impedance value should be as close as possible to 90 Ohms differential.

In case there is a need to add an ESD protection, the suggested connection is the following:




NOTE:
VUSB pin should be disconnected before activating the Power Saving Mode.

### 6.2.2 USB HSIC

The UE910 Module is provided by one USB HSIC interface.
The USB HSIC (High Speed Inter Processor) Interface allows supporting the inter-processor communication between an application processor (AP) – the host, and the modem processor (CP) – the UE910.

The following table is listing the available signals:

| PAD | Signal | I/O | Function | Type | NOTE |
|---|---|---|---|---|---|
| **A12** | HSIC_USB_DATA | I/O | USB HSIC data signal | CMOS 1.2V | |
| **A11** | HSIC_USB_STRB | I/O | USB HSIC strobe signal | CMOS 1.2V | |
| **H15** | HSIC_SLAVE_WAKEUP | I | Slave Wake Up | CMOS 1.8V | Shared with SPI_MRDY |
| **F15** | HSIC_HOST_WAKEUP | O | Host Wake Up | CMOS 1.8V | Shared with SPI CLK |
| **K15** | HSIC_SUSPEND_REQUEST | O | Slave Suspend Request | CMOS 1.8V | Shared with GPIO08 |
| **J15** | HSIC_HOST_ACTIVE | I | Active Host Indication | CMOS 1.8V | Shared with SPI_SRDY |

For the detailed use of USB HSIC port please refer to the related Application Note.

NOTE:
Due to the shared functions, when the USB_HSIC port is used, it is not possible to use the SPI and GPIO_08.

The USB_HSIC is not active by default but it has to be enabled using the AT#PORTCFG command (refer to the AT user guide for the detailed syntax description).

### 6.2.3 SPI

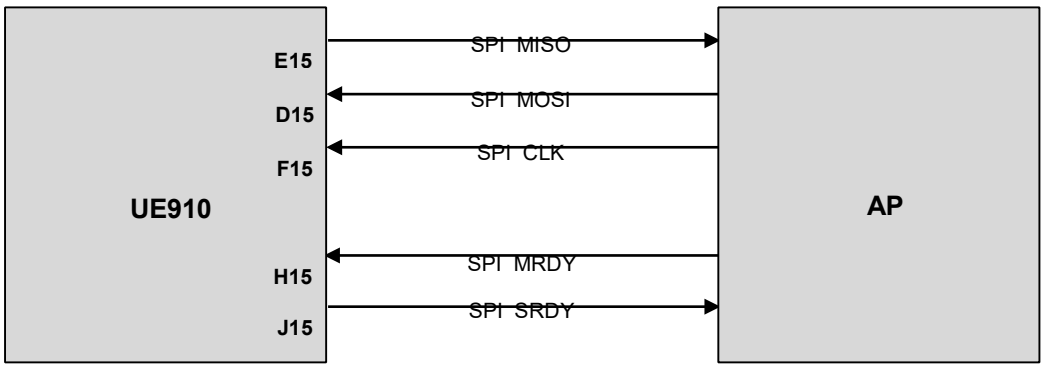
The UE910 Module is provided by one SPI interface.
The SPI interface defines two handshake lines for flow control and mutual wake-up of the modem and the Application Processor: SRDY (slave ready) and MRDY (master ready).

The AP has the master role, that is, it supplies the clock.
The following table is listing the available signals:

| PAD | Signal | I/O | Function | Type | NOTE |
|---|---|---|---|---|---|
| **D15** | SPI_MOSI | I | SPI MOSI | CMOS 1.8V | Shared with TX_AUX |
| **E15** | SPI_MISO | O | SPI MISO | CMOS 1.8V | Shared with RX_AUX |
| **F15** | SPI_CLK | I | SPI Clock | CMOS 1.8V | |
| **H15** | SPI_MRDY | I | SPI_MRDY | CMOS 1.8V | |
| **J15** | SPI_SRDY | O | SPI_SRDY | CMOS 1.8V | |

NOTE:
Due to the shared functions, when the SPI port is used, it is not possible to use the AUX_UART port.

#### 6.2.3.1 *SPI Connections*



### 6.2.4 Serial Ports

The UE910 module is provided with by 2 Asynchronous serial ports:
- MODEM SERIAL PORT 1 (Main)
- MODEM SERIAL PORT 2 (Auxiliary)

Several configurations can be designed for the serial port on the OEM hardware, but the most common are:
- RS232 PC com port
- microcontroller UART @ 1.8V (Universal Asynchronous Receive Transmit)
- microcontroller UART @ 5V or other voltages different from 1.8V

Depending from the type of serial port on the OEM hardware a level translator circuit may be needed to make the system work.
On the UE910 the ports are CMOS 1.8.

#### 6.2.4.1 *MODEM SERIAL PORT 1 (USIF0)*

The serial port 1 on the UE910 is a +1.8V UART with all the 7 RS232 signals.
It differs from the PC-RS232 in the signal polarity (RS232 is reversed) and levels.

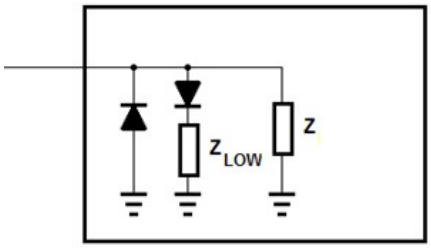
The following table is listing the available signals:

| RS232 Pin | Signal | Pad | Name | Usage |
|---|---|---|---|---|
| 1 | C109/DCD | **N14** | Data Carrier Detect | Output from the UE910 that indicates the carrier presence |
| 2 | C104/RXD | **M15** | Transmit line *see Note | Output transmit line of UE910 UART |
| 3 | C103/TXD | **N15** | Receive line *see Note | Input receive of the UE910 UART |
| 4 | C108/DTR | **M14** | Data Terminal Ready | Input to the UE910 that controls the DTE READY condition |
| 5 | GND | **M12, B13, P13, E14 …** | Ground | Ground |
| 6 | C107/DSR | **P14** | Data Set Ready | Output from the UE910 that indicates the module is ready |
| 7 | C106/CTS | **P15** | Clear to Send | Output from the UE910 that controls the Hardware flow control |
| 8 | C105/RTS | **L14** | Request to Send | Input to the UE910 that controls the Hardware flow control |
| 9 | C125/RING | **R14** | Ring Indicator | Output from the UE910 that indicates the incoming call condition |

The following table shows the typical input value of internal pull-up resistors for RTS, DTR and TXD input lines and in all module states:

| STATE | RTS DTR TXD | |
|---|---|---|
| | | Pull up tied to |
| ON | 5K to 12K | 1V8 |
| OFF | Schottky diode | |
| RESET | Schottky diode | |
| POWER SAVING | 5K to 12K | 1V8 |

The input line ON_OFF and HW_SHDN state can be treated as in picture below




NOTE:
According to V.24, some signal names are referred to the application side, therefore on the UE910 side these signal are on the opposite direction: TXD on the application side will be connected to the receive line (here named C103/TXD)
RXD on the application side will be connected to the transmit line (here named C104/RXD)

For a minimum implementation, only the TXD, RXD lines can be connected, the other lines can be left open provided a software flow control is implemented.

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the UE910 when the module is powered off or during an ON/OFF transition.

### 6.2.4.2 *MODEM SERIAL PORT 2 (USIF1)*

The secondary serial port on the UE910 is a CMOS1.8V with only the RX and TX signals.
The signals of the UE910 serial port are:

| PAD | Signal | I/O | Function | Type | NOTE |
|---|---|---|---|---|---|
| **D15** | TX_AUX | O | Auxiliary UART (TX Data to DTE) | CMOS 1.8V | Shared with SPI_MOSI |
| **E15** | RX_AUX | I | Auxiliary UART (RX Data from DTE) | CMOS 1.8V | Shared with SPI_MISO |

NOTE:
Due to the shared pins, when the Modem Serial port is used, it is not possible to use the SPI functions.

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the UE910 when the module is powered off or during an ON/OFF transition.

### 6.2.4.3 *RS232 LEVEL TRANSLATION*

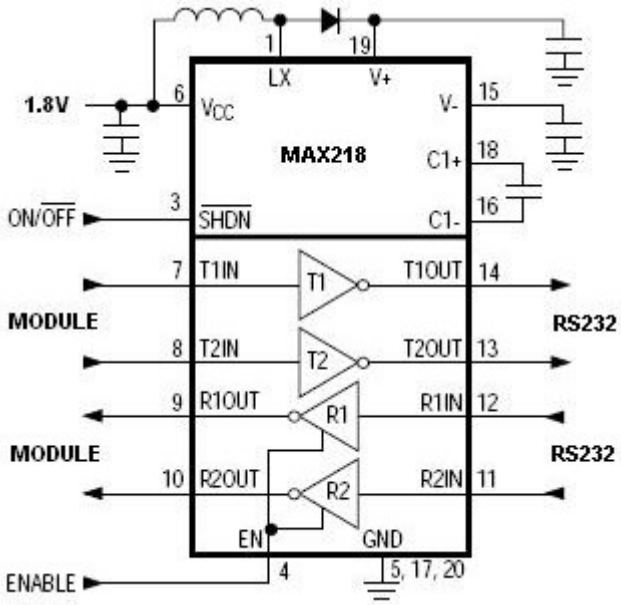
In order to interface the UE910 with a PC com port or a RS232 (EIA/TIA-232) application a level translator is required. This level translator must:

- invert the electrical signal in both directions;
- Change the level from 0/1.8V to +15/-15V.

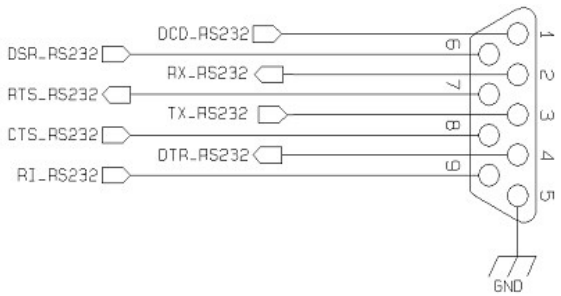
Actually, the RS232 UART 16450, 16550, 16650 & 16750 chipsets accept signals with lower levels on the RS232 side (EIA/TIA-562), allowing a lower voltage-multiplying ratio on the level translator. Note that the negative signal voltage must be less than 0V and hence some sort of level translation is always required.
The simplest way to translate the levels and invert the signal is by using a single chip level translator. There are a multitude of them, differing in the number of drivers and receivers and in the levels (be sure to get a true RS232 level translator not a RS485 or other standards).
By convention the driver is the level translator from the 0-1.8V UART to the RS232 level. The receiver is the translator from the RS232 level to 0-1.8V UART.
In order to translate the whole set of control lines of the UART you will need:

- 5 drivers
- 3 receivers

An example of RS232 level adaptation circuitry could be done using a MAXIM transceiver (MAX218) In this case the chipset is capable to translate directly from 1.8V to the RS232 levels (Example done on 4 signals only).




The RS232 serial port lines are usually connected to a DB9 connector with the following layout:



## 6.3 General Purpose I/O

The UE910 module is provided by a set of Configurable Digital Input / Output pins (CMOS 1.8V)
Input pads can only be read; they report the digital value (high or low) present on the pad at the read time.
Output pads can only be written or queried and set the value of the pad output.
An alternate function pad is internally controlled by the UE910 firmware and acts depending on the function implemented.

The following table shows the available GPIO on the UE910:

| PAD | Signal | I/O | Drive Strength | Default State | NOTE |
|---|---|---|---|---|---|
| **C8** | GPIO_01 | I/O | **1** mA | INPUT | Alternate function STAT LED |
| **C9** | GPIO_02 | I/O | **1** mA | INPUT | |
| **C10** | GPIO_03 | I/O | **1** mA | INPUT | |
| **C11** | GPIO_04 | I/O | **1** mA | INPUT | |
| **B14** | GPIO_05 | I/O | **1** mA | INPUT | |
| **C12** | GPIO_06 | I/O | **1** mA | INPUT | |
| **C13** | GPIO_07 | I/O | **1** mA | INPUT | |
| **K15** | GPIO_08 | I/O | **1** mA | INPUT | |
| **L15** | GPIO_09 | I/O | **1** mA | INPUT | |
| **G15** | GPIO_10 | I/O | **1** mA | INPUT | |

### 6.3.1 Using a GPIO as INPUT

The GPIO pads, when used as inputs, can be connected to a digital output of another device and report its status, provided this device has interface levels compatible with the 1.8V CMOS levels of the GPIO.
If the digital output of the device to be connected with the GPIO input pad has interface levels different from the 1.8V CMOS, then it can be buffered with an open collector transistor with a 47K pull up to 1.8V.

NOTE:
In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the UE910 when the module is powered off or during an ON/OFF transition.

### 6.3.2 Using a GPIO as OUTPUT

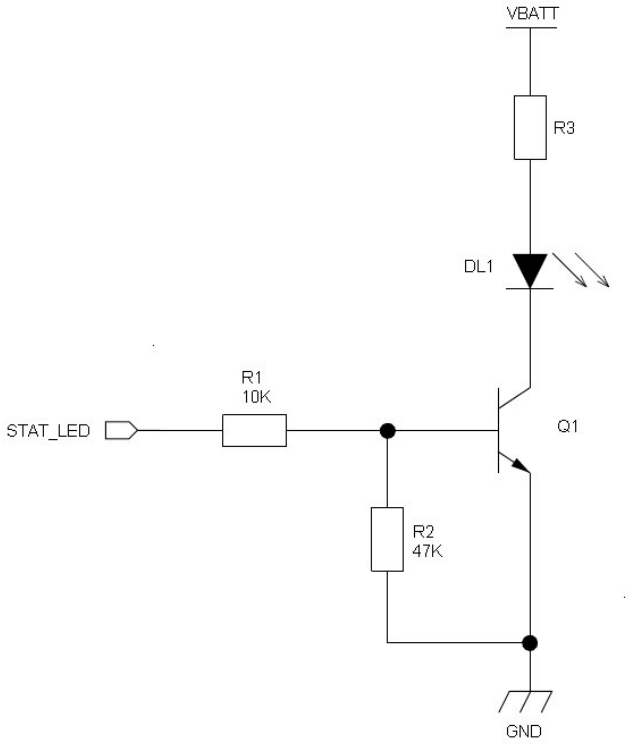
The GPIO pads, when used as outputs, can drive 1.8V CMOS digital devices or compatible hardware. When set as outputs, the pads have a push-pull output and therefore the pull-up resistor may be omitted.

### 6.3.3 Indication of network service availability

The STAT_LED pin status shows information on the network service availability and Call status. The function is available as alternate function of GPIO_01 (to be enabled using the AT#GPIO=1,0,2 command).
In the UE910 modules, the STAT_LED needs an external transistor to drive an external LED. Therefore, the status indicated in the following table is reversed with respect to the pin status

| Device Status | Led Status |
|---|---|
| Device off | Permanently off |
| Not Registered | Permanently on |
| Registered in idle | Blinking 1sec on + 2 sec off |
| Registered in idle + power saving | It depends on the event that triggers the wakeup (In sync with network paging) |
| Voice Call Active | Permanently on |
| Dial-Up | Blinking 1 sec on + 2 sec off |

A schematic example could be:




## 6.4 External SIM Holder

Please refer to the related User Guide (SIM Holder Design Guides, 80000NT10001a).

## 6.5 ADC Converter

The UE910 is provided by one AD converter. It is able to read a voltage level in the range of 0÷1.2 volts applied on the ADC pin input, store and convert it into 10 bit word.

The input line is named as **ADC_IN1** and it is available on Pad **B1**

The following table is showing the ADC characteristics:

| Item | Min | Typical | Max | Unit |
|---|---|---|---|---|
| Input Voltage range | 0 | - | 1.2 | Volt |
| AD conversion | - | - | 10 | bits |
| Input Resistance | 1 | - | - | Mohm |
| Input Capacitance | - | 1 | - | pF |

The ADC could be controlled using an AT command.
The command is ***AT#ADC=1,2***
The read value is expressed in mV

Refer to SW User Guide or AT Commands Reference Guide for the full description of this function.

# 7 RF SECTION

## 7.1 Bands Variants

The following table is listing the supported Bands:

| Product | Supported 3G bands |
|---|---|
| UE910-EU | FDD B1, B8 |

## 7.2 TX Output Power

| Band | Power Class |
|---|---|
| GSM 900 | Class 4 (2W) |
| DCS 1800 | Class 1 (15W) |
| FDD B1, B8 | Class 3 (0.25W) |

## 7.3 RX Sensitivity

| Band | Power Class |
|---|---|
| GSM 900 | -109dBm |
| DCS 1800 | -110dBm |
| FDD B1, B8 | -111dBm |

# 7.4 Antenna Requirements

## 7.4.1 Main Antenna

The antenna connection and board layout design are the most important aspect in the full product design as they strongly affect the product overall performances, hence read carefully and follow the requirements and the guidelines for a proper design.

The antenna and antenna transmission line on PCB for a Telit UE910-EU device shall fulfil the following requirements:

| Item | Value |
|---|---|
| Frequency range | Depending by frequency band(s) provided by the network operator, the customer shall use the most suitable antenna for that/those band(s) |
| Bandwidth | 80 MHz in GSM900<br>170 MHz in DCS |
| Bandwith(WCDMA) | 250 MHz in WCDMA B1<br>80 MHz in WCDMA B8 |
| Impedance | 50 ohm |
| Input power | >33 dBm (2W) peak power in GSM<br>>24dBm Average power in WCDMA |
| VSWR absolute max | ≤ 10:1 (limit to avoid permanent damage) |

### 7.4.2 PCB design guidelines

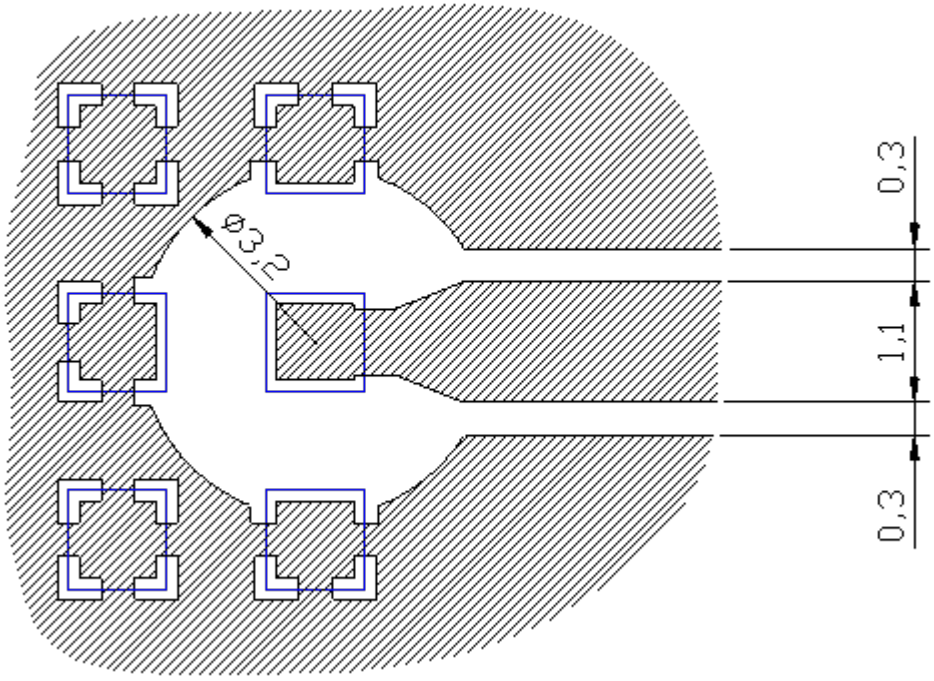
When using the UE910-EU, since there's no antenna connector on the module, the antenna must be connected to the UE910-EU antenna pad (K1) by means of a transmission line implemented on the PCB. In the case the antenna is not directly connected at the antenna pad of the UE910-EU, then a PCB line is needed in order to connect with it or with its connector. This transmission line shall fulfil the following requirements:

| Item | Value |
|---|---|
| Characteristic Impedance | 50 ohm |
| Max Attenuation | 0,3 dB |
| Coupling | Coupling with other signals shall be avoided |
| Ground Plane | Cold End (Ground Plane) of antenna shall be equipotential to the UE910-EU ground pins |

The transmission line should be designed according to the following guidelines:

- Ensure that the antenna line impedance is 50 ohm;
- Keep the antenna line on the PCB as short as possible, since the antenna line loss shall be less than 0,3 dB;
- Antenna line must have uniform characteristics, constant cross section; avoid meanders and abrupt curves;
- Keep, if possible, one layer of the PCB used only for the Ground plane;
- Surround (on the sides, over and under) the antenna line on PCB with Ground, avoid having other signal tracks facing directly the antenna line track;
- The ground around the antenna line on PCB has to be strictly connected to the Ground Plane by placing vias every 2mm at least;
- Place EM noisy devices as far as possible from UE910 antenna line;
- Keep the antenna line far away from the UE910 power supply lines;
- If you have EM noisy devices around the PCB hosting the UE910, such as fast switching ICs, take care of the shielding of the antenna line by burying it inside the layers of PCB and surround it with Ground planes, or shield it with a metal frame cover.
- If you don't have EM noisy devices around the PCB of UE910, by using a micro strip on the superficial copper layer for the antenna line, the line attenuation will be lower than a buried one;

The following image is showing the suggested layout for the Antenna pad connection:



# 8 AUDIO SECTION

## 8.1 Overview

The UE910-EU is provided by one digital Audio interface:

- Digital Audio Path

## 8.2 Digital Voice Interface

The UE910 Module is provided by one DVI digital voice interface.

The Signals are available on the following Pads:

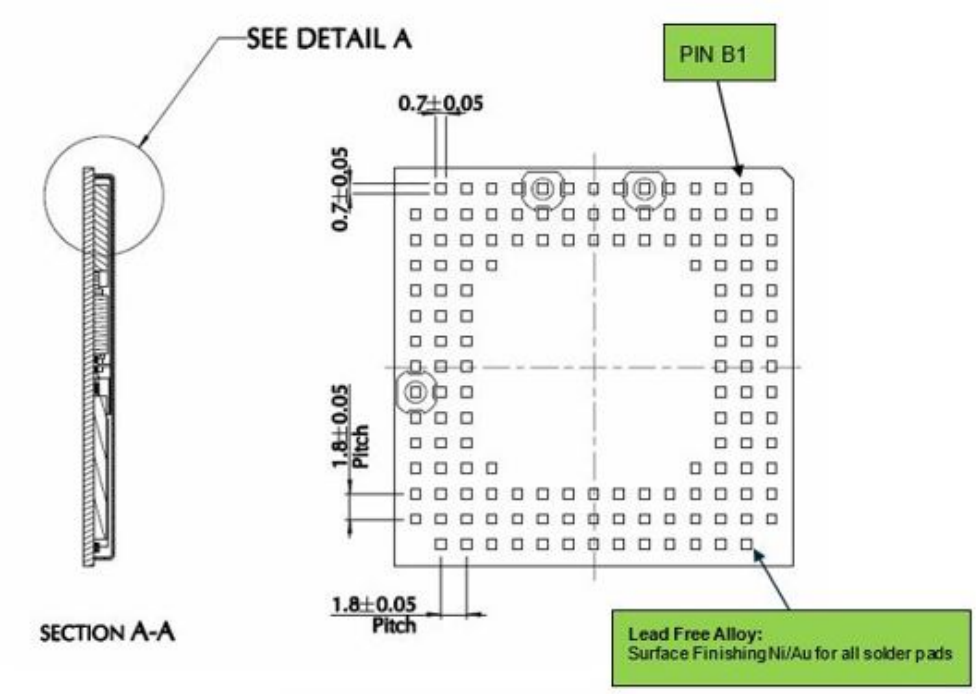
| PAD | Signal | I/O | Function |
|---|---|---|---|
| **B9** | DVI_WA0 | I/O | Digital Voice Interface (Word Alignment / LRCLK) |
| **B6** | DVI_RX | I | Digital Voice Interface (RX) |
| **B7** | DVI_TX | O | Digital Voice Interface (TX) |
| **B8** | DVI_CLK | I/O | Digital Voice Interface (BCLK) |

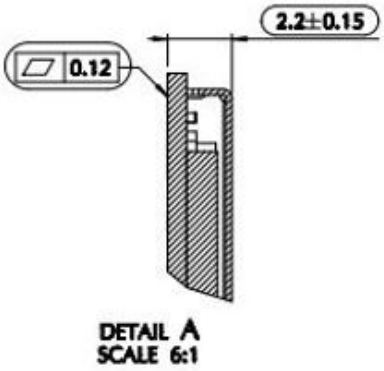
### 8.2.1 CODEC Examples

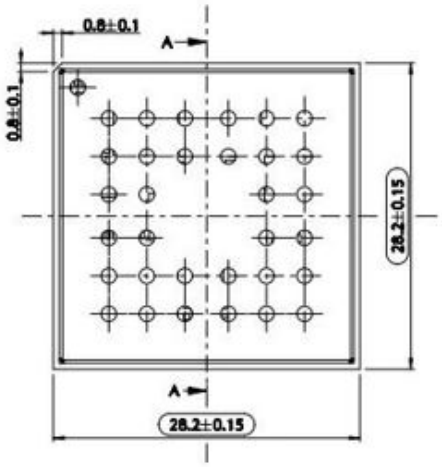
Please refer to the Digital Audio Application note.

# 9 MECHANICAL DESIGN

## 9.1 Drawing

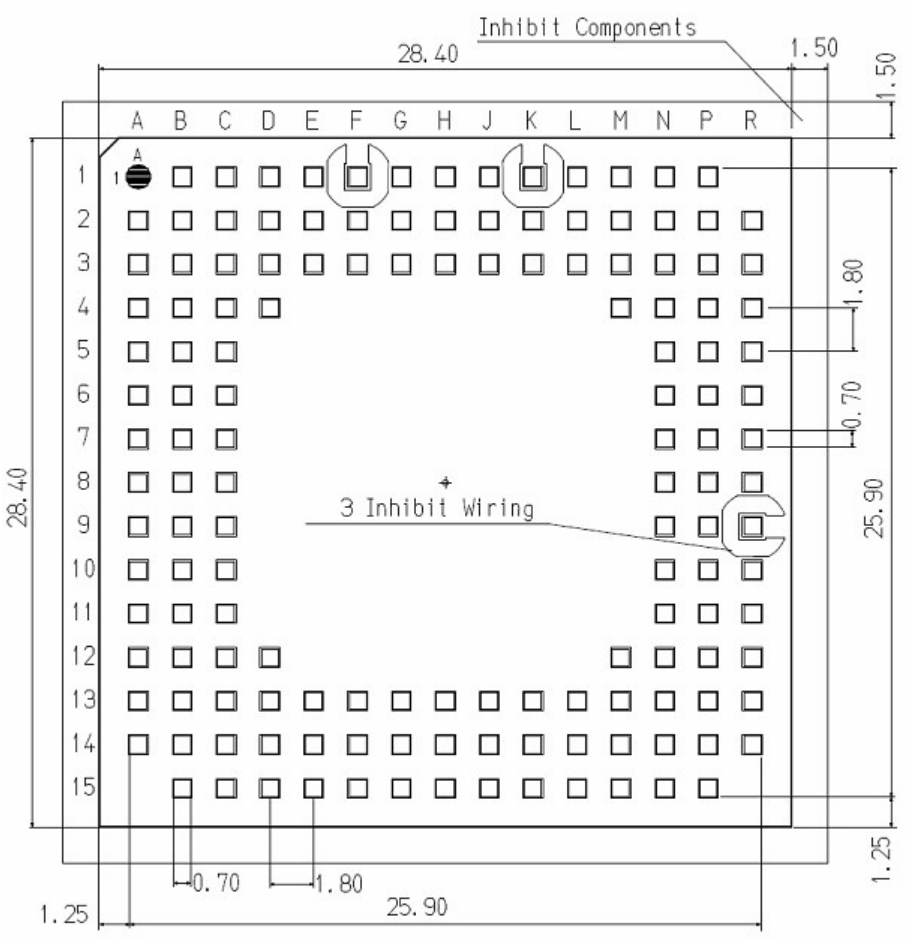


The UE910 modules have been designed in order to be compliant with a standard lead-free SMT process.

## 9.2 Footprint



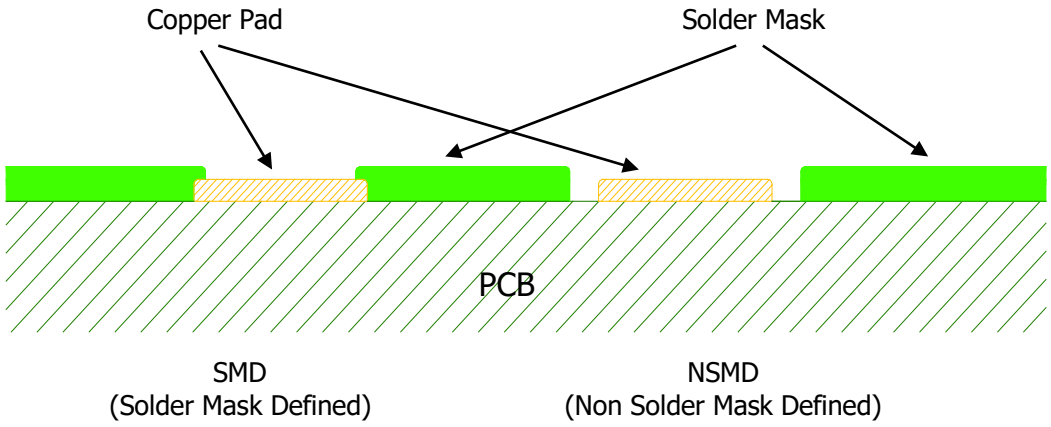

In order to easily rework the UE910-EU is suggested to consider on the application a 1.5 mm placement inhibit area around the module.
It is also suggested, as common rule for an SMT component, to avoid having a mechanical part of the application in direct contact with the module.

NOTE:
In the customer application, the region under WIRING INHIBIT (see figure above) must be clear from signal or ground paths.

# 10 APPLICATION DESIGN

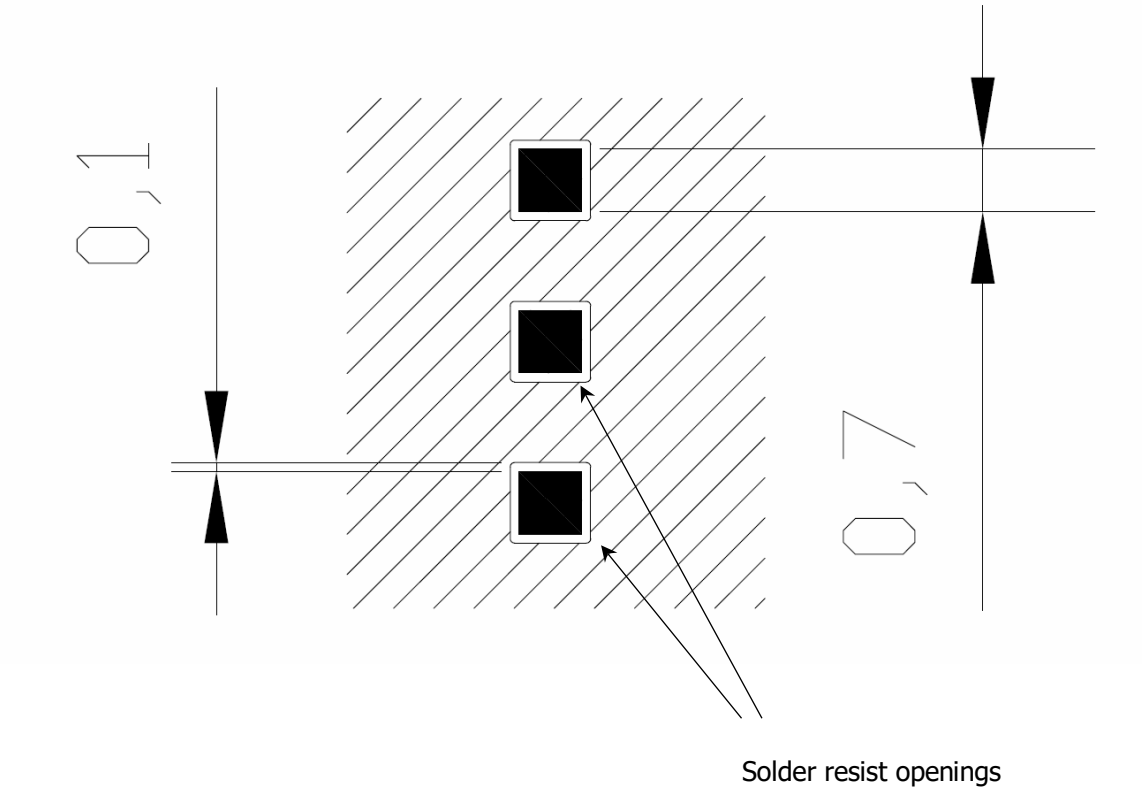
## 10.1 PCB pad design

Non solder mask defined (NSMD) type is recommended for the solder pads on the PCB.

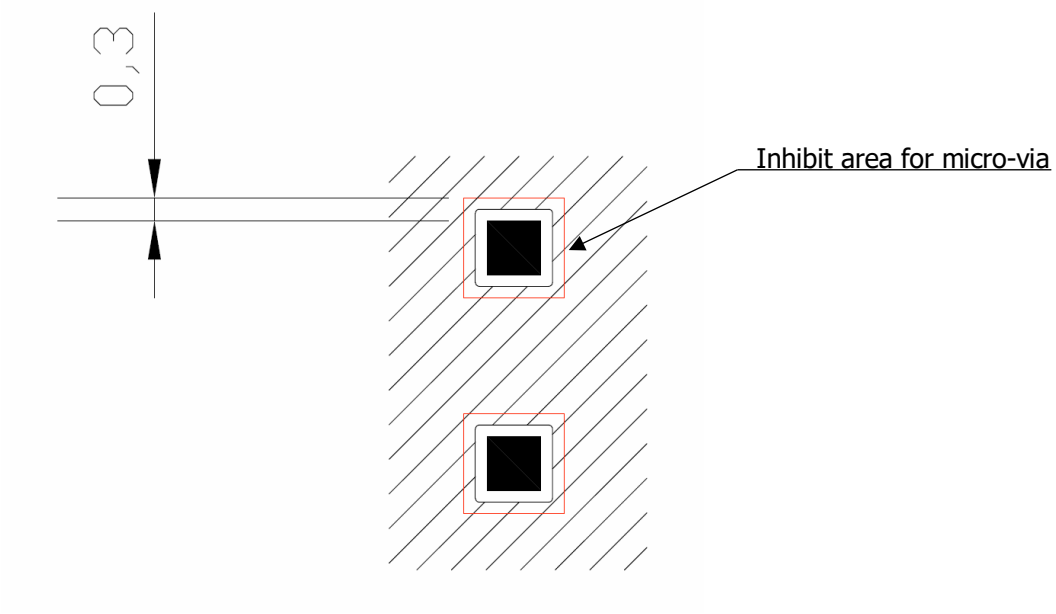



## 10.2 PCB pad dimensions

The recommendation for the PCB pads dimensions are described in the following image (dimensions in mm)



It is not recommended to place via or micro-via not covered by solder resist in an area of 0,3 mm around the pads unless it carries the same signal of the pad itself




Holes in pad are allowed only for blind holes and not for through holes.

Recommendations for PCB pad surfaces:

| Finish | Layer Thickness (um) | Properties |
|---|---|---|
| Electro-less Ni / Immersion Au | 3 –7 / 0.05 – 0.15 | good solder ability protection, high shear force values |

The PCB must be able to resist the higher temperatures which are occurring at the lead-free process. This issue should be discussed with the PCB-supplier. Generally, the wettability of tin-lead solder paste on the described surface plating is better compared to lead-free solder paste.
It is not necessary to panel the application's PCB, however in that case it is suggested to use milled contours and predrilled board breakouts; scoring or v-cut solutions are not recommended.

## 10.3 Stencil

Stencil's apertures layout can be the same of the recommended footprint (1:1), we suggest a thickness of stencil foil ≥ 120 µm.

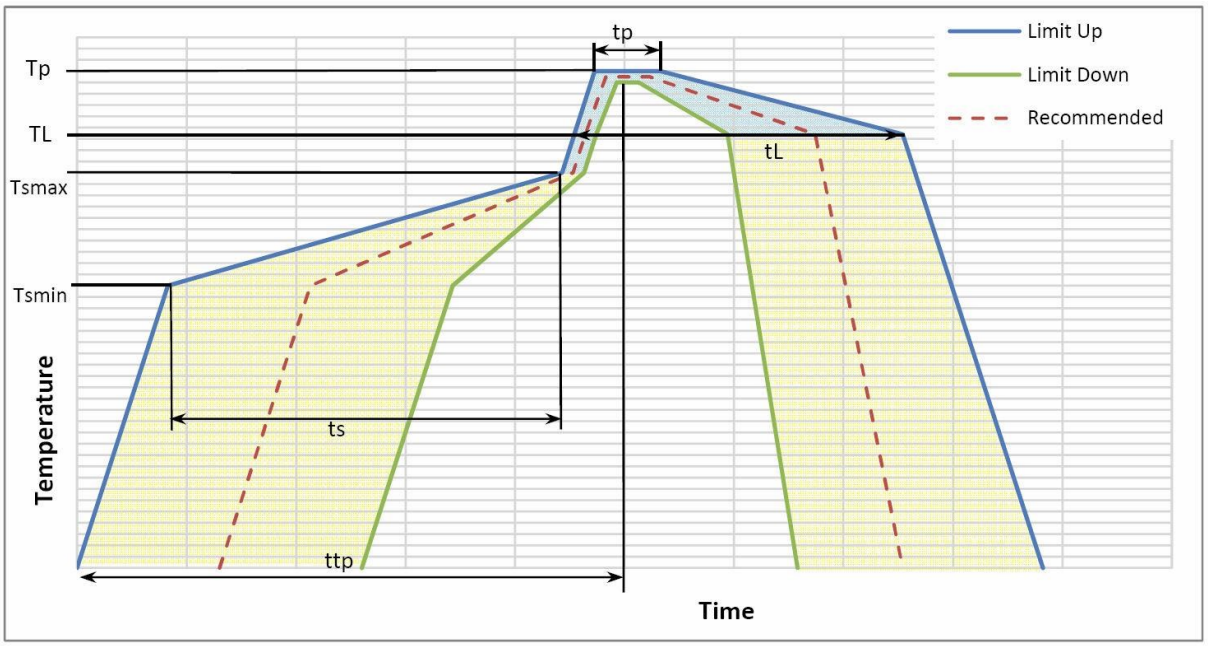
## 10.4 Solder paste

| Item | Lead Free |
|---|---|
| Solder Paste | Sn/Ag/Cu |

We recommend using only "no clean" solder paste in order to avoid the cleaning of the modules after assembly.

## 10.5 Solder reflow

Recommended solder reflow profile:



| Profile Feature | Pb-Free Assembly |
|---|---|
| Average ramp-up rate ($T_L$ to $T_P$) | 3°C/second max |
| Preheat<br>– Temperature Min (Tsmin)<br>– Temperature Max (Tsmax)<br>– Time (min to max) (ts) | <br>150°C<br>200°C<br>60-180 seconds |
| Tsmax to TL<br>– Ramp-up Rate | <br>3°C/second max |
| Time maintained above:<br>– Temperature (TL)<br>– Time (tL) | <br>217°C<br>60-150 seconds |
| Peak Temperature (Tp) | 245 +0/-5°C |
| Time within 5°C of actual Peak Temperature (tp) | 10-30 seconds |
| Ramp-down Rate | 6°C/second max. |
| Time 25°C to Peak Temperature | 8 minutes max. |

NOTE:

All temperatures refer to topside of the package, measured on the package body surface

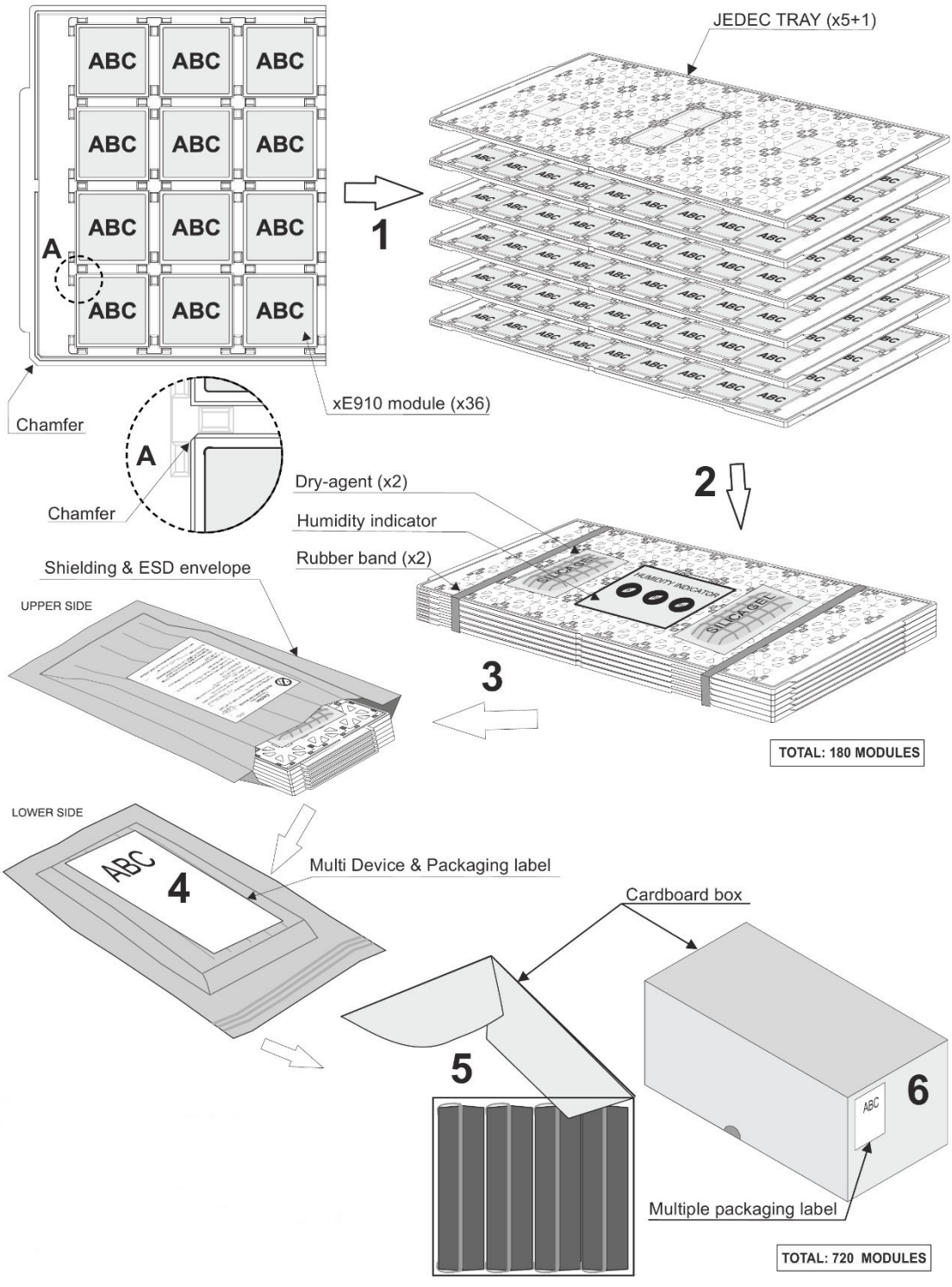
WARNING:

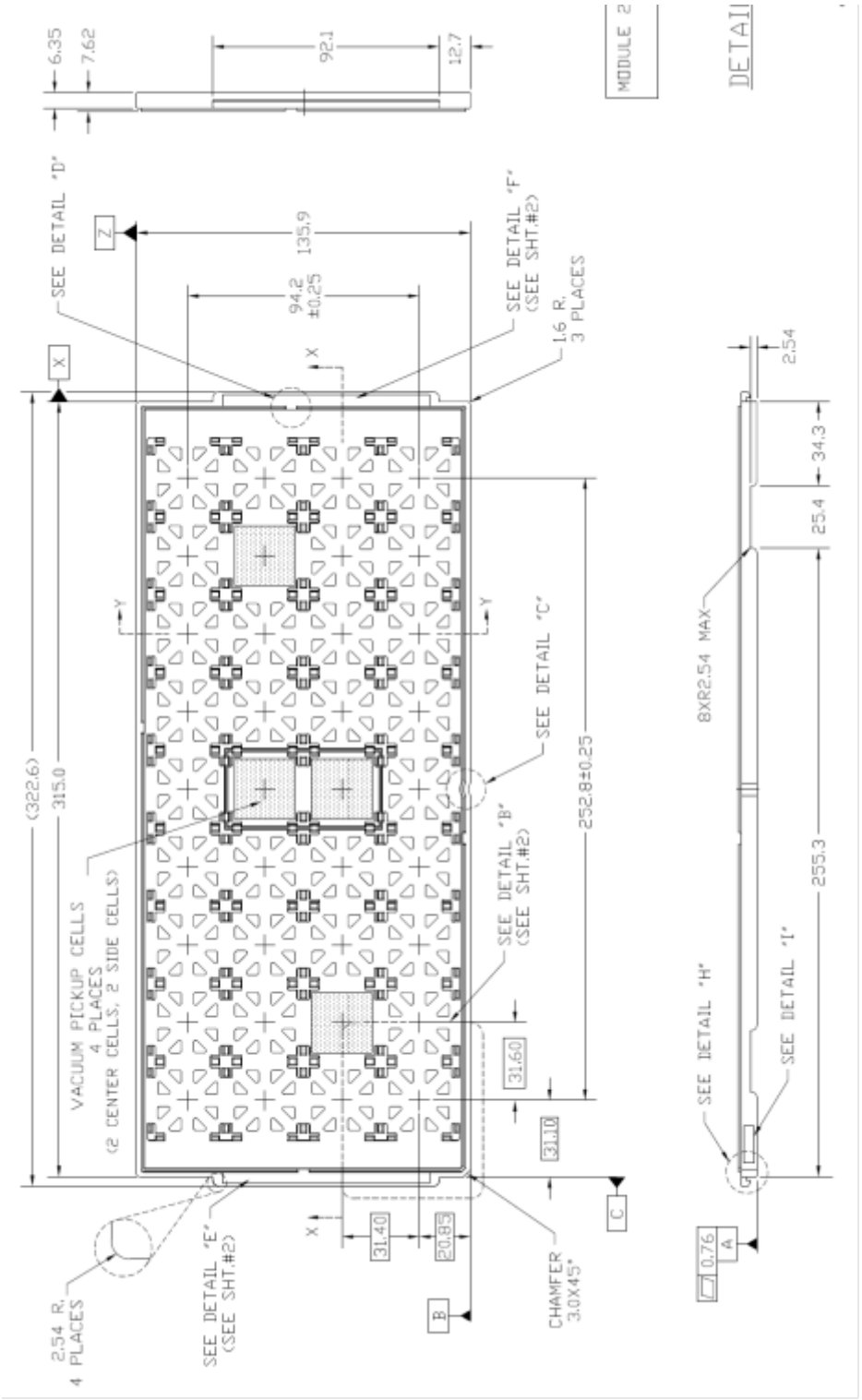
The UE910-EU module withstands one reflow process only.

# 11 PACKAGING

## 11.1 Tray

The UE910-EU modules are packaged on trays of ***36*** pieces each. These trays can be used in SMT processes for pick & place handling.

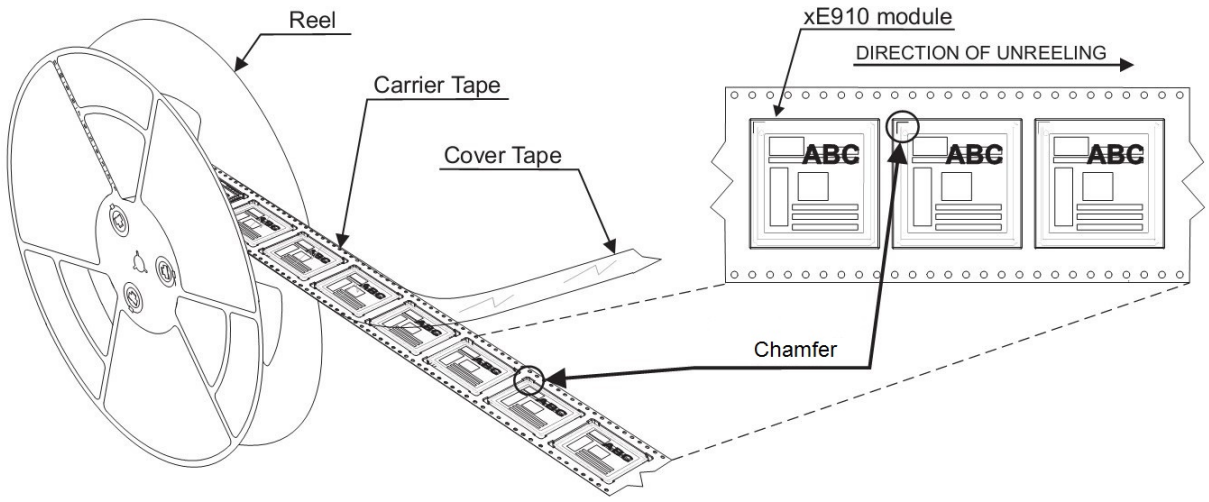




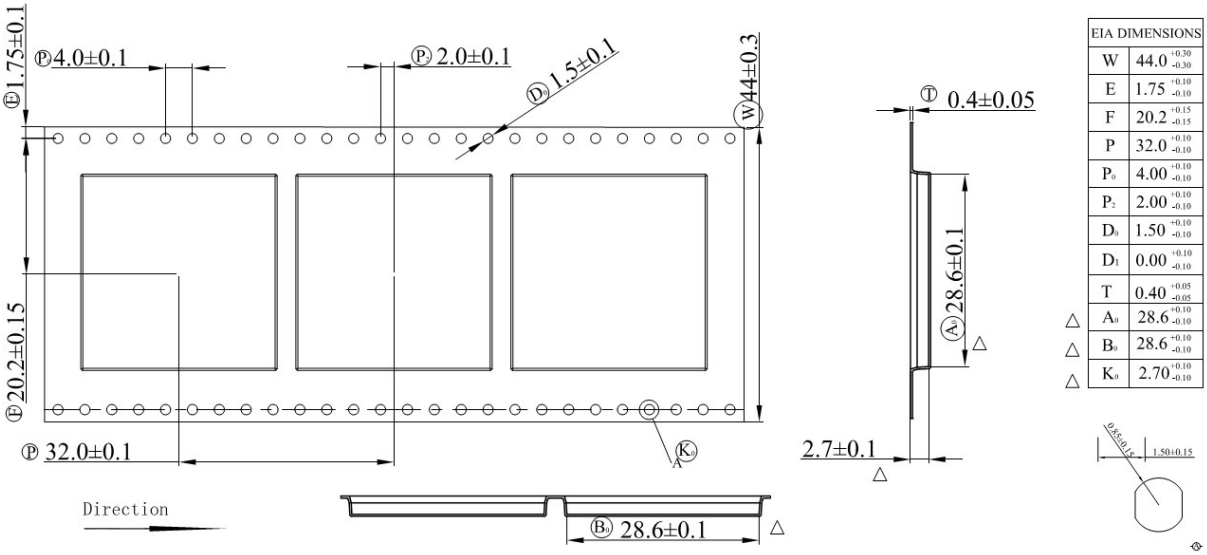
## 11.2 Reel

The UE910 can be packaged on reels of 200 pieces each.

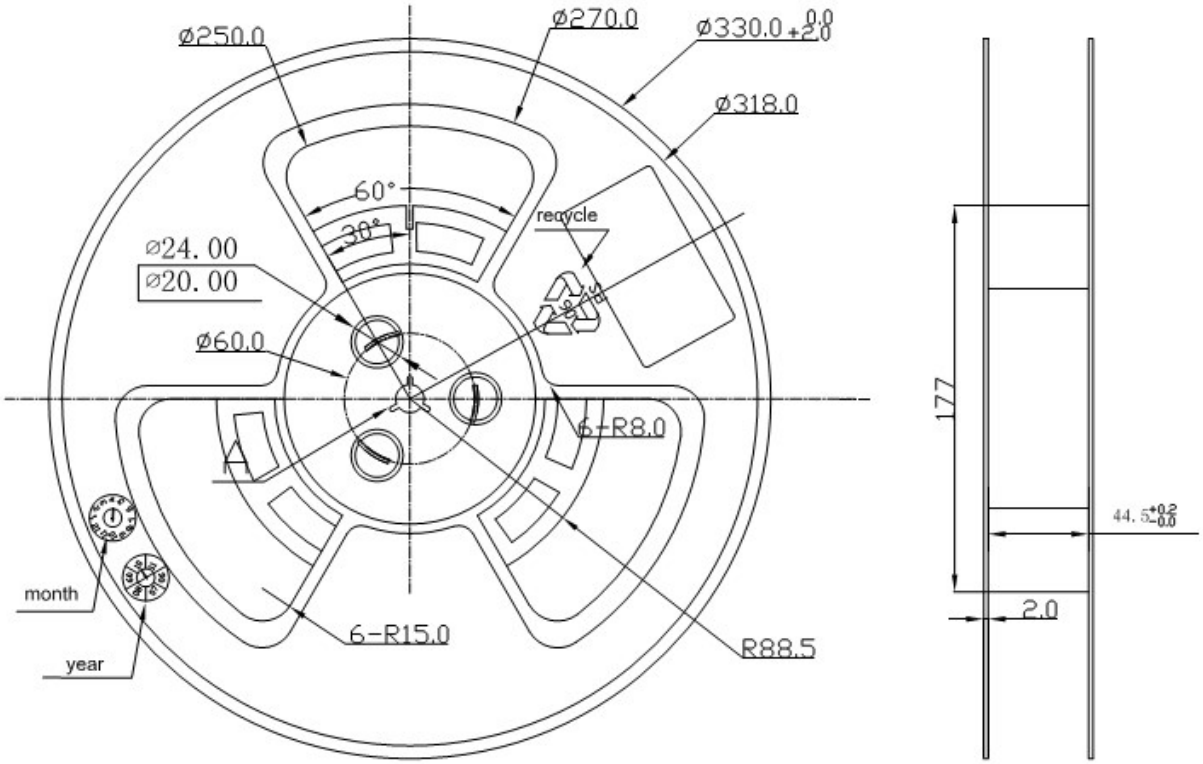
See figure for module positioning into the carrier.



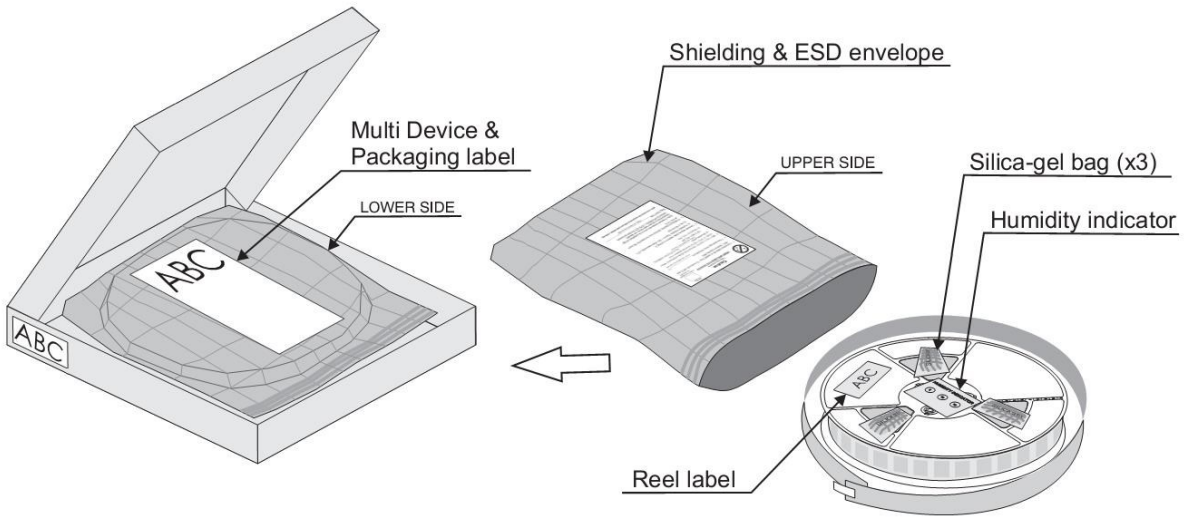

### 11.2.1 Carrier Tape Detail



## 11.2.2 Reel Detail




## 11.2.3 Reel Box Detail



## 11.3 Moisture sensitivity

The UE910 is a Moisture Sensitive Device level 3, according to standard IPC/JEDEC J-STD-020, take care all the relatives requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

a) Calculated shelf life in sealed bag is 12 months when stored in a noncondensing atmospheric environment of <40°C/90% RH.

b) Environmental condition during the production: ≤30°C/60% RH according to IPC/JEDEC J-STD033.

c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition b) IPC/JEDEC J-STD-033 is respected.

d) Baking is required if conditions b) or c) are not respected.

e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more

# 12 SAFETY RECOMMANDATIONS

**READ CAREFULLY**

Be sure the use of this product is allowed in the country and in the environment required. The use of this product may be dangerous and has to be avoided in the following areas:

Where it can interfere with other electronic devices in environments such as hospitals, airports, aircrafts, etc

Where there is risk of explosion such as gasoline stations, oil refineries, etc

It is responsibility of the user to enforce the country regulation and the specific environment regulation.

Do not disassemble the product; any mark of tampering will compromise the warranty validity.

We recommend following the instructions of the hardware user guides for a correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to be conforming to the security and fire prevention regulations.

The product has to be handled with care, avoiding any contact with the pins because electrostatic discharges may damage the product itself. Same cautions have to be taken for the SIM, checking carefully the instruction for its use. Do not insert or remove the SIM when the product is in power saving mode.

The system integrator is responsible of the functioning of the final product; therefore, care has to be taken to the external components of the module, as well as of any project or installation issue, because the risk of disturbing the LTE network or external devices or having impact on the security. Should there be any doubt, please refer to the technical documentation and the regulations in force.

Every module has to be equipped with a proper antenna with specific characteristics. The antenna has to be installed with care in order to avoid any interference with other electronic devices and has to guarantee a minimum distance from the body (20 cm). In case of this requirement cannot be satisfied, the system integrator has to assess the final product against the SAR regulation.

The European Community provides some Directives for the radio equipment introduced on the market. All the relevant information's are available on the European Community website:
https://ec.europa.eu/growth/single-market/european-standards/harmonised-standards/rtte_en

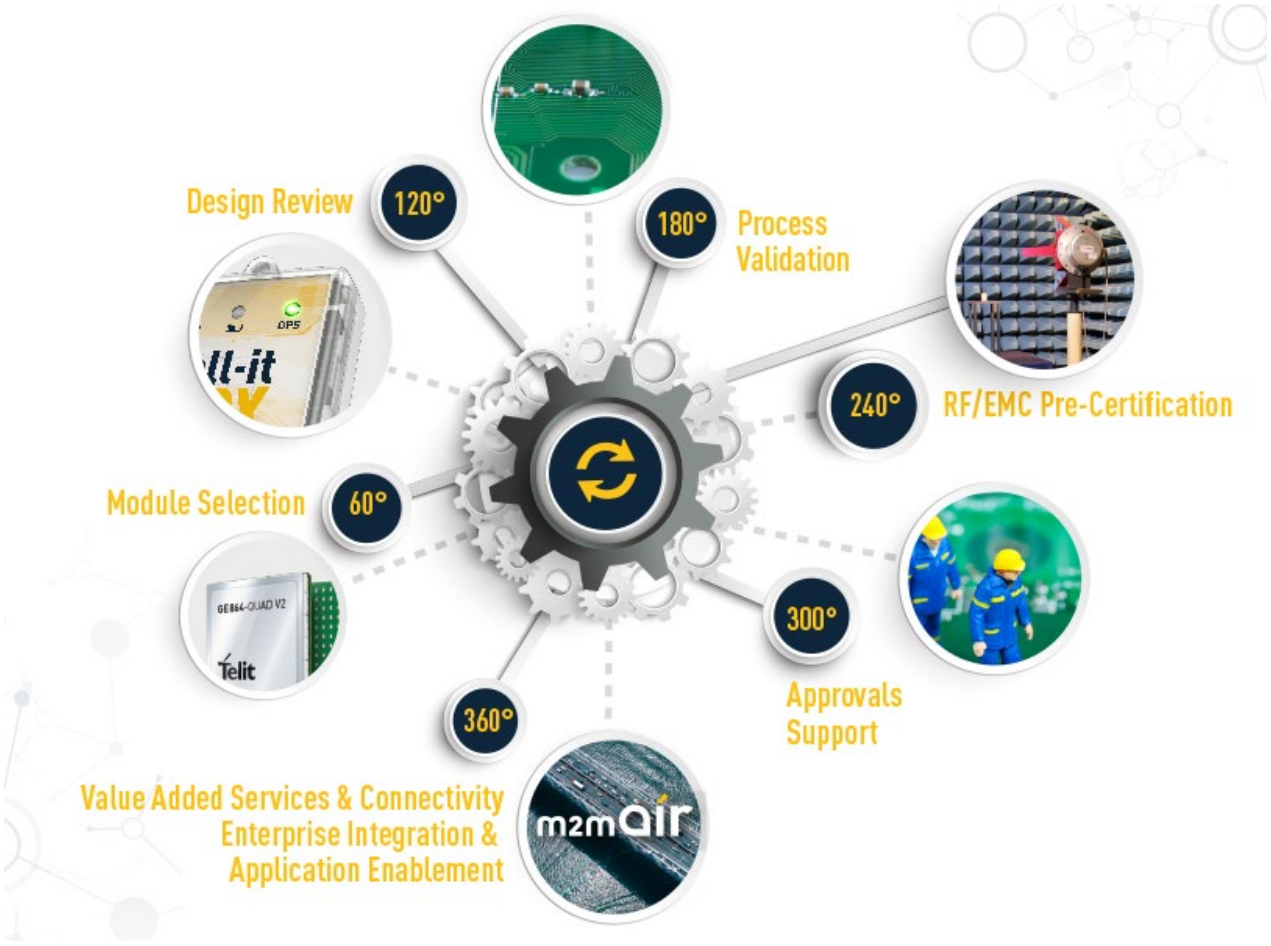
The text of the Directive 2014/53/EU regarding radio equipment is available at:

http://eur-lex.europa.eu/legal-content/EN/TXT/?qid=1429097565265&uri=CELEX:32014L0053

# 13 DOCUMENT HISTORY

## 13.1 Revisions

| Revision | Date | Changes |
|---|---|---|
| 0 | 2015-07-24 | First Issue |
| 1 | 2017-05-10 | Updated par 8 and Pad layout; Modified reference to 2014/53/EU Directive |
| 2 | 2019-02-06 | Updated par 11.1 Tray Packaging |
| | | |
| | | |
| | | |


Design Review
120°
180°
Process
Validation
240°
RF/EMC Pre-Certification
Module Selection
60°
300°
Approvals
Support
360°
Value Added Services & Connectivity
Enterprise Integration &
Application Enablement
m2mair