



# xE866 Global Form Factor Application Note

80439NT11318A Rev.3 – 2017-04-18

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## APPLICABILITY TABLE (REMOVE UNUSED)

### PRODUCTS

-   GE866-QUAD
-   UE866 SERIES
-   LE866 SERIES
-   ME866 SERIES
-   NE866 SERIES

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## 1. INTRODUCTION

### 1.1. Scope

The aim of this document is the description of some hardware solutions useful for developing an application compatible with the products: Telit GE866, Telit UE866, Telit LE866 and to highlight the minor differences between the above mentioned products.

### 1.2. Contact Information, Support

For general contact, technical support services, technical questions and report documentation errors contact Telit Technical Support at:

- TS-EMEA@telit.com
- TS-AMERICAS@telit.com
- TS-APAC@telit.com

Alternatively, use:

<http://www.telit.com/support>

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

<http://www.telit.com>

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

### 1.3. Text Conventions

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Danger – This information **MUST** be followed or catastrophic equipment failure or bodily injury may occur.

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Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

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Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

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All dates are in ISO 8601 format, i.e. YYYY-MM-DD.



#### 1.4. Related Documents

- GE866-QUAD Hardware User Guide, 1VV0301051 Rev. 6
- UE866 Hardware User Guide, 1VV0301157 Rev. 11
- LE866 Hardware User Guide, 1VV0301210 Rev. 5
- LE866 PSM Application Note, 80471NT11483A Rev. 1
- NE866B1 HW User Guide 1VV0301354 Rev. 2
- ME866 HARDWARE USER GUIDE 1vv0301346 Rev.0 - Preliminary

## 2. OVERVIEW

In this document all the basic functions of a mobile phone will be taken into account; for each one of them a proper hardware solution will be suggested and eventually the wrong solutions and common errors to be avoided will be evidenced. Obviously, this document cannot embrace the whole hardware solutions and products that may be designed. The wrong solutions to be avoided shall be considered as mandatory, while the suggested hardware configurations shall not be considered mandatory, instead the information given shall be used as a guide and a starting point for properly developing your product with the described modules. For further hardware details that may not be explained in this document refer to the Telit Product Description documents where all the hardware information is reported.

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### NOTICE:

The integration of the xE866 cellular module within user application shall be done according to the design rules described in this manual.

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The Unified Form Factor (UFF) is a concept of a products family characterized by the same mechanical and electrical form factor with different radio access technology.

This new approach protects customer's investment by giving you the possibility to migrate with the simple plug-and-play switch of your module with other wireless modules in the Unified Form Factor range without changing your application. In this way Telit offers easy access to different cellular technologies, certifications or bandwidth. For example if you develop applications based on today's mobile operator GSM/GPRS cellular technology if required it might be upgraded in the future to higher data speed capability such as UMTS/HSDPA.

The main advantages are summarized below:

- Increase of the efficiency in the use of the investments assigned to the development of the application (NRE), resulting in higher ROI, thus justifying the business choice of the UFF products;
- Products that are designed to bring technology enhancements to the integrators, such as higher data rates and new wireless standards while maintaining backwards compatibility in form factor and logical interfaces;
- Ease of integration;
- Telit as a single supplier of wireless modems;
- The customer can focus on its core business and application, not the management of operations and procurement required for wireless modems;
- One single application for different markets.

Telit, acknowledging the requirements of the developers, has taken great care to minimize any difference in the interface of the products with the Unified Form Factor; nevertheless some minor differences are still present. Differences are mainly due by the fact that different technologies have different electrical and mechanical characteristics, however, the application can, with some care, easily accommodate multiple wireless modems.

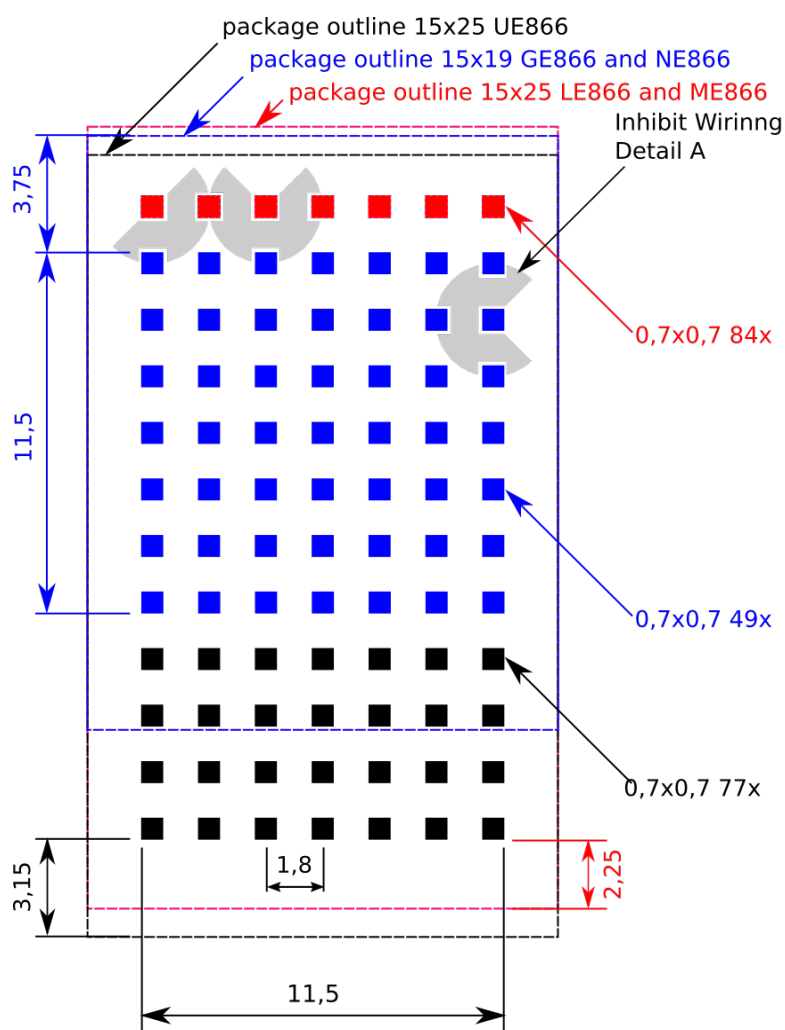
This document has been created to guide you when developing applications based on Unified Form Factor concept by pointing out module differences

### 3. MECHANICAL DIMENSIONS

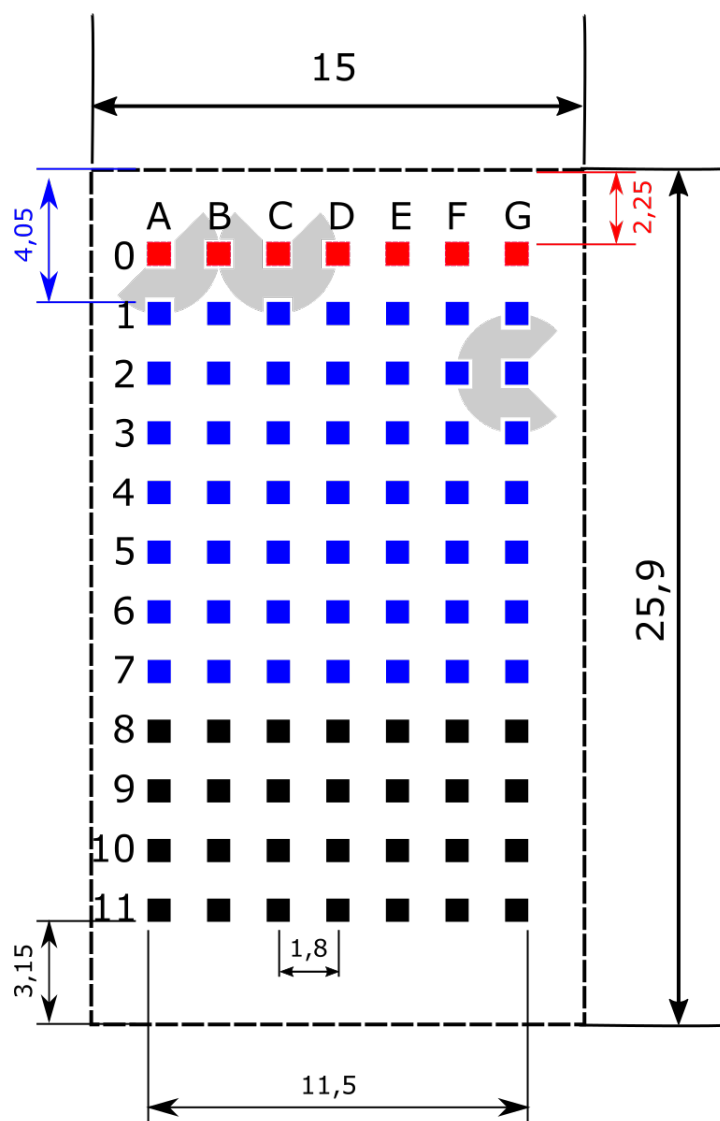
The Telit xE866 overall dimensions are:

	LENGTH (MM)	WIDTH (MM)	THICKNESS (MM)
<b>GE866</b>	19	15	2.2
<b>UE866</b>	25	15	2.2
<b>LE866</b>	25	15	2.2
<b>ME866</b>	25	15	2.2
<b>NE866</b>	19	15	2.2

In a common design application which is going to use multiple models, we recommend to consider the highest dimensions as reference.



If figure below is indicated the minimum clearance needed in order to have the possibility to mount all xE866 family products (all sizes are in mm):



Note that the alignment between the different footprints shall be the A1 pad and not the module mechanical corner.



**NOTE:**

In order to easily rework the xE866, it is suggested considering on the application 1.5mm placements inhibit area around the module.

**NOTE:**

The 3D drawings/models versions are available separately and they are provided in IGES format. Please contact the TELIT technical support to get the models.

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## 4. MODULE CONNECTIONS

### 4.1. Common PIN-OUT

PIN	SIGNAL	I/O	FUNCTION	TYPE	COMMENT
<b>PROG. / DATA + HW FLOW CONTROL</b>					
<b>A4</b>	C103/TXD	I	Serial data input from DTE	CMOS 1.8V	
<b>A5</b>	C104/RXD	O	Serial data output to DTE	CMOS 1.8V	
<b>B1</b>	C106/CTS(*)	O	Output for Clear to Send signal (CTS) to DTE	CMOS 1.8V	
<b>A1</b>	RTS(*)	I	Input for request to Send signal (RTS) from DTE	CMOS 1.8V	
<b>Asynchronous Auxiliary Serial Port 2</b>					
<b>C1</b>	TX_AUX	O	Auxiliary UART (TX Data to DTE)	CMOS 1.8V	Primary Logging Port
<b>C2</b>	RX_AUX(*)	I	Auxiliary UART (RX Data from DTE)	CMOS 1.8V	
<b>POWER SUPPLY</b>					
<b>E2</b>	VBATT	-	Main power supply (Baseband)	Power	
<b>E1</b>	VBATT_PA	-	Main power supply (Radio PA)	Power	
<b>SIM CARD INTERFACE</b>					
<b>C7</b>	SIMVCC	-	External SIM signal – Power supply for the SIM	1.8 / 3V	

<b>B7</b>	SIMRST	O	External SIM signal – Reset	1.8 / 3V
<b>A6</b>	SIMIO	I/O	External SIM signal - Data I/O	1.8 / 3V
<b>A7</b>	SIMCLK	O	External SIM signal – Clock	1.8 / 3V
<b>Telit GPIOs</b>				
<b>C5</b>	GPIO_01 / DVI_WA0/SIMIN	I/O	Telit GPIO_01 Configurable GPIO/ Digital Audio Interface (WA0)	CMOS 1.8V
<b>RF SECTION</b>				
<b>G2</b>	ANTENNA	I/O	GSM/EDGE/UMTS/LTE Antenna (50 Ohm)	RF
<b>MISCELLANEOUS FUNCTIONS</b>				
<b>G6</b>	VAUX/PWRMON	O	1.8V stabilized output I <sub>max</sub> = 100mA/ Power ON monitor	1.8V
<b>G4</b>	RESET*	I	Reset Input (Active Low)	Connect in Open-Drain
<b>RESERVED</b>				
<b>G5, B6</b>				
<b>GROUND PINS</b>				
<b>D1, F1, G1, D2, F2, C3, E3, F3, G3, F6</b>				



**WARNING:**  
RESERVED pins reported above must not be connected.

**NOTE:**

The internal GPIO pull-up/pull-down could be set to the preferred status for the application using the AT#GPIO command.

Please refer to the AT Commands User Guide for the detailed command syntax.

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**NOTE:**

On NE866 the functions marked with (\*) are not available on early samples and will be supported on future release.

For more information, please refer to the related SW documentation

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## 4.2. PIN-OUT differences

UE866 has 4 rows of pins more than GE866 and NE866; LE866 and ME866 have another row up to row 1 called row 0, see the figures below:

	A	B	C	D	E	F	G
1	C165RTS	C166CTS	TX_AUX	GND	VBATT_PA	GND	GND
2	C166DTR	C166DCD	RX_AUX	GND	VBATT	GND	ANT
3	C167DDR	C125RING	GND	RFU	GND	GND	GND
4	C163TXD	GPIO_06	GPIO_07	USB_VBUS	DAC_OUT	ADC_IN1	RESET*
5	C164RXD	GPIO_05	GPIO_01	GPIO_04	USB_D+	VRTC	RESERVED
6	SIMIO	RESERVED	GPIO_02	GPIO_03	USB_D-	GND	VALXPWR MON
7	SIMCLK	SIMRST	SIMVCC	RESERVED	RESERVED	RESERVED	RESERVED
8	GND	RESERVED	RFU	RFU	RFU	RFU	GND
9	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
10	RESERVED	RESERVED	RESERVED	RESERVED	RFU	RESERVED	RESERVED
11	GND	RESERVED	RESERVED	SPL_MRDY	SPL_BRDY	SPL_CLK	GND

**GE866**

	A	B	C	D	E	F	G
0	RESERVED	GND	DIV ANT	GND	VBATT_PA	GND	GND
1	C165RTS	C166CTS	TX_AUX	GND	VBATT_PA	GND	GND
2	C166DTR	C166DCD	RX_AUX	GND	VBATT	GND	MAIN ANT
3	C167DDR	C125RING	GND	RFU	GND	GND	GND
4	C163TXD	GPIO_06	GPIO_07	RESERVED	DAC_OUT	ADC_IN1	RESET*
5	C164RXD	GPIO_05	GPIO_01	GPIO_04	USB_D+	RESERVED	RESERVED
6	SIMIO	RESERVED	GPIO_02	GPIO_03	USB_D-	GND	VALXPWR MON
7	SIMCLK	SIMRST	SIMVCC	RESERVED	RESERVED	RESERVED	RESERVED
8	GND	RESERVED	RESERVED	VDDIO_IN	PSM_STAT_US	PSM_ENA_OUT	GND
9	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
10	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
11	GND	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	GND

**UE866**

	A	B	C	D	E	F	G
1	RTN* SP_CLK* UC_CLK* GND*	CTS* SP_CLK* UC_CLK* GND*	TX_RXN SP_CLK* UC_CLK* GND*	GND	VBATT	GND	GND
2	RFU	RFU	EX_RXD* SP_CLK* UC_CLK* GND*	GND	VBATT	GND	ANT
3	RFU	RFU	GND	PSM_WAKE UP	GND	GND	GND
4	TRD	RFU	RFU	RFU	RFU	ADC_IN1	RESET*
5	RND	SIM_IN	RFU	RFU	RFU	RFU	SIP_RD
6	SIMIO	RFU	RFU	RFU	RFU	GND	VALXPWR MON
7	SIMCLK	SIMRST	SIMVCC	RFU	RFU	RFU	RFU

**NE866**

**LE866 and ME866**



### WARNING:

In case GE866 or NE866 is mounted don't place solder past on the pins in rows 0 and from 8 to 11; in case UE866 is mounted don't place solder past on row 0.



### NOTE:

In order to have a xE866 compatible design you should use a 12 row footprint.



On LE866 and ME866 pin D8 (VDDIO\_IN) shall be externally connected to VAUX (pin G6), in a xE866 common design pin D8 shall be connected to pin G6.

#### 4.2.1. USB Port

The USB port is present in UE866, ME866 and LE866, on GE866 the USB port is not present but D4, E5 and E6 pins are unconnected so in a xE866 common design the USB connection can be predisposed and used in case UE/LE866 is mounted. The UE866 and LE866 supports High Speed (480Mb/s) mode, for this reason the signal traces should be routed carefully: trace lengths, number of vias and capacitive loading should be minimized and the characteristic impedance value should be as close as possible to 90 Ohms differential.

USB can be used for the following purposes: communication with external peripheral devices, debug monitor.

The following table is listing the available signals:

PIN	SIGNAL	I/O	FUNCTION	TYPE	COMMENT
<b>USB HS 2.0 Communication Port</b>					
<b>E5</b>	USB_D+	I/O	USB differential Data (+)		Unconnected on GE866
<b>E6</b>	USB_D-	I/O	USB differential Data (-)		Unconnected on GE866
<b>D4</b>	VUSB	I	Power sense for the internal USB transceiver.		Unconnected on GE866, LE866 and ME866

VUSB pin is present on UE866. It must be connected to +5V in order to activate the USB port.

For more information about USB port, refer to the Hardware User Guide.



We recommend adding USB PCB connector pads for convenient access for network certification testing, firmware upgrade and module debug logs. The USB connector can be “DNP” until needed. This may be more convenient than just test points alone.

#### 4.2.2. Analog Audio

On GE866 an analog audio front-end port is present, the pinout is indicated in the following table:

PIN	SIGNAL	I/O	FUNCTION	TYPE	COMMENT
<b>Analog Voice Interface</b>					
<b>D7</b>	EAR+	AO	Ear signal output, phase +		
<b>E7</b>	EAR-	AO	Ear signal output, phase +		
<b>F7</b>	MIC+	AI	Microphone signal input; phase +		
<b>G7</b>	MIC-	AI	Microphone signal input; phase -		



On LE866, UE866, ME866 and NE866 the analog audio interface is not present. In a xE866 common design you should use the digital audio interface.

#### 4.2.3. GPIO

On the different xE866 family modems not all the alternate functions are implemented and on NE866 there isn't any available GPIO so in a xE866 global form factor design you should avoid using the GPIO

See table below to verify the Alternate function availability on the various products.

In a xE866 common design you should avoid using the Alternate functions not available in all the products such as JDR, TX Disable, RFTXMON and BUZZER.

PIN	SIGNAL	I/O	FUNCTION	AVAILABILITY
<b>GPIO</b>				
<b>C5</b>	GPIO_01 / DVI_WA0	I/O	Telit GPIO_01 Configurable GPIO/ Digital Audio Interface (WA0)	-
<b>C6</b>	GPIO_02 / JDR / DVI_RX	I/O	Telit GPIO_02 Configurable GPIO/ Jammer Detect Report / Digital Audio Interface (RX)	JDR NOT Available on LE866
<b>D6</b>	GPIO_03 / DVI_TX	I/O	Telit GPIO_03 Configurable GPIO/ Digital Audio Interface (TX)	-
<b>D5</b>	GPIO_04/ TX Disable / DVI_CLK	I/O	Telit GPIO_04 Configurable GPIO/ TX Disable input / Digital Audio Interface (CLK)	TX Disable NOT Available on UE866 and LE866
<b>B5</b>	GPIO_05 / RFTXMON	I/O	Telit GPIO_05 Configurable GPIO/ Transmitter ON monitor	RFTXMON NOT Available on UE866 and LE866
<b>B4</b>	GPIO_06 / ALARM / BUZZER	I/O	Telit GPIO_06 Configurable GPIO/ ALARM / BUZZER	BUZZER NOT Available on UE866 and LE866
<b>C4</b>	GPIO_07 / STAT_LED	I/O	Telit GPIO_07 Configurable GPIO / Status LED	-

#### 4.2.4. SIMIN GPIO Input

On the xE866 modems the SIMIN feature is not bounded to a particular I/O, but instead it can be configured on one of the GPIOs available, provided no other function is used on that I/O. Not all the GPIO are available as SIMIN sources in all products, see table below:

GPIO AVAILABLE FOR SIMIN	
<b>GE866</b>	ALL
<b>UE866</b>	ALL
<b>LE866</b>	ALL
<b>NE866</b>	B5
<b>ME866</b>	ALL

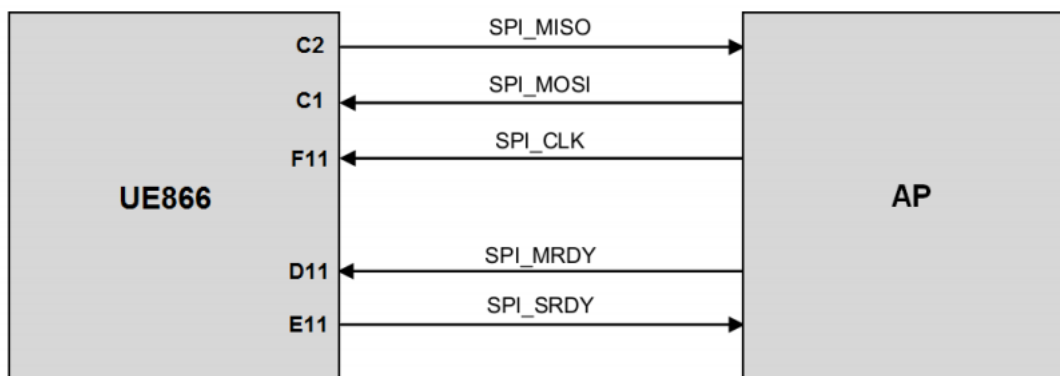
In a xE866 common design you should tie the SIMIN function to B5 (GPIO\_05).

#### 4.2.5. SPI Port

Only UE866 is provided by an SPI hardware interface that shares the hardware resources with the AUX\_UART port. To use either AUX\_UART or SPI an AT port configuration command must be sent. It shall be noted that by default the hardware SPI port of the module differs from the standard SPI. This interface supports two handshake lines for flow control and mutual wake-up: SRDY (slave ready) and MRDY (master ready). The application has the master role, that is, it supplies the clock.

PIN	SIGNAL	I/O	FUNCTION	TYPE	COMMENT
<b>SPI</b>					
<b>C1</b>	SPI_MOSI	I	SPI MOSI	CMOS 1.8V	Shared with TX_AUX
<b>C2</b>	SPI_MISO	O	SPI_MISO	CMOS 1.8V	Shared with RX_AUX
<b>F11</b>	SPI_CLK	I	SPI Clock	CMOS 1.8V	Shared with HSIC_HOST_WAKEUP
<b>D11</b>	SPI_MRDY	I	SPI_MRDY	CMOS 1.8V	Shared with HSIC_SLAVE_WAKEUP

<b>E11</b>	SPI_SRDY	O	SPI_SRDY	CMOS 1.8V	Shared with HSIC_HOST_ACTIVE
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**WARNING:**

In a common xE866 design the SPI port should be not used.



**NOTE:**

Due to shared functions, when the SPI port is used, it's not possible to use the AUX\_UART port.

For more information, see UE866 Hardware User Guide.

#### 4.2.6. Antenna Diversity

On LE866 is included an input for a second RX antenna to improve the radio sensitivity. The function is called Antenna Diversity. In a xE866 common design in order to have the possibility to use the diversity antenna when LE866 is mounted you should route the diversity antenna connection to C0 pad.

PIN	SIGNAL	I/O	FUNCTION	TYPE	COMMENT
<b>RF SECTION</b>					
<b>C0</b>	ANT_DIV	I	Antenna Diversity Input (50 ohm)	RF	



As of dec. 2014, PTCRB updated PPMD document section 11.10.6 Feature/Function Set for Integrated Devices, and in the last revision the Diversity is not anymore among the exception features that may not match the modem capabilities. This means that if the assembled modem supports Diversity antenna, then in order to get PTCRB approval (and subsequent US carrier approval) the application MUST have a diversity antenna.



**NOTE:**  
If the RX Diversity is not used/connected, disable the Diversity functionality using the AT#RXDIV command (ref to the AT User guide for the proper syntax) and leave the pad C0 unconnected.

#### 4.2.7. RTC

The xE866 modems internally provide a real time clock.

On the GE866, UE866 the supply of the RTC is separate from the rest of the digital parts, allowing having only RTC running when all other parts of the device are off. This supply is connected to pin VRTC and a backup capacitor can be added in order to increase the RTC autonomy during power off of the main supply. No devices must be powered from this pin.

The internal RTC on LE866, NE866 and ME866 is powered directly from VBATT, there is no VRTC separate voltage like in the other products of the xE866 family; so in order to keep the RTC running, VBATT should not be removed.

In a xE866 common design, the VRTC pin should not be used and if RTC always running is a requirement then VBATT signal shall be backed up.

PIN	SIGNAL	I/O	FUNCTION	TYPE	COMMENT
<b>RTC</b>					
<b>F5</b>	VRTC	AO	Backup for the embedded RTC supply	-	



**WARNING:**  
In a common xE866 design the VRTC pin should be not used.

## 5. LOGIC LEVEL SPECIFICATIONS

### 5.1. Absolute Maximum Ratings – Not Functional

INPUT LEVEL ON ANY DIGITAL PIN (CMOS 1.8V) WITH RESPECT TO GROUND		
	MIN	MAX
<b>GE866</b>	-0.3V	2.1V
<b>UE866</b>	-0.3V	2.1V
<b>LE866</b>	-0.3V	VDDIO_IN + 0.3V
<b>NE866</b>	-0.3V	2.1V
<b>ME866</b>	-0.3V	VDDIO_IN + 0.3V
<b>LE866 and ME866 when VDDIO is not supplied</b>	-0.3V	0.3V



**NOTE:**

On LE866 VDDIO\_IN shall be within the range 1.7V – 1.9V, hence the MAX voltage on any digital pin for the LE866 is in the range 2.0V – 2.1V.

### 5.2. Operating Range – Interface levels (1.8V CMOS)

	Input High Level		Input Low Level		Output High Level		Output Low Level	
	Min	Max	Min	Max	Min	Max	Min	Max
<b>GE866</b>	1.3V	1.9V	0.0V	0.35V	1.6V	1.9V	0.0V	0.2V
<b>UE866</b>	1.5V	1.9V	0.0V	0.35V	1.6V	1.9V	0.0V	0.2V



<b>LE866</b>	1.5V	1.9V	0.0V	0.35V	1.6V	1.9V	0.0V	0.2V
<b>NE866</b>	1.25 V	1.95 V	0.0V	0.35V	1.4V	1.85V	0.0V	0.2V
<b>ME866</b>	1.55 V	1.9V	0.0V	0.35V	1.35V	1.8V	0.0V	0.8V

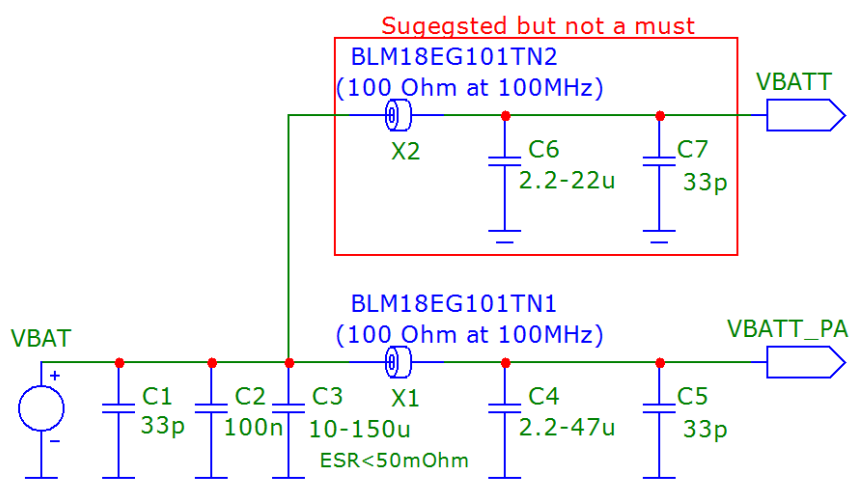
### 5.3. Current characteristic

	OUTPUT CURRENT	INPUT CURRENT
<b>GE866</b>	1mA	1 $\mu$ A
<b>UE866</b>	1mA	1 $\mu$ A
<b>LE866</b>	1mA	1 $\mu$ A
<b>NE866</b>	1mA	TBC
<b>ME866</b>	1mA	10 $\mu$ A

## 6. POWER SUPPLY

The power supply circuitry and board layout are a very important part in the full product design and they strongly reflect on the product overall performances, hence read carefully the requirements and the guidelines that will follow for a proper design.

To improve EMI filtering an EMI suppression circuitry must be added on modem's VBATT\_PA, and if possible also on VBATT. Follow schematic on figure below.



### 6.1. Power Supply Requirements

The external power supply must be connected to VBATT & VBATT\_PA signals and must fulfill the following requirements:

	NOMINAL SUPPLY VOLTAGE	NORMAL OPERATING VOLTAGE RANGE	EXTENDED OPERATING VOLTAGE RANGE
<b>GE866</b>	3.8V	3.40V - 4.20V	3.10V* - 4.50V
<b>UE866</b>	3.8V	3.40V - 4.20V	3.10V* - 4.50V
<b>LE866</b>	3.8V	3.40V - 4.20V	3.10V - 4.50V
<b>NE866</b>	3.8V	3.40V - 4.20V	3.10V - 4.20V
<b>LE866</b>	3.8V	3.40V - 4.20V	3.10V - 4.50V



\*On UE866 and GE866 the Power supply must be higher than 3.22 V to power on the module, when the module is ON the voltage level on VBATT can go to 3.1V.



The Operating Voltage Range MUST never be exceeded; care must be taken in order to fulfil min/max voltage requirement.



Overshoot voltage (regarding MAX Extended Operating Voltage) and drop in voltage (regarding MIN Extended Operating Voltage) MUST never be exceeded;  
The “Extended Operating Voltage Range” can be used only with completely assumption and application of the HW User guide suggestions.



The electrical design for the Power supply should be made ensuring it will be capable of a peak current output of at least 2 A.



For a xE866 common design the voltage level of the power supply should stay in the **Normal Operating voltage Rate**.



In order to avoid latch-up issues we recommend particular care be taken such that no digital pins connected to the modem of the modem remain high when the modem is turned off.

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## 7. DAC AND ADC

### 7.1. ADC

On GE866, UE866 and LE866 is available an ADC input useful mainly for antenna detection purposes (pin F4). The following table is showing the ADC characteristics for the GE866, UE866 and LE866:

MODULE	Input Voltage range		AD conversion	Resolution	Input Resistance
	MIN	MAX	BIT	MAX	MIN
GE866	0.0V	1.2V	10	1.17mV	1MΩ
UE866	0.0V	1.2V	10	1.17mV	1MΩ
LE866	0.0V	1.0V	10	1mV	1MΩ
NE866	0.0V	1.45V	10	1mV	1MΩ
ME866	0.0V	1.0V	10	1mV	TBC

### 7.2. DAC

The GE866, UE866 and LE866 provides a Digital to Analog Converter. The signal (named DAC\_OUT) is available on pin E4.

The on board DAC is a 10 bit converter, able to generate an analogue value based on a specific input in the range from 0 up to 1023. However, an external low-pass filter is necessary

The following table is showing the DAC characteristics that are the same for all the xE866 modules:

	MIN	MAX	UNIT
Voltage range (filtered)	0	1.8	Volt
Range	0	1023	Steps

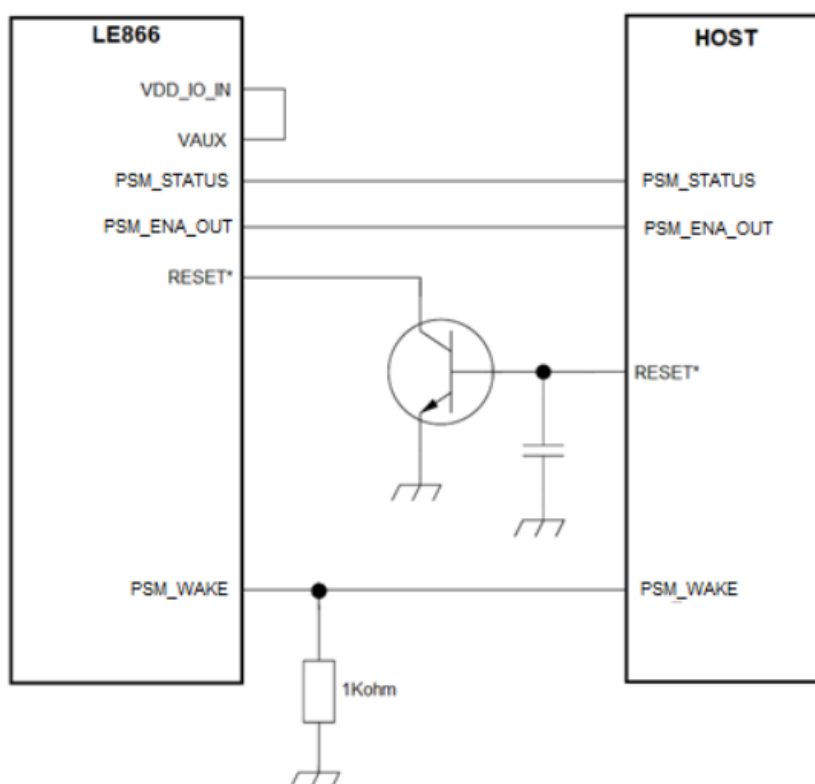
For more information see the DAC Converter chapter on xE866 Hardware User Guides.

## 8. PSM MODE

The LE866, ME866 and NE866 include unique advanced features in order to support the PSM according to 3GPP Rel-12 for this purpose the LE866 and ME866 have 3 dedicated pins, NE866 instead use only PSM\_WAKE (D3) and SPL\_IND (G5), for more information see the relative PSM Application note.

PIN	SIGNAL	I/O	FUNCTION	TYPE
D3	PSM_WAKE	I	WAKE UP FROM PSM MODE	ANALOG
E8	PSM_STATUS	O	PSM STATUS	CMOS 1.8V
F8	PSM_ENA_OUT	O	PSM ENABLE FOR EXTERNAL LDO	CMOS 1.8V

On GE866 and UE866 those pins are internally unconnected so in a xE866 family common design you can predispose the interconnections in order to have the possibility to use the PSM features when the LE866 or ME866 is mounted:





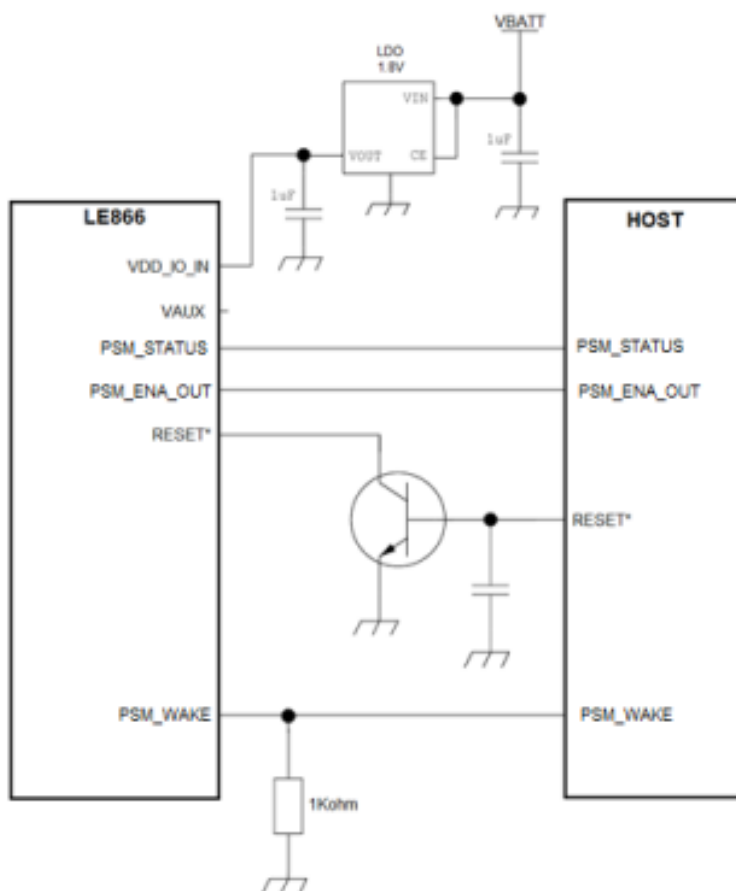
**NOTE:**

VDDIO\_IN can be directly supplied from VAUX\_PWRMON line (adding an R0 in series for debug purposes)

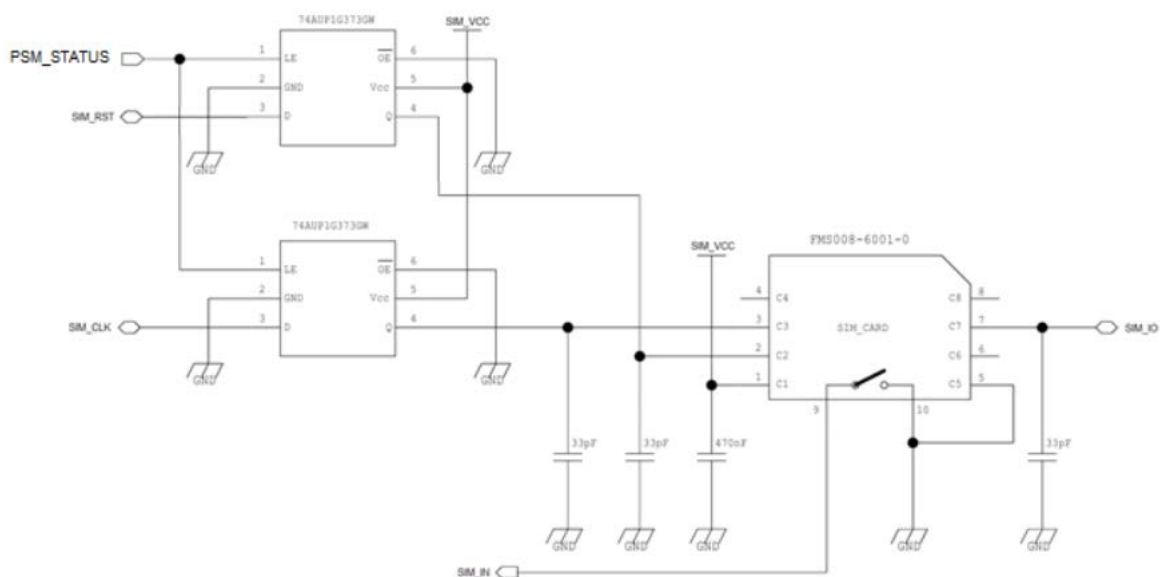


**NOTE:**

If VDDIO\_IN line is not powered (i.e. during the sleep states in PSM=2 when supplied by VAUX, during transition phases BOOT, RESET etc. and when the module is unsupplied) it is important to avoid back powering the digital pins. Exceeding the absolute maximum ratings could damage permanently the module.



Be aware that in order to have the possibility to use the PSM features, when the LE866 is mounted, you need also to predispose two latches on the SIM\_RST and SIM\_CLK lines as indicated in figure below:



For more information refer to the document “LE866 PSM APPLICATION NOTE”.

## 9. DOCUMENT HISTORY

Revision	Date	Changes
0	2014-11-05	First issue
1	2015-06-24	Added LE866
2	2017-01-02	New document layout New note in 4.2 New chapter 8 New Paragraphs 4.2.3 and 4.2.6 Fix the PIN number, in Chapter 4.1
3	2017-04-18	Added NE866 and ME866





# SUPPORT INQUIRIES

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