WE866E4-P Module Hardware User Guide

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Contents

Chapter 1 Introduction

1.1 Scope

The aim of this document is to describe the hardware solutions useful for developing a product with Telit WE866E4-P module.

1.2 Audience

This document is intended for Telit customers, who are integrators, about to implement their applications using our WE866E4-P modules.

1.3 Contact Information, Support

For general contact, technical support services, technical questions and report documentation errors contact Telit Technical Support at:

- TS-SRD@telit.com

Alternatively, use:

http://www.telit.com/support

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

http://www.telit.com

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

1.4 Text Convention

The following table shows the symbol conventions used in this manual for notification and important instructions.

Table 1 Symbol Conventions

Icon	Type	Description
	Note	Provides helpful suggestions needed in understanding a feature or references to material not available in the manual.
	Alert	Alerts you of potential damage to a program, device, or system or the loss of data or service.
	Caution	Cautions you about a situation that could result in minor or moderate bodily injury if not avoided.
	Warning	Warns you of a potential situation that could result in death or serious bodily injury if not avoided.
	Electro-Static Discharge (ESD)	Notifies you to take proper grounding precautions before handling a product.
	Danger	Indicates information MUST be followed or catastrophic equipment failure or bodily injury may occur

All dates are in ISO 8601 format, i.e. YYYY-MM-DD

1.5 Related Documents

Please refer to http://www.telit.com/gnss/ for current documentation and downloads.

1.5.1 Related Documents and Download

- Datasheets
- Product User Guides
- EVK User Guides
- Software User Guides
- Application Notes
- TelitView installation and documentation

1.5.2 Related Documents requiring a Non Disclosure Agreement

- Authorized Software User Guides
- Product firmware

Chapter 2 Overview

The aim of this document is to describe some hardware solutions useful for developing a product with Telit WE866E4-P module. All the basic functions of a mobile phone is considered and certified for an appropriate hardware solution, common errors and wrong solution that can be avoided are documented. The wrong solutions to be avoided shall be considered as mandatory, while the suggested hardware configurations shall not be considered mandatory, instead the information given shall be used as a guide and a starting point for proper development of a product with the Telit WE866E4-P module.

For further hardware details refer to the "*Telit WE866E4-P Product Description*" document where all the hardware information is reported.

NOTE:
1).(EN) The integration of WE866E4-P WiFi+BT module within user application shall be done according to the design rules describe in this manual.
2).(IT)
3).(DE)
4).(SL)
5).(FR)
6).(HE)

Chapter 3 Pin Allocation

3.1 Pins Out

Table 2, page 13 describes the WE866E4-P module pin signal description.

Table 2 WE866E4-P Module Pin Signal Description

Pins	Name	Input/Output	Function	Type	Comments
USB HS 2.0 COMMUNICATION PORT					
E5	USB_D+	Input/Output	USB differential Data+		
E6	USB_D-	Input/Output	USB differential Data -		
E4	VUSB	Input	Power sense for USB		
High Speed Asynchronous Serial Port (USIF0)					
A4	UART0_TXD	Output	Serial data output	CMOS VIO	
A5	UART0_RXD	Input	Serial data input	CMOS VIO	
B4	UART0_RTS	Output	Output	CMOS VIO	
B3	UART0_CTS	Input	Input	CMOS VIO	
Low Speed Asynchronous Serial Port (USIF0)					
C3	UART1_RXD	Input	Serial data input	CMOS VIO	
C4	UART1_TXD	Output	Serial data input	CMOS VIO	
Serial Peripheral Interface (SPI) CMOS VIO					
A3	SPI_MISO	Input	Pull-down (see Note 1)	CMOS VIO	Master
B2	SPI_MOSI	Output	Pull-down (see Note 1)	CMOS VIO	Master
A2	SPI_CLK	Output	Pull-down (see Note 1)	CMOS VIO	Master
D9	SPI_CS	Output	Pull-down	CMOS VIO	Master
Secure Digital Input Output (SDIO)					
A6	SDIO_D2	Input/Output	DATA2	CMOS VIO	
B6	SDIO_D1	Input/Output	DATA1	CMOS VIO	
B7	SDIO_D3	Input/Output	DATA3	CMOS VIO	
C7	SDIO_D0	Input/Output	DATA0	CMOS VIO	
D7	SDIO_CLK	Input/Output	Clock	CMOS VIO	
E7	SDIO_CMD	Input/Output	Command	CMOS VIO	
Inter - Integrated Circuit Interface					

Table 2 WE866E4-P Module Pin Signal Description (Continued)

Pins	Name	Input/Output	Function	Type	Comments
F8	I2C_SDA	Input/Output	Data	CMOS VIO	GP IO_6
G8	I2C_SCL	Input/Output	Clock	CMOS VIO	GPIO_7
Analog Interface					
A8	ADC_IN1	Input	12 BITS 1Mhz	VIO	1V8 only
A9	ADC_IN2	Input	12 BITS 1Mhz	VIO	1V8 only
B9	ADC_IN3	Input	12 BITS 1Mhz	VIO	1V8 only
Digital Audio Interface (I2S) Master/Slave					
C5	I2S_SYNC	Input/Output	Synchronization	CMOS VIO	
D5	I2S_SCK	Input/Output	Clock	CMOS VIO	
C6	I2S_SDI	Input	Input Data	CMOS VIO	
D6	I2S_SDO	Output	Output Data	CMOS VIO	
Miscellaneous Functions					
G5	WiFI_EN	Input	Power Enable	CMOS VIO	Active HI
G6	BT_EN	Input	Power Enable	CMOS VIO	Active HI
D1	ANT_1	Input/Output	Wi-Fi 2.4G and 5G	RF	50Ohms
G3	ANT_2	Input/Output	BT 2.4G	CMOS VIO	50Ohms
D3	GPIO_1	Input/Output	GENERIC IO	CMOS VIO	WAKEUP
E3	GPIO_2	Input/Output	GENERIC IO	CMOS VIO	BT_PRIORITY
F5	GPIO_3	Input/Output	GENERIC IO	CMOS VIO	WI-FI ACTIVE
F6	GPIO_4	Input/Output	GENERIC IO	CMOS VIO	BT_ACTIVE
F7	GPIO_5	Input/Output	GENERIC IO	CMOS VIO	DAC_OUT
Power Supply					
A1	VDD_BLE	Input	Main BLE Power Supply	Power	
A2	VDD_WLAN	Input	Main Wi-Fi Power Supply	Power	
A3	VIO	Input	Digital I/O Power Supply	Power	
B1	GND		Ground	Power	
B2	GND		Ground	Power	
C1	GND		Ground	Power	
C2	GND		Ground	Power	
D2	GND		Ground	Power	
E1	GND		Ground	Power	
E2	GND		Ground	Power	
F1	GND		Ground	Power	
F2	GND		Ground	Power	
F3	GND		Ground	Power	

Table 2 WE866E4-P Module Pin Signal Description (Continued)

Pins	Name	Input/Output	Function	Type	Comments
F4	GND		Ground	Power	
G1	GND		Ground	Power	
G2	GND		Ground	Power	
G4	GND		Ground	Power	
G7	GND		Ground	Power	
A7	GND		Ground	Power	
C9	GND		Ground	Power	
Reversed					
B5	RESERVED		RESERVED		
D4	RESERVED		RESERVED		

3.2 A Pad Layout

The following representation shows the top view of the Pad layout:

	A	B	C	D	E	F	G
1	VDD_BLE	GND	GND	ANT_1	GND	GND	GND
2	VDD_WLAN	GND	GND	GND	GND	GND	GND
3	VIO	UART0_CTS	UART1_RX	GPIO_1 WAKEUP	GPIO_2 BT_PRIORITY	GND	ANT_2
4	UART0_TXD	UART0_RTS	UART_TX	RES	USB_VDD	GND	GND
5	UART0_RX	RES	I2S_SYNC	I2S_SCK	USB_DP	GPIO_3 Wi-Fi Active	WiFi_EN
6	SDIO_D2	SDIO_D1	I2S_SDI	I2S_SDO	USB_DM	GPIO_4 BT_ACTIVE	BT_EN
7	GND	SDIO_D3 SPI_MOSI UART0_RTS	SDIO_D0 SPI_MISO UART0_RXD	SDIO_CLK SPI_CLK UART0_CTS	SDIO_CMD SPI_CS UART0_TXD	GPIO_5 DAC_OUT1	GND
8	ADC_IN1	JTAG_TCK	JTAG_TD0	JTAG_TMS	JTAG_TDI	GPIO_6 I2C_SDA	GPIO_7 I2C_SCL
9	ADC_IN2	ADC_IN3	GND	SPI_CS (MASTER) GPIO	SPI_CLK (MASTER) GPIO	SPI_MOSI (MASTER) GPIO	SPI_MISO (MASTER) GPIO

Chapter 4 Power Supply

4.1 Power Supply Requirements

Table 3, page 17 provide the Power supply requirements of WE866E4-P module.

Table 3 Power Supply Requirements

Power Supply	Minimum	Typical	Maximum
Absolute Maximum to avoid permanent damage at any power supply pin	-0.3V		4.0V
Recommended-VDD_BLE, VDD_WLAN, USB_VDD	3.14V	3.3V	3.46V
Recommended VIO	3.14/1.71V	3.3V/1.8V	3.46V/1.86V
Note: The ADC cannot be used if VIO is not equal to 1V8.			

4.2 Power Consumption

Table 4, page 17 lists the types of Power Consumption.

Table 4 Power Consumption

Power Consumption	Typical
POWER DOWN WiFi_EN=0, BT_EN=0	TBD µA
Suspend	TBD µA
Host OFF	TBD µA
Sleep	TBD µA
ON; Radio OFF	TBD mA
BLE RX	TBD mA
BLE TX	TBD mA
WiFi RX	TBD mA
WiFi TX	TBD mA

Table 4 Power Consumption

Power Consumption	Typical
DTIM=1	TBD mA
DTIM=3	TBD µA
DTIM=10	TBD µA

4.3 General Design Rules

It is recommended to provide a 10µF capacitors right next to the VDD_WLAN and BT pins, and 2.2µF at each of the other power supply pins like VIO.

Chapter 5 Digital Section

5.1 Logic Levels

Table 5, page 19 describes the logic level of the voltage between signal and ground.

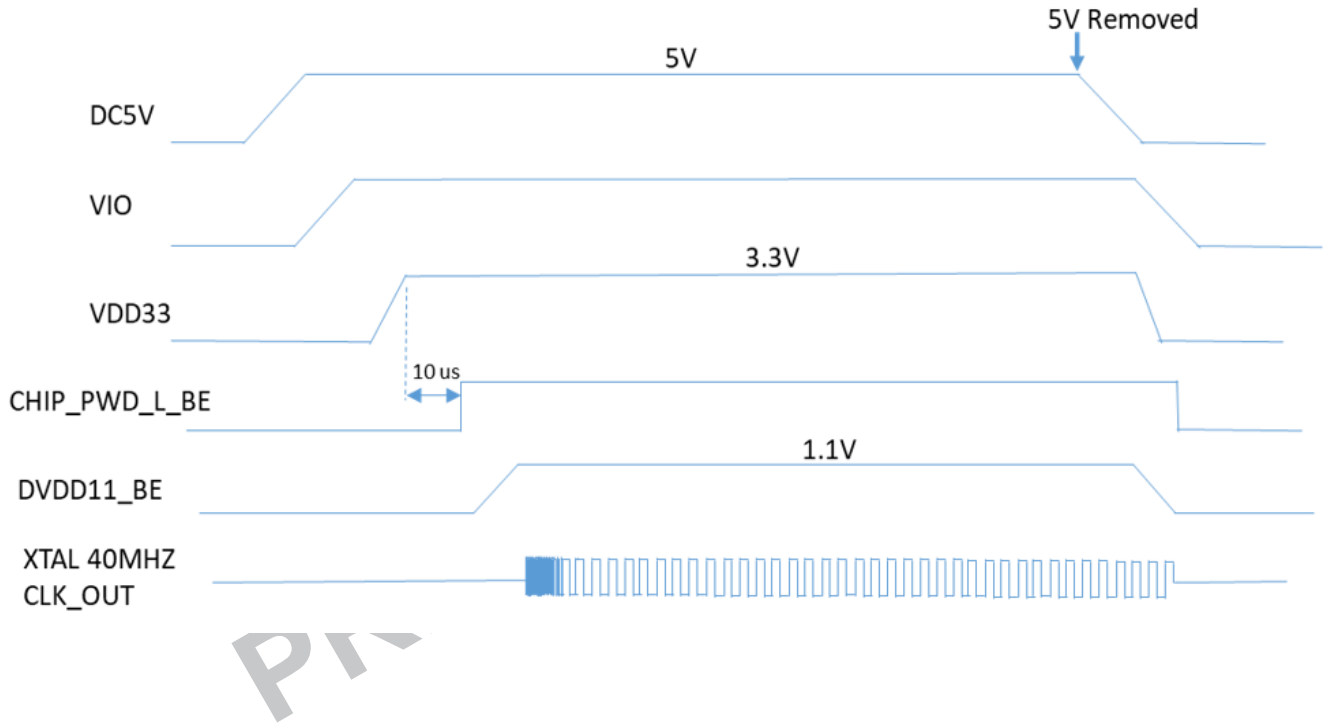
Table 5 Logic Level

Parameter	Minimum	Maximum
Input level on any digital pin	-0.3V	VIO + 0.3V
Levels with VIO = 3.3V		
V_{IH} Input high level	2.4V	3.6V
V_{IL} Input low level	-0.3V	0.3V
V_{OH} Output high level	3.0V	3.6V
V_{OL} Output high level	-0.3V	0.4V
Levels with VIO = 3.3.V	**Typical**	
I_{IH} Input current	60 µA (Rod is ON) 0.1 µA (Rpd is OFF)	
I_{IL} Input current	60 µA (Rod is ON) 0.1 µA (Rpd is OFF)	
I_{OH} Output current	5mA (x4 drive strength) 3.3mA (x2 drive strength) 2.6(x1 drive strength)	
I_{OL} Output current	5mA (x4 drive strength) 3.3mA (x2 drive strength) 2.6(x1 drive strength)	
Note: The ADC cannot be used if VIO is not equal to 1V8.		

5.2 Power Up/Down Sequence

The BT_EN is the main power enable pin including the WIFI_EN. All supplies should be stable for a minimum of 10 µs before BT_EN is de-asserted (i.e, greater than VIL for VIO). If VIO = 3.3V, then VDD_BLE, VDD_WLAN, and VIO shares the same 3.3V power (see Figure 1, page 20).

Figure 1 Power Up/Down Sequence



5.3 Power ON Reset Time

Table 6, page 20 describes the Power ON reset time.

Table 6 Power ON Reset Time

Parameter	Description	Minimum	Maximum	Units
tR	Rise time of poweer to 90% of final voltage	N/A	25	ms
tS	Minimum of 10 uS before BLE_EN is asserted	10	N/A	µs

5.4 Unconditional Shutdown

The BT_EN is used for unconditional shutdown.

5.5 Communication Ports

5.5.1 High Speed UART

High-speed Universal Asynchronous Receiver/Transmitter (UART) interfaces is configured to serve either as a host interface link or a debug message console.

Two HS UART interfaces are present, one with dedicated pin out and second sharing the pins with the SDIO interface pins.

Table 7, page 21 describes the High Speed UART Configuration for WE866E4-P.

Table 7 High Speed UART Configuration

Property	Configuration
Baudrate	115200 bps, no auto-baud rate detection, can be changed by the host up to 3 Mbps using a special command
Data Bits	8-Bits
Flow Control	CTS/RTS
Parity	None
Stop Bits	1
Bit Order	LS Bit First

5.5.2 Low Speed UART

High-speed Universal Asynchronous Receiver/Transmitter (UART) interfaces is configured to serve either as debug port.

Table 8, page 21 describes the Low Speed UART Configuration for WE866E4-P.

Table 8 Low Speed UART Configuration

Property	Configuration
Baudrate	Up to 115200 bps, no auto-baud rate detection, debug port
Data Bits	8-Bits
Flow Control	CTS/RTS
Parity	None
Stop Bits	1
Bit Order	LS Bit First

5.5.3 SDIO

One SDIO Slave interface.

- Compliant to SDIO v2.0 specification
- Interface clock frequency up to 48 MHz
- Data transfer modes: 4-bit SDIO, 1-bit SDIO, SPI

5.5.4 SPI

The two general-purpose SPI interfaces are one configured as dedicated master and the other configured as master/slave pin-mux with SDIO interface pins.

- Interface clock frequency up to 48 MHz

5.5.5 I2C

The I2C Master/Salve interface have weak internal processing unit. So add external processing unit of 4.7K down to 1K, if needed.

5.5.6 USB

USB 2.0 device interface, provide a simplified, high-speed and scalable manufacturing test and configuration for QCA4020-based systems.

5.6 General Purpose Input/Output

It is a special signaling GPIO.

5.6.1 ADC Converter

Analog to Digital Converter (ADC) measurements for inputs:

- 12-bit ADC up to 1Msps
- Alternatively 1 differential input, -1.75V to +1.75V, common mode 0.875V

Chapter 6 RF Section

6.1 RF Variants

6.1.1 Wi-Fi

Table 9, page 23 describes the Wi-Fi RF Frequency band.

Table 9 Wi-Fi Frequency Band

RF Frequency	Channel	Range	Units
2.4GHz RF Frequency range	Center channel frequency at 5MHz spacing	2.412 ≤ Fc ≤ 2.484	GHz
5GHz RF Frequency range	Center channel frequency at 5MHz spacing	4.9 ≤ Fc ≤ 5.925	GHz

6.1.2 Bluetooth

Table 10, page 23 describes the Bluetooth RF Frequency band.

Table 10 Wi-Fi Frequency Band

RF Frequency	Channel	Range	Units
RF Frequency range	Fc=2402 + k × 2 MHz, where k = 0, ..., 39	2.4 ≤ F ≤ 2.4835.	GHz

6.2 TX Output Power

6.2.1 Wi-Fi

6.2.1.1 For 2.4GHz

Table 11, page 24 lists the Wi-Fi RF Frequency Transmission for 2.4GHz.

Table 11 Wi-Fi RF Frequency Transmission for 2.4GHZ

Standard	Modulation	Data rates	2.4 GHz: Transmit power with IEEE 802.11 EVM and spectral mask compliance at balun output at 25 °			
		Index	802.11b/g	802.11n 20 MHz	802.11n 40 MHz	Unit
			Typ	Typ	Typ	
802.11b	BPSK	1 Mbps	19	NA	NA	dBm
	QPSK	2 Mbps	19	NA	NA	dBm
	CCK	5.5 Mbps	19	NA	NA	dBm
	CCK	11 Mbps	19	NA	NA	dBm
802.11g	BPSK	6 Mbps	19	NA	NA	dBm
	BPSK	9 Mbps	19	NA	NA	dBm
	QPSK	12 Mbps	19	NA	NA	dBm
	QPSK	18 Mbps	18	NA	NA	dBm
	16 QAM	24 Mbps	18	NA	NA	dBm
	16 QAM	36 Mbps	18	NA	NA	dBm
	64 QAM	48 Mbps	18	NA	NA	dBm
	64 QAM	54 Mbps	18	NA	NA	dBm
802.11n	BPSK	MCS0	NA	19	18	dBm
	QPSK	MCS1	NA	19	18	dBm
	QPSK	MCS2	NA	19	18	dBm
	16 QAM	MCS3	NA	18	18	dBm
	16 QAM	MCS4	NA	18	18	dBm
	64 QAM	MCS5	NA	17	17	dBm
	64 QAM	MCS6	NA	17	17	dBm
	64 QAM	MCS7	NA	17	17	dBm
Note: The performance includes balun, but excludes external duplexer, filter and external switch loss.						

6.2.1.2 For 5GHz

Table 12, page 25 lists the Wi-Fi RF Frequency Transmission for 5GHz.

Table 12 Wi-Fi RF Frequency Transmission for 5GHZ

Standard	Modulation	Data rates	2.4 GHz: Transmit power with IEEE 802.11 EVM and spectral mask compliance at balun output at 25 ° Degrees			
		Index	802.11b/g	802.11n 20 MHz	802.11n 40 MHz	Unit
			Typ	Typ	Typ	
802.11b	BPSK	6 Mbps	16	NA	NA	dBm
	BPSK	9 Mbps	16	NA	NA	dBm
	QPSK	12 Mbps	16	NA	NA	dBm
	QPSK	18 Mbps	16	NA	NA	dBm
	16 QAM	24 Mbps	16	NA	NA	dBm
	16 QAM	36 Mbps	14	NA	NA	dBm
	64 QAM	48 Mbps	13	NA	NA	dBm
	64 QAM	54 Mbps	13	NA	NA	dBm
802.11g	BPSK	6 Mbps	19	NA	NA	dBm
	BPSK	9 Mbps	19	NA	NA	dBm
	QPSK	12 Mbps	19	NA	NA	dBm
	QPSK	18 Mbps	18	NA	NA	dBm
	16 QAM	24 Mbps	18	NA	NA	dBm
	16 QAM	36 Mbps	18	NA	NA	dBm
	64 QAM	48 Mbps	18	NA	NA	dBm
	64 QAM	54 Mbps	18	NA	NA	dBm
802.11n	BPSK	MCS0	NA	16	15	dBm
	QPSK	MCS1	NA	16	15	dBm
	QPSK	MCS2	NA	15	14	dBm
	16 QAM	MCS3	NA	15	14	dBm
	16 QAM	MCS4	NA	14	13	dBm
	64 QAM	MCS5	NA	14	13	dBm
	64 QAM	MCS6	NA	13	12	dBm
	64 QAM	MCS7	NA	13	12	dBm
Note: The performance includes balun, but excludes external duplexer, filter and external switch loss.						

6.2.2 Bluetooth

Table 13, page 26 lists the Bluetooth Transmission.

Table 13 Bluetooth Transmission

TX Characteristic	Rate	Min	Type	Max	Units
Max RF Output Power	LE 1M	1.5	4	4.3	dBm
	LE 2M	1.5	4	4.2	dBm
Note: 1).Measurement data is at chip output, 25°C, 1.8V IO. 2).When Tx power higher than 4dBm, an external BPF is required for out of band emission. BPF spec is upon the external PA is selected.					

6.3 RX Sensitivity

6.3.1 Wi-Fi

6.3.1.1 For 2.4GHz

Table 14, page 26 lists the RX Sensitivity for 2.4GHz.

Table 14 RX Sensitivity for 2.4GHZ

Standard	Modulation	Data rates	2.4 GHz: Transmit power with IEEE 802.11 EVM and spectral mask compliance at balun output at 25 °Degrees			
		Index	802.11b/g	802.11n 20 MHz	802.11n 40 MHz	Unit
			Typ	Typ	Typ	
802.11b	BPSK	1 Mbps	19	NA	NA	dBm
	QPSK	2 Mbps	19	NA	NA	dBm
	CCK	5.5 Mbps	19	NA	NA	dBm
	CCK	11 Mbps	19	NA	NA	dBm
802.11g	BPSK	6 Mbps	19	NA	NA	dBm
	BPSK	9 Mbps	19	NA	NA	dBm
Note: The performance includes balun, but excludes external duplexer, filter and external switch loss.						

6.3.1.2 For 5GHz

Table 15, page 27 lists the RX Sensitivity for 5GHz.

Table 15 RX Sensitivity for 5GHZ

Standard	Modulation	Data rates	2.4 GHz: Transmit power with IEEE 802.11 EVM and spectral mask compliance at balun output at 25 °			
		Index	802.11b/g	802.11n 20 MHz	802.11n 40 MHz	Unit
			Typ	Typ	Typ	
802.11b	BPSK	6 Mbps	-93	NA	NA	dBm
	64 QAM	54 Mbps	-75.5	NA	NA	dBm
802.11g	BPSK	MCS0	NA	-93	-90	dBm
	64 QAM	MCS7	NA	-72.5	-69	dBm
Note: The performance includes balun, but excludes external duplexer, filter and external switch loss.						

6.3.2 Bluetooth

Table 16, page 27 lists the Bluetooth RX Sensitivity.

Table 16 Bluetooth RX Sensitivity

RX Characteristic	Rate	Min	Type	Max	Units
RX Sensitivity	1Mbps	<-= -70dBM	-97	-99	dBm
Note: Measurement data is at chip output, 25°C, 1.8V IO.					

6.4 Wi-Fi Antenna Requirements

Special care must be taken during the design of the RF section on the application board.

CAUTION! *: If The below recommendation is strictly not followed then RF performance degradation and infringements of emission limits will occur*

A 50Ω antenna is required with Telit's WE866E4-P module interface features an SMA connector for an external antenna, alternatively a chip or a printed antenna can be used.

If an integrated or printed antenna is used, it is recommended to place it at the edge of the application board. Since the antenna impedance is required to be tuned to 50Ω.

It is recommended to foresee a PI matching network between the WE866E4-P module and the antenna during first prototyping. If not, a series 0Ω-resistor can be used, leaving the two shunt components unpopulated.

To meet Telit's FCC certification standard, the antenna on the application board should have a gain value equal/less then the one recommended by Telit.

6.4.1 PCB Design Guidelines

The WE866E4-P module provides a 50Ω antenna pad, which is routed to the antenna connector (or the integrated antenna) by means of a transmission line.

It is important that the impedance of this line is controlled to 50Ω. The line should be as short as possible with a constant cross section and without abrupt curves. It is isolated from any other noise sources and cross overs from other lines in adjacent layers. Instead, a continuous ground plane is recommended under the antenna trace and a ground via curtain should connect to the coplanar ground planes.

An example of implementation - the details of the antenna trace on the WE866E4-P interface board is as described:

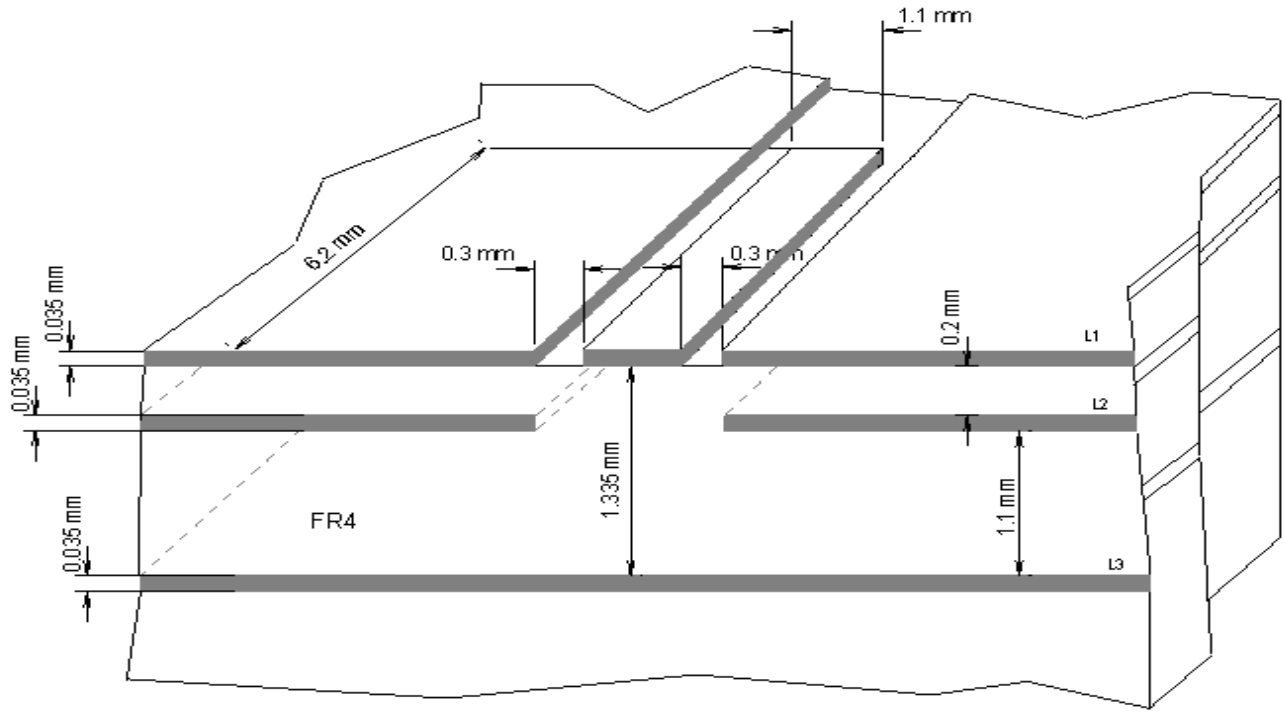
A Grounded Coplanar Waveguide (G-CPW) line has been chosen, since this kind of transmission line ensures good impedance control and can be implemented in an outer PCB layer as required in this case. A SMA female connector has been used to feed the line.

The interface board is realized on a FR4, 4-layers PCB. Substrate material is characterized by relative permittivity εr = 4.6 ± 0.4 @ 1 GHz, TanD= 0.019 ÷ 0.026 @ 1 GHz.

A characteristic impedance of nearly 50 Ω is achieved using trace width of 1.1 mm, clearance from coplanar ground plane = 0.3 mm each side. The line uses reference ground plane on layer 3, while copper is removed from layer 2 underneath the line. Height of the trace above ground plane is 1.335 mm. Calculated characteristic impedance is 51.6 Ω, estimated line loss is less than 0.1 dB.

Figure 2, page 28 shows the line geometry:

Figure 2 PCB Design



6.4.2 PCB Guidelines in case of FCC Certification

TBD

6.5 BlueTooth Antenna Requirements

6.5.1 PCB Design Guidelines

TBD

6.5.2 PCB Guidelines in case of FCC Certification

TBD

Chapter 7 Audio Section

7.1 Electrical Characteristics

The audio interface is only digital, through the I2S.The voltage of this interface pins have same electrical characteristics as for digital pins and are related to the power bank VIO.

7.2 Codec Examples

TBD

Chapter 8 Mechanical Design

8.1 Drawing

Figure 3, page 33 shows the Mechanical Design of the module.

Figure 3 Mechanical Design

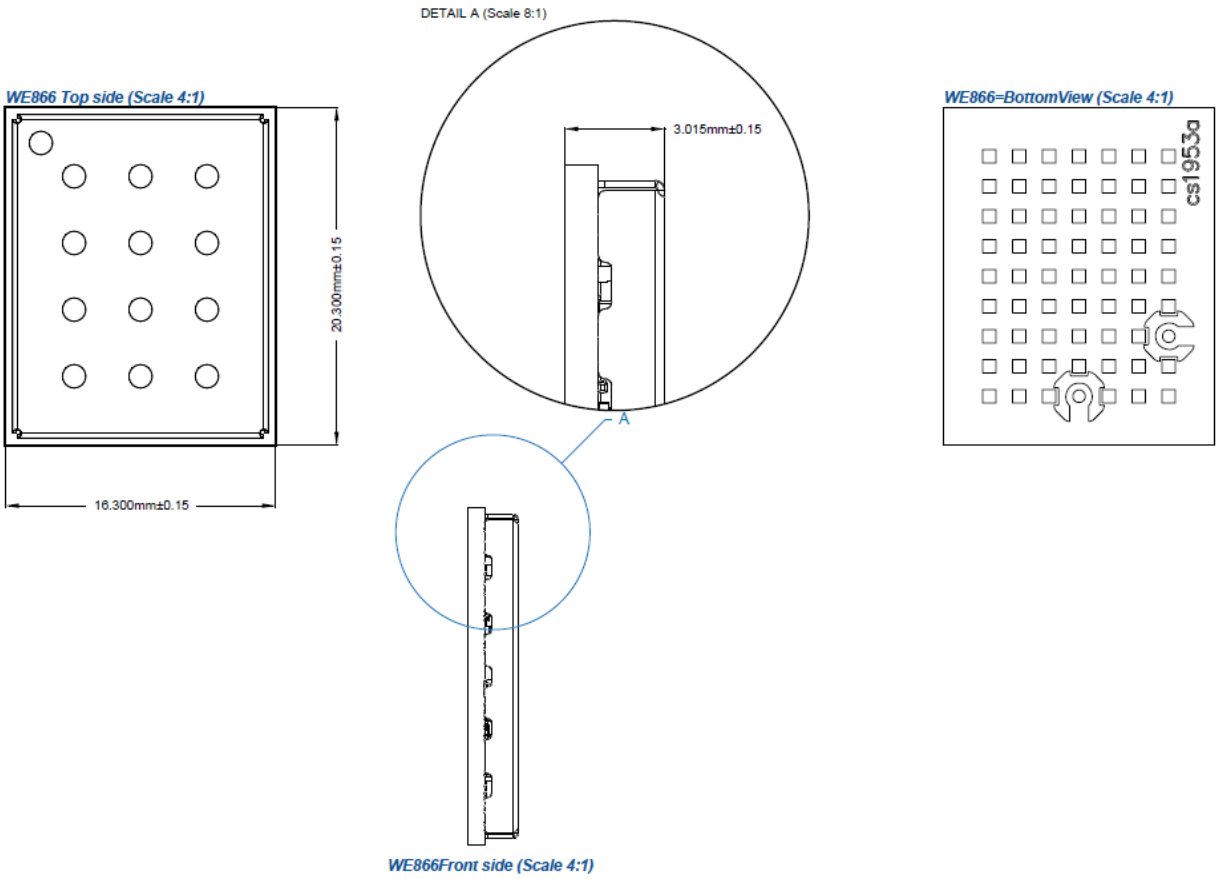
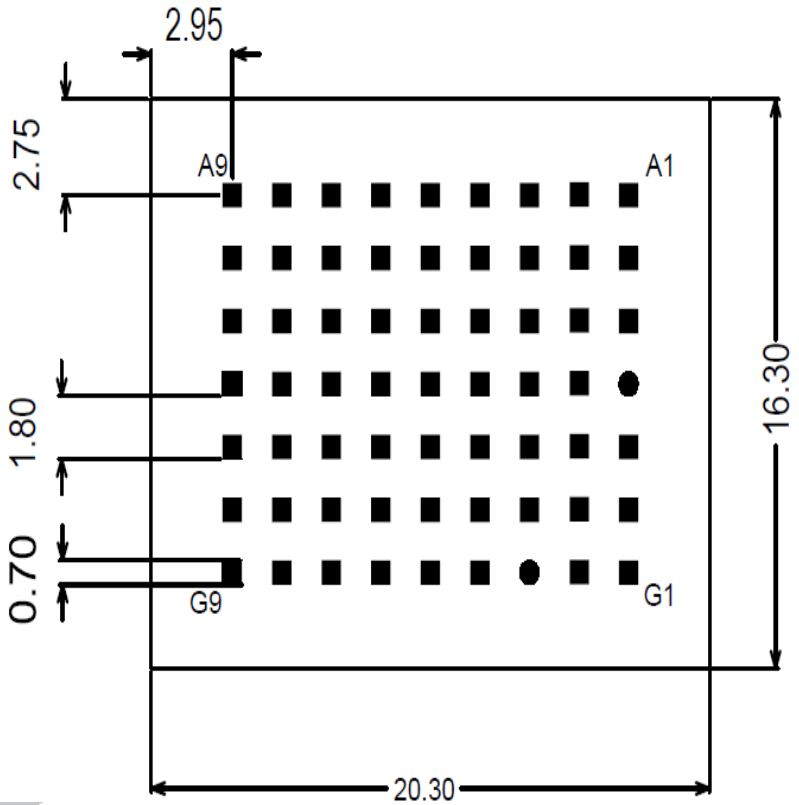


Figure 4, page 34 shows the Top View of WE866E4-P module.

Figure 4 Top View of WE866E4-P Module



Chapter 9 Application PCB Design.

9.1 Footprint

Figure 5, page 35 shows the top view Footprint of copper pad pattern.

Figure 5 Copper pad Pattern - Top View

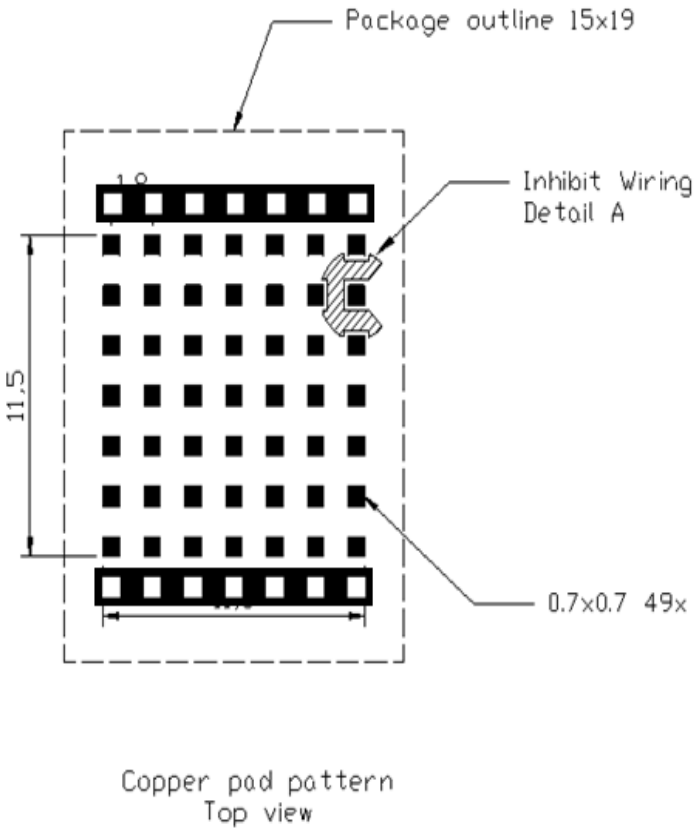


Figure 6, page 36 shows the Pad A details.

Figure 6 Pad A Details

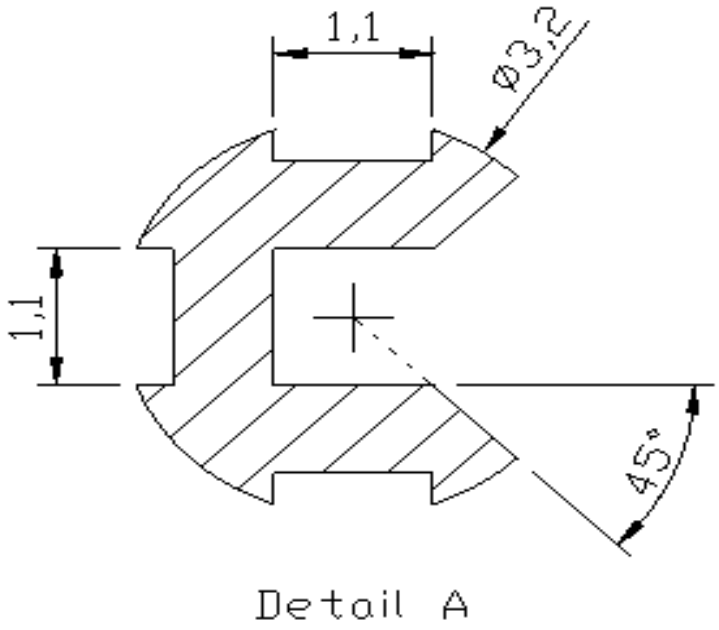


Figure 7, page 36 shows the Pad details.

Figure 7 Pad Details

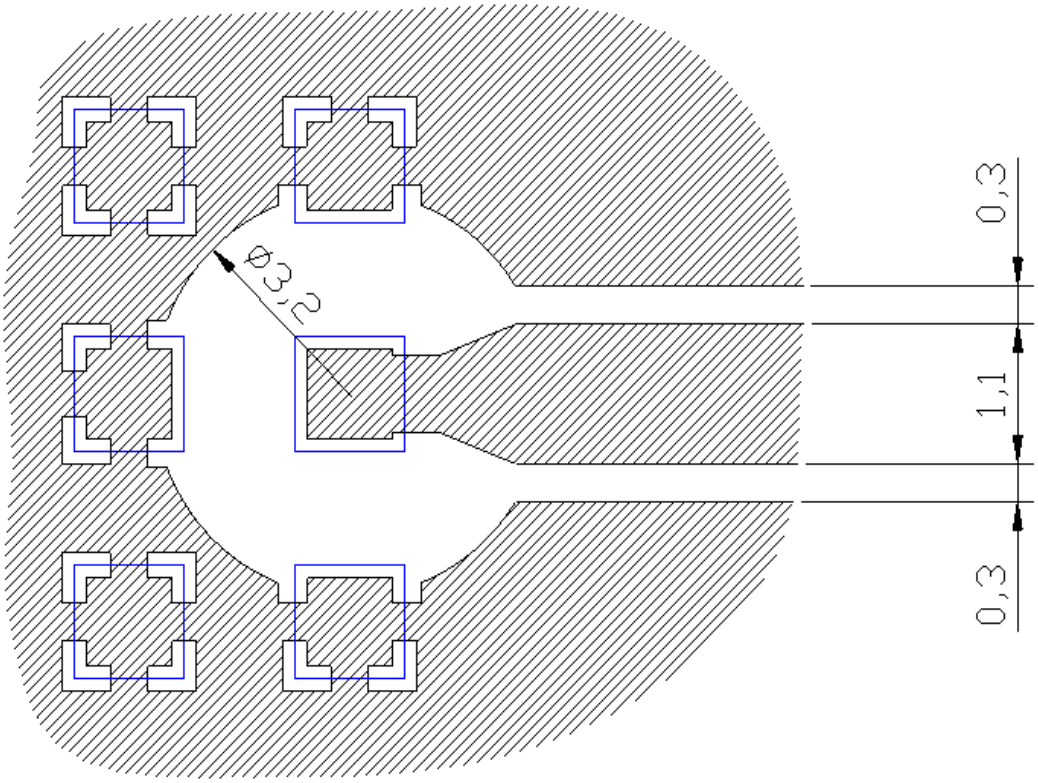
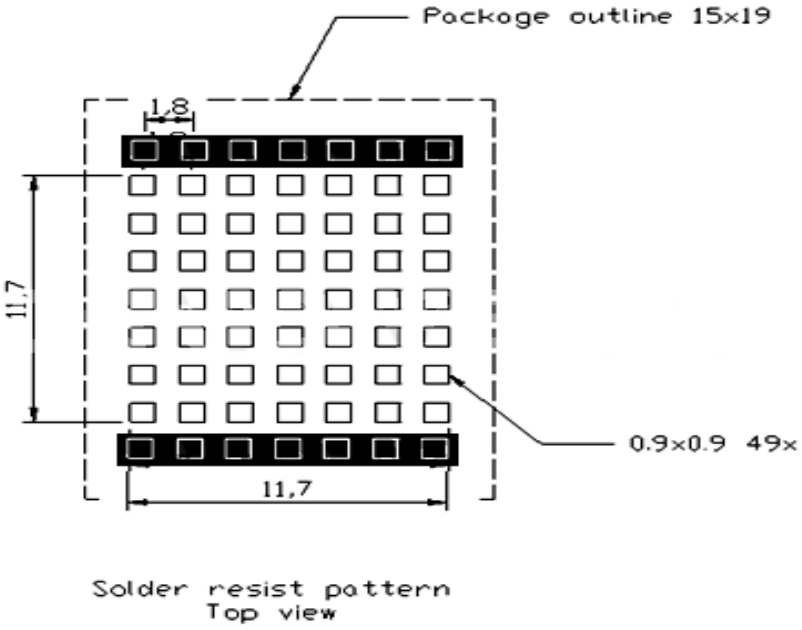


Figure 8, page 37 shows the top view of Solder resist pattern.

Figure 8 Solder Resist Pattern-Top View

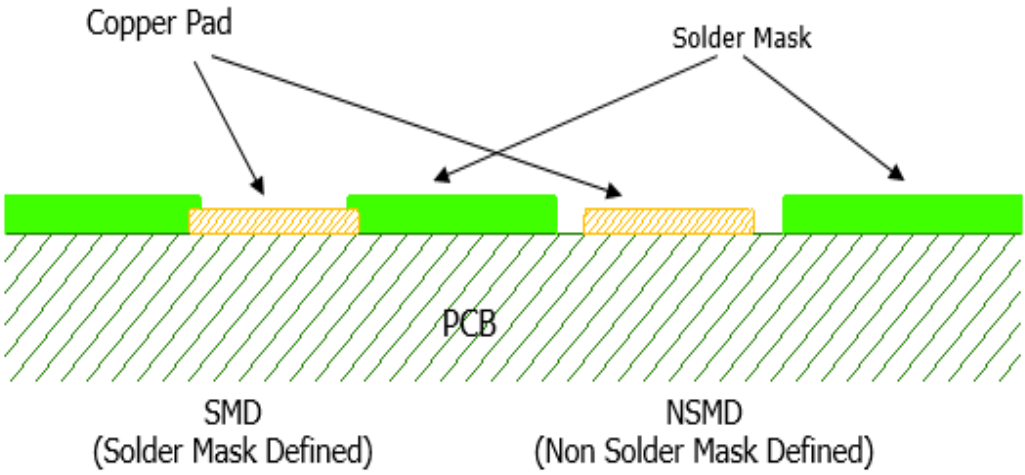


9.2 PCB Pad Design

Non-Solder Mask Defined (NSMD) type is recommended for the solder pads on the PCB.

Figure 9, page 38 shows the PCB pad design.

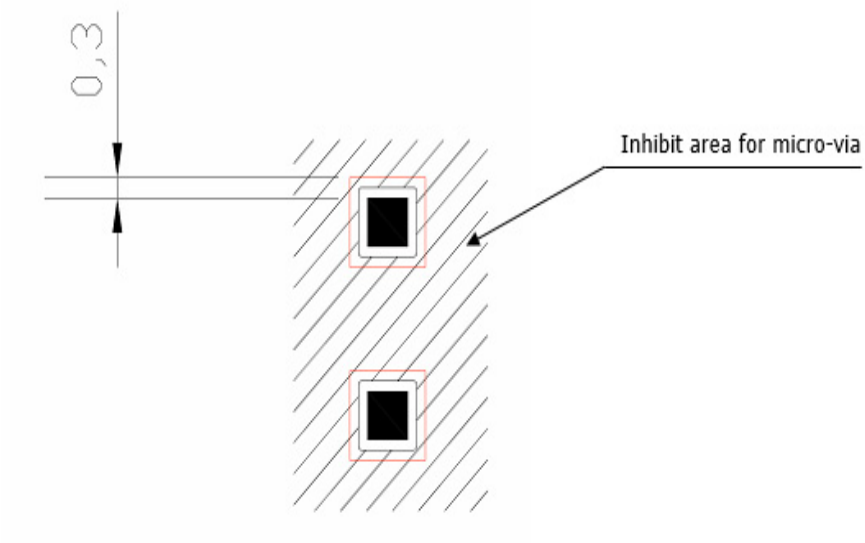
Figure 9 Solder Pads on PCB



9.3 PCB Pad Dimension

It is not recommended to place or micro-via not covered by solder resist in an area of 0.3 mm around the pads unless it carries the same signal of the pad itself. Holes in the pad are allowed only for blind holes and not for through holes. Figure 10, page 38 shows the Pad dimension:

Figure 10 Solder Resist Pattern-Top View



9.3.1 Recommendations for PCB Pad Surface

Table 17, page 39 provides the recommendation for PCB Pad Surface.

Table 17 Recommendation for PCB Pad Surface

Finish	Layer Thickness (um)	Properties
Electro-less Ni/Immersion Au	3 - 7/ 0.03 - 0.15	Good solderability protection, high shear force values

The PCB must be able to resist higher temperatures which occurs at the lead-free process. This issue should be discussed with the PCB supplier. Generally, the wettability of tin-lead solder paste on the described surface plating is better compared to lead-free solder paste.

It is not necessary to panel the application PCB, however it is suggested to use milled contours and pre-drilled board breakouts. Scoring or v-cut solutions are not recommended.

9.4 Stencil

Stencil's apertures layout can be the same of the recommended footprint (1:1), a thickness of stencil foil ≥ 120 µm is suggested.

9.5 Solder Paste

It is recommended to use only "no clean" solder paste in order to avoid the cleaning of the modules after assembly. The lead-free solder paste is Sn/Ag/Cu.

9.6 Solder Re-flow

Figure 11, page 40 shows the recommended solder profile re-flow:

Figure 11 Solder Re-flow Profile

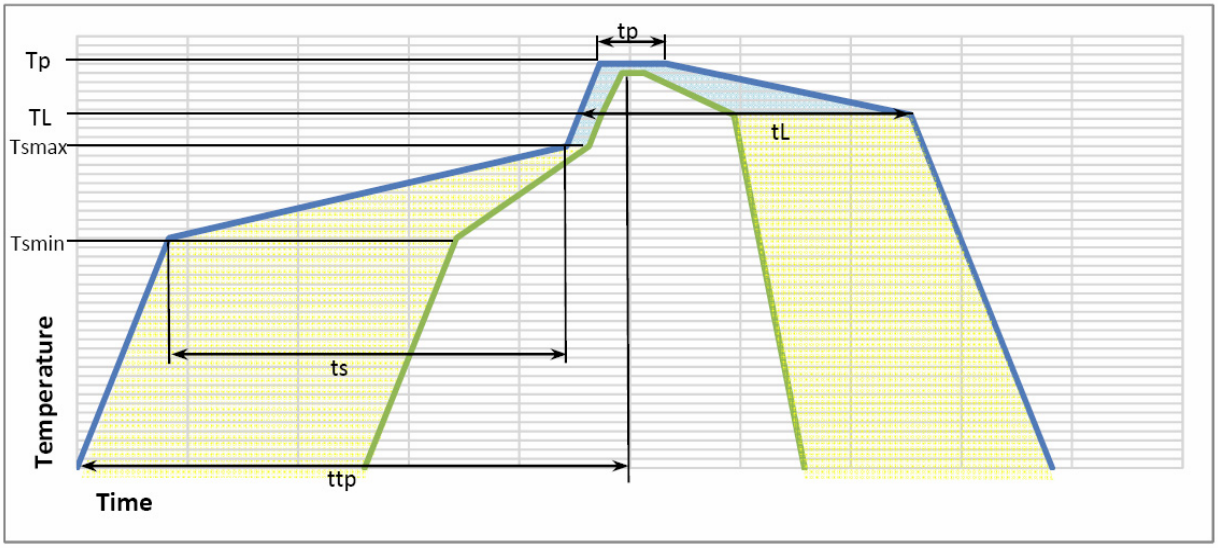


Table 18, page 40 provides the Solder re-flow profile features and its Pb-Free Assembly.

Table 18 Solder Re-flow Parameters

Profile Features	Pb-Free Assembly
Average ramp-up rate (TL to TP)	3°C/second max
Preheat	
Temperature Min (Tsmin)	150°C
Temperature Max (Tsmax)	200°C
Time (min to max) (ts)	60-180 seconds
Tsmax to TL	
Ramp-up rate	3°C/second max
Time Maintained	
Temperature (TL)	217°C
Time (t)	60-150 seconds
Peak Temperature (Tp)	245 +0/-5°C
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds
Ramp-down Rate	6°C/second max
Time 25°C to Peak Temperature	8 minutes max

NOTE: *All temperatures refer to topside of the package, measured on the package body surface.*

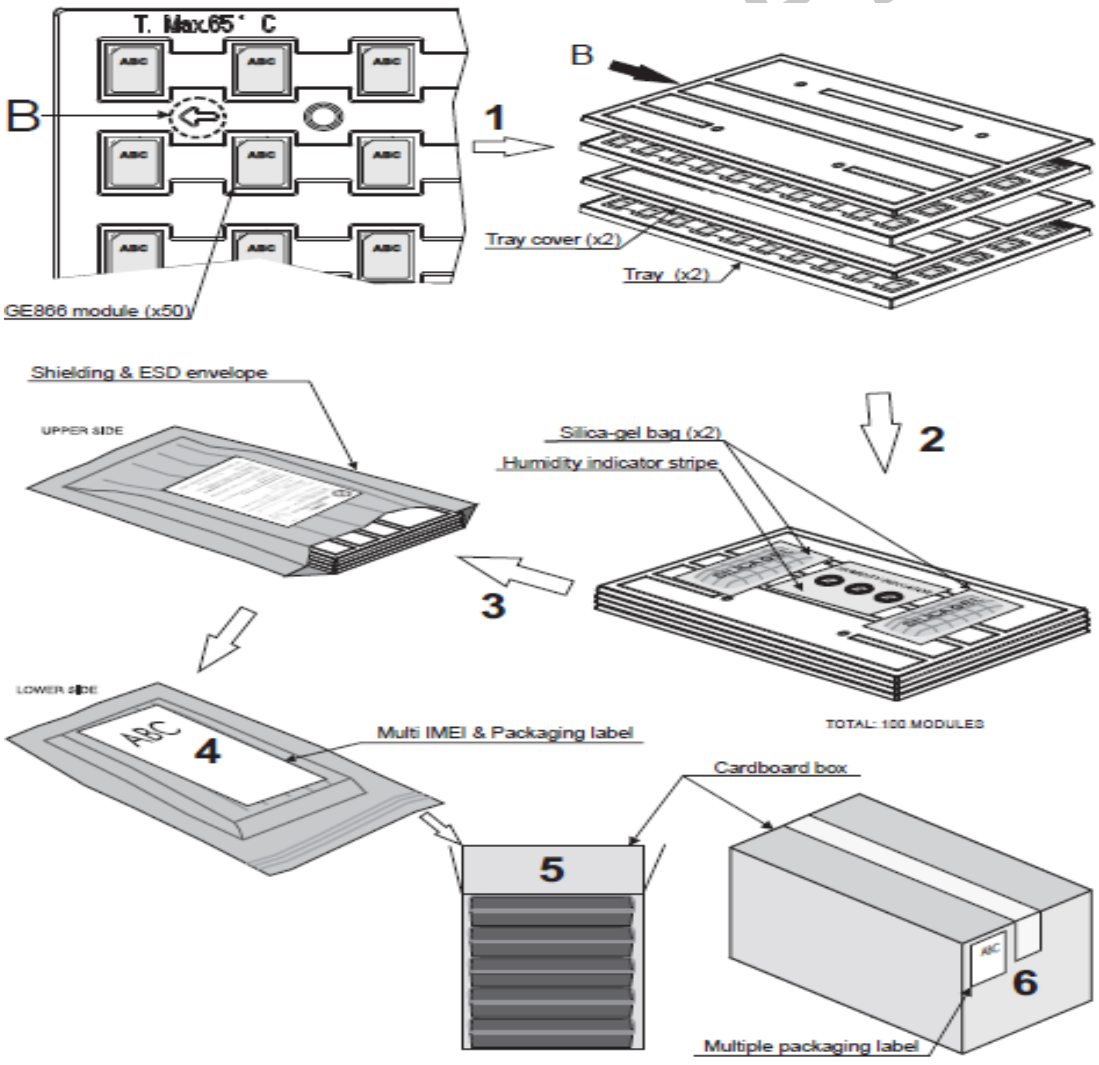
CAUTION! *WE866E4 module withstands one re-flow process only.*

Chapter 10 Packaging

10.1 Tray

The WE866E4-P modules are packaged in trays of 50 pieces each where small quantities are required (i.e. for test and evaluation purposes). Trays are not designed to be used in SMT processes for pick and place handling.

Figure 12 Packaging in Trays



10.2 Reel

Figure 13, page 44 shows WE866E4-P modules that are packaged on reels of 200 pieces each.

Figure 13 Reel - Packaging

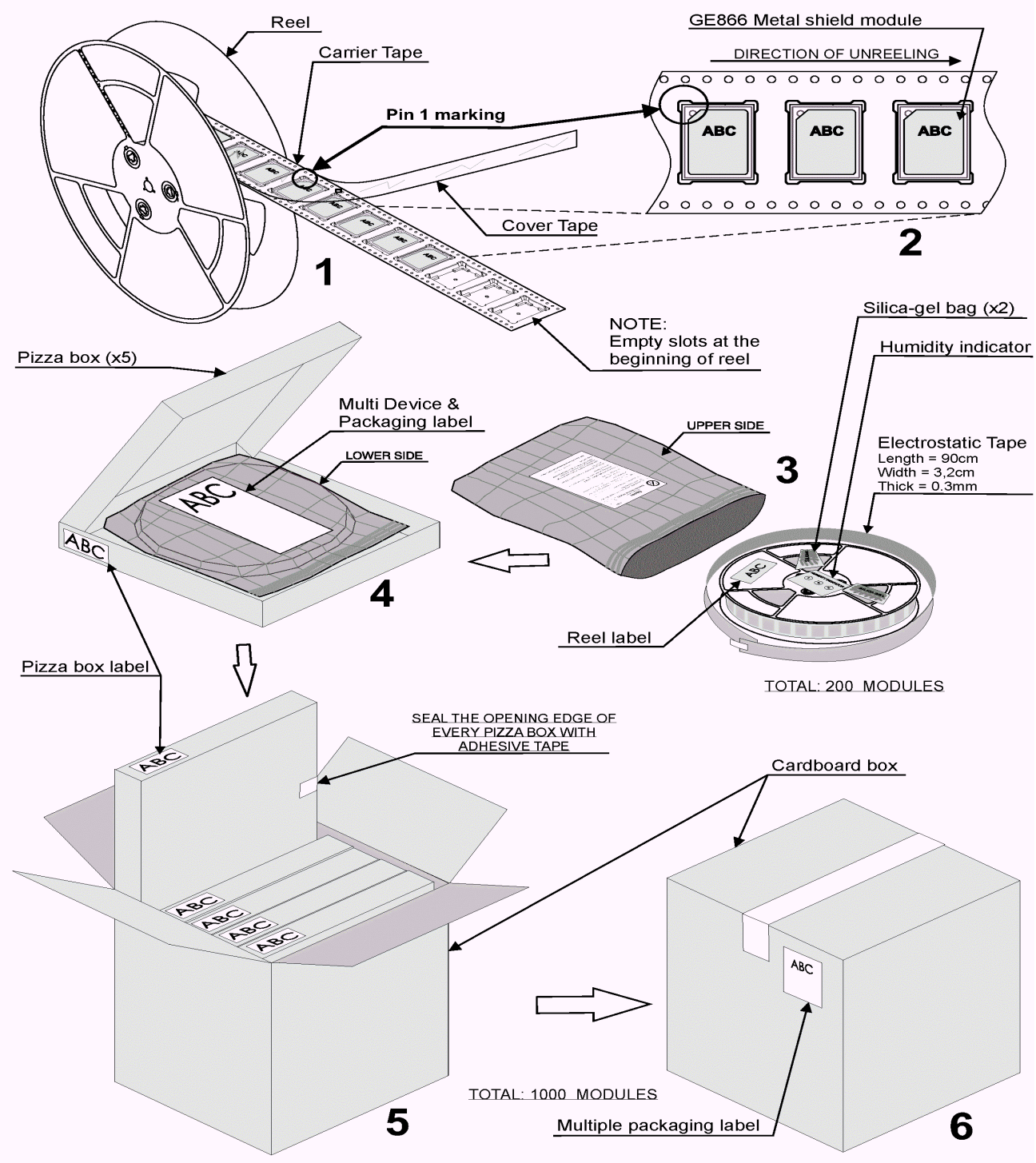
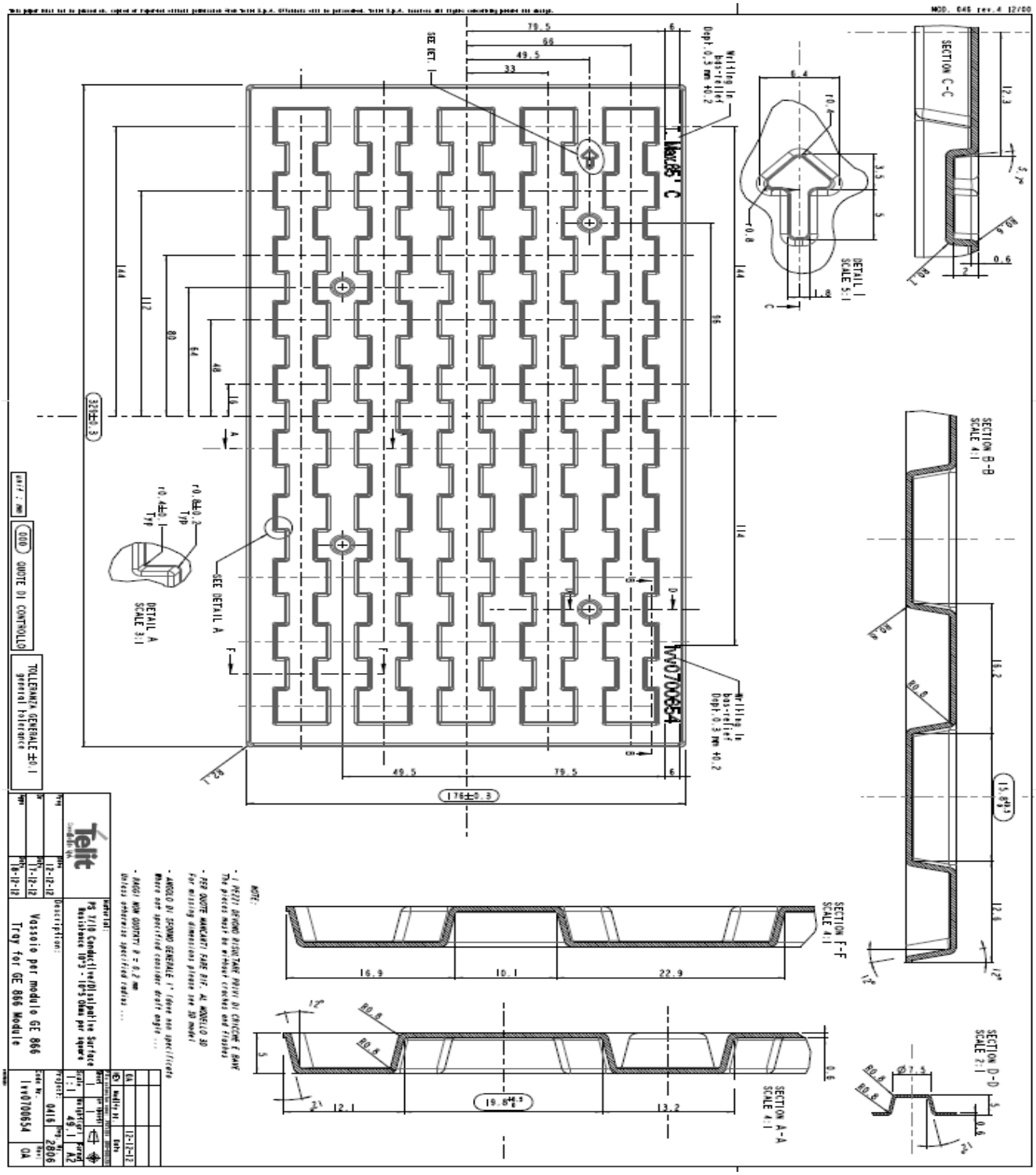


Figure 14, page 45 shows the schematic representation of Packaging.

Figure 14 Reel - Packaging in Trays



CAUTION! *These trays can withstand a maximum temperature of 65°C.*

10.3 Moisture Sensitivity

According to IPC/JEDEC J-STD-020 standards the moisture sensitivity level of the WE866E4-P module Product is “3”. To use such a component the customer has to take care of the following conditions:

a. The shelf life of the Product inside the dry bag is 12 months - from the seal date of the bag, when stored in a non-condensing atmospheric environment of < 40°C and < 90% RH.

b. Environmental condition during the production: <= 30°C / 60% RH according to IPC/JEDEC J-STD-033B.

c. The maximum time between the opening of the sealed bag and the re-flow process must be 168 hours if condition (b) “IPC/JEDEC J-STD-033B paragraph 5.2” is followed.

d. Baking is required if conditions (b) or (c) are not followed.

e. Baking is required if the humidity indicator inside the bag indicates 10% RH or more.

Chapter 11 Conformity Assessment Issue

11.1 FCC/IC Regulatory Notice

TBD

Chapter 12 Safety Recommendation

12.1 Read Carefully

Be sure the use of this product is allowed in the country and in the environment required. The use of this product may be dangerous and has to be avoided in the following areas:

- Where it can interfere with other electronic devices in environments such as hospitals, airports, aircrafts, etc.
- Where there is risk of explosion such as gasoline stations, oil refineries, etc. It is the responsibility of the user to enforce the country regulation and the specific environment regulation.

Do not disassemble the product; any mark of tampering will compromise the warranty validity. We recommend following the instructions of the hardware user guides for correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to be conformed to the security and fire prevention regulations. The product has to be handled with care, avoiding any contact with the pins because electrostatic discharges may damage the product itself. Same cautions have to be taken for the SIM, checking carefully the instruction for its use. Do not insert or remove the SIM when the product is in power saving mode.

The system integrator is responsible for the functioning of the final product; therefore, care has to be taken to the external components of the module, as well as any project or installation issue, because the risk of disturbing the GSM network or external devices or having impact on the security. Should there be any doubt, please refer to the technical documentation and the regulations in force. Every module has to be equipped with a proper antenna with specific characteristics. The antenna has to be installed with care in order to avoid any interference with other electronic devices and has to guarantee a minimum distance from the body (20 cm). In case this requirement cannot be satisfied, the system integrator has to assess the final product against the SAR regulation.

The European Community provides some Directives for the electronic equipment introduced on the market. All of the relevant information is available on the European Community website:

http://ec.europa.eu/enterprise/sectors/rtte/documents/

The text of the Directive 99/05 regarding telecommunication equipment is available, while the applicable Directives (Low Voltage and EMC) are available at:

http://ec.europa.eu/enterprise/sectors/electrical/

Chapter 13 Acronyms

TTSC	Telit Technical Support Centre
USB	Universal Serial Bus
HS	High Speed
DTE	Data Terminal Equipment
UMTS	Universal Mobile Telecommunication System
WCDMA	Wide band Code Division Multiple Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
UART	Universal Asynchronous Receiver Transmitter
HSIC	High Speed Inter Chip
BLE	Bluetooth low energy
SPI	Serial Peripheral Interface
ADC	Analog – Digital Converter
DAC	Digital – Analog Converter
I/O	Input Output
GPIO	General Purpose Input Output
CMOS	Complementary Metal – Oxide Semiconductor
MOSI	Master Output – Slave Input
MOSO	Master Input – Slave Output
CLK	Clock
MRDY	Master Ready
SRDY	Slave Ready
CS	Chip Select
RTC	Real Time Clock
PCB	Printed Circuit Board
ESR	Equivalent Series Resistance
VSWR	Voltage Standing Wave Radio

VNA	Vector Network Analyzer

Document History

Revision	Date	Changes
0.0	January 2018	Initial Release.
1.0	March 2018	Added Figure 4Top View of WE866E4-P Module, page 34
1.1	May 2018	Watermarked “PRELIMINARY”.
1.2	July 2018	Updates to Figure 3, page 33, Figure 4, page 34

SUPPORT INQUIRIES

Link to **www.telit.com** and contact our technical support team for any questions related to technical issues.

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