HE863-Family Digital Voice Interface Application Note

Making machines talk.

APPLICABILITY TABLE

PRODUCT
HE863-EUR
HE863-EUG
HE863-NAR
HE863-NAG
HE863-AUG

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Contents

1.   Introduction

1.1.   Scope

The aim of this document is the description of *the HE863-Family Digital Voice Interface feature* offered by the Telit modules that could be used in several applications, as example to connect the Wireless Module to a Bluetooth device.

1.2.   Audience

This document is intended for helping Telit modules customer integrators.

1.3.   Contact Information, Support

For general contact, technical support, to report documentation errors and to order manuals, contact Telit's Technical Support Center (TTSC) at:

TS-EMEA@telit.com
TS-NORTHAMERICA@telit.com
TS-LATINAMERICA@telit.com
TS-APAC@telit.com

Alternatively, use:

http://www.telit.com/en/products/technical-support-center/contact.php

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

http://www.telit.com

To register for product news and announcements or for product questions contact Telit's Technical Support Center (TTSC).

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

1.4.   Document Organization

This document contains the following chapters.

Chapter 1: "*Introduction*" **provides a scope for this document, target audience,** contact and support information, and text conventions.

Chapter 2: "*Overview*" **provides an overview of the document.**

Chapter 3: "*Digital Interface Description* ". Physical, technical and protocol description.

Chapter 4: "*DVI on HE863 family* ". **Deals with pin**-out of the DVI ports available in HE863 Family.

Chapter 5: "*DVI on HE863 family* ". **Deals with pin**-out of the DVI ports available in HE863 family.

Chapter 6: "*AT commands* ". **Deals with AT commands to use with DVI** interface.

Chapter 7: "*Module interfacing*". **Some suggestion about the use of the modules with** a MAXIM ® codec .

Chapter 8: "*DVI pin positions on EVK adapters* "Deals with EVK adapters pinout.

Chapter 9: "*DVI implementations*".

Chapter 10 "*SAFETY RECOMMENDATIONS*".

1.5.   Text Conventions

Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

1.6.   Related Documents

- HE863-Family Software User Guide, 1vv0300893

- HE863 Family Hardware User Guide, 1vv0300891

- HE863-Family AT commands Reference Guide, 80377ST10083a

- Telit Digital Voice Interface Application Note, 80000NT10004a

1.7.   Document History

Revision	Date	Changes
Rev.0	01/05/2011	First release
Rev.1	02/05/2011	Deleted AT CMD
Rev.2	10/02/2012	Added CLK period of Slave mode

2. Generality

This document cannot embrace the whole hardware solutions and products that may be designed. The suggested hardware configurations shall not be considered mandatory; instead the information given shall be used as a guide or a starting point for properly developing your product with the Telit modules.

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The following information can be applied HE863-Family.

2.1. I2S Overview

The I2S Audio Interface (I2SBus or IISBus) is a serial bus designed for digital audio devices. This popular serial bus has been developed by Philips ® in 1986 as a 3-wire bus for interfacing to audio chips such as codecs. It is a simple data interface, without any form of address or device selection.

The I2S design handles audio data separately from clock signals. On an I2S bus, there is only one bus master and one transmitter: the master may be a transmitter, a receiver, or a controller for data transfers between other devices acting as transmitter and receiver.

In high-quality audio applications involving a codec, the codec is typically the master so that it has precise control over the I2S bus clock.

An I2S bus design consists of the following serial bus lines:

- a line with two time-division multiplexing (TDM) data channels [SD]
- a *word select* line [WS] , also called *Word Alignment* signal [WA]
- a clock line [SCK]

Data is transmitted two's complement (MSB first) and sent from the transmitter while the data synchronization is either the *high-to-low* or *low-to-high* transition of the clock signal ,the receiver latches the data on the *leading edge* of the clock signal.

The I2S bus carries two channels (left and right) 8 bit long, which are typically used to carry stereo audio data streams. The data alternates between left and right channels, as controlled by the word select signal driven by the bus master.

The Word Alignment signal [WA] is sent one clock before the useful data.

The I2S Bus uses standard TTL logic levels.

2.2.   DVI description

The Digital Voice Interface is an I2S Audio Interface that works in PCM at 8 KHz Mono voice data.
It provides a bidirectional, synchronous, serial interface to off-chip audio devices.

The Telit Modules support the Digital Voice Interface (from here onwards DVI), which can be used to transfer digital audio data to and from the module itself.

In the rest of this document we will refer to it as DVI port.

⚠️ WARNING: the Telit Modules can have one or two DVI ports, but only one can be active at the time. The choice between these two ports depends by the configuration of the alternate function of the interface pins on the customer applications.

Please refer to the pin-out section (or to User Guide of the module that you are using) for the available DVI ports.

⚠️ WARNING: The DVI can be configured either as MASTER (clock output) or SLAVE (clock input), SLAVE mode being allowed only on DVI#1 port.

The DVI Volume is controlled by the same AT command as for the analog interface: for more information refer to the AT Commands Reference Guide for the Telit modules.

The Echo canceller feature is active both for DVI and for the analog audio.

2.2.1.   Features summary

Used mode ....PCM mono voice data
Data valid........................on falling edge of clock transition
Operations mode............ Master and Slave
Transmission..................bi-directional (independent receiver and transmitter)
Sampling rate................. 8 kHz
Mode supported............. burst and continuous transmission

WA pulse **length**..............one clock cycle

2.3.   Hint on PCM

Although analog communication is ideal for human communication, analog transmission is neither robust nor efficient at recovering from line noise.
As example in the early telephony network, when analog transmission was passed through amplifiers to boost the signal, not only was the voice boosted but the line noise was amplified, as well. This line noise resulted in an often-unusable connection.
It is much easier for digital samples, which are comprised of 1 and 0 bits, in order to be separated from line noise. Therefore, when analog signals are regenerated as digital samples, a clean sound is maintained.
PCM converts analog sounds into digital form by sampling the analog sounds 8000 times per second and converting each sample into a numeric code. If you sample an analog signal at twice the rate of the highest frequency of interest, you can accurately reconstruct that signal back into its analog form (Nyquist theorem). Because most speech content is below 4000Hz, a sampling rate of 8000 times per second (8KHz that means 125 μsec between samples) is required.

2.4. Signals

The DVI can be set to allow PCM data to be transferred from and to other devices. Only four signals are needed, because the Clock and Word Alignment are used for both receive and transmit direction. The Word Alignment signal (called WAO in the rest of this document) acts as frame synchronization signal, avoiding a continuous data transfer.

I2S Signal function	DVI Signal function	Description
Clock	PCM_CLK	Data Clock
Word Alignment	PCM_SYNC(WA0)	Frame Synchronism
serial audio data input	PCM_RX	Received Data
serial audio data output	PCM_TX	Transmitted Data

DVI signals table.

2.4.1. Electrical Characteristics

	Minimum	Maximum	Unit
V_{IL}	-0.36	0.36	V
V_{IH}	1.26	3.3	V
V_{OI}		0.45	V
V_{OH}	1.26		V

2.5. Mode of operation

The DVI operates in 16-bit data burst mode, starting with the most significant bit (MSB).

Voice is 13-bit 2's complement but the output of the speech decoder is saved on 16-bit 2's complement (Q15 format). The last 3 LSBs are equal to 0.

The data transmit operation works as follows:
At each falling edge of CLK, the state on the WAO line is checked. After a high level on WAO has been detected (syncro capture condition) the MSB of the transmit data is put on the TX line at the next rising edge of CLK.
Now the interface waits until a low level on WAO is detected during the falling edge of CLK (start bits shifting condition).

If this condition has been revealed, the interface shifts out the remaining data bits, one bit at each rising edge of CLK. As soon as all 16 bits have been transmitted a new data sample is transferred immediately from the TX buffer to a shift register. Thus, a continuous data transfer can be achieved.

The data receive operation works in nearly the same way.

The frame lasts for 17 clock pulses, because one more clock pulse is needed for the frame synchronization of the signal WAO.

Figure 1 . Timing of Digital Voice Interface signal in PCM mode

2.6.   Master mode Clock frequency

As described, in PCM mode each frame contains 16 data bits+1 WAO cycle; this results in a frame length of 17 shift clock cycles. Reminding that the audio sampling rate is 8KHz, the nominal bit clock frequency will be:

$$fclk = 8KHz * 17 = 136KHz$$

2.7.   Timing characteristics

The **DVIs** can be configured both **MASTER** (the clock signal is internally generated) and **SLAVE** (the clock signal is externally generated).

2.7.1.   Master Mode

Parameter	Symbol	Limit Values			Unit
		Min	typ	Max	
CLK clock period	t_{I2Sbm1}	-	T=7,35[1]	-	μs
CLK high time	t_{I2Sbm2}	T/2-20	T/2		μs
CLK low time	t_{I2Sbm3}	T/2-20	T/2		μs
TX invalid before CLK high end(before shifting edge of CLK)	t_{I2Sbm4}	-	-	24	ns
TX valid before CLK low begin (after shifting edge of CLK)	t_{I2Sbm5}	-	-	31.2	ns
RX setup time before CLK low end (before latching edge of CLK)	t_{I2Sbm6}	59.6	-	-	ns
RX hold time after CLK high begin (after latching edge of CLK)	t_{I2Sbm7}	10	-	-	ns
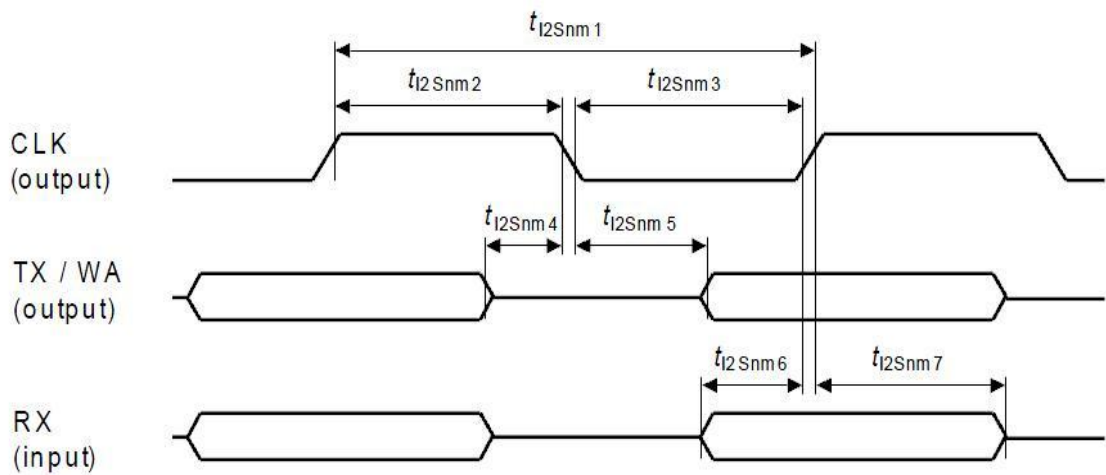
i2s_normal_master.vsd

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[1] In MASTER mode the DVI provides CLK *(136KHz)* and WA *(8KHz)* signals.

2.7.2. Slave Mode

Parameter	Symbol	Limit Values			Unit
		Min	typ	Max	
CLK clock period	t_{I2Sbm1}	T=7,35	$-^2$	T=3.846	µs
CLK high time	t_{I2Sbm2}	120	-	-	ns
CLK low time	t_{I2Sbm3}	120	-	-	ns
TX invalid before CLK falling	t_{I2Sbm4}	-	-	12	ns
TX (continued) valid after CLK falling edge	t_{I2Sbm5}	-	-	78.8	ns
RX setup time before CLK rising edge (before latching edge of CLK)	t_{I2Sbm6}	21.6	-	-	ns
RX hold time after CLK rising edge (after latching edge of CLK)	t_{I2Sbm7}	24	-	-	ns
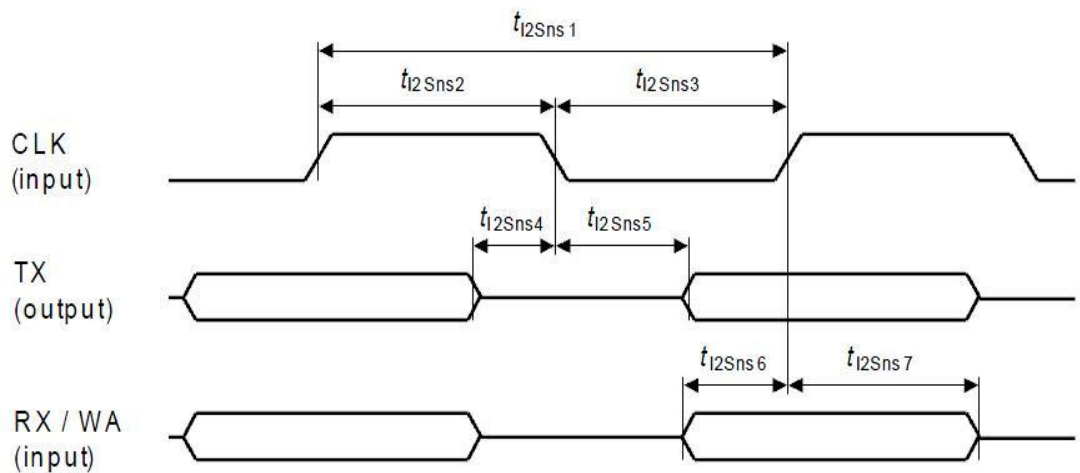
i2s_normal_slave.vsd

3.   AT Commands

The following table shows the *AT commands* which activate and control all *DVI* functions.

#DVI - Digital Voice band Interface	

AT#DVI=<mode>[,<dviport>, <clockmode>]	Set command enables/disables the Digital Voice band Interface.
	
	Parameters:
	<mode> - enables/disables the DVI.
	  0 - disable DVI; audio is forwarded to the analog line; DVI pins can be used for other purposes, like GPIO, etc. (factory default)
	  1 - enable DVI; audio is forwarded to the DVI block
	<dviport>
	  2 - DVI port 2 will be used (factory default)
	<clockmode>
	  0 - DVI slave
	  1 - DVI master (factory default)
	
	NOTE: #DVI parameters are saved in the extended profile.

AT#DVI?	Read command reports last setting, in the format: **#DVI: <mode>,<dviport>,<clockmode>**
AT#DVI=?	Test command reports the range of supported values for parameters **<mode>,<dviport>** and **<clockmode>**
Example	AT#DVI=1,2,1 OK *DVI activated for audio. DVI is configured as master providing on DVI Port #2*

4.   Modules Pin-out

In the following paragraphs you can find the cross list between the *DVI* signals and their physical positions on the Telit modules.

4.1.   HE863 Family

4.1.1.   HE863

Due to physical interface restrictions, the HE863 Modules family has only the *DVI# 1* port available on the system interface.

The connections to the application are made through the BGA system.

4.1.1.1.   DVI Port1 pin-out

DVI Function	Module Function	Ball
PCM_CLK	I2S2-CLK0	M6
PCM_SYNC	I2S2-WAO	M7
PCM_RX	I2S2-RX	M8
PCM_TX	I2S2-TX	M9

5. DVI pin positions on EVK adapters

Before designing their own applications, Telit offers to the customers the possibility to evaluate the module performance using an Evaluation kit EVK, on which it is possible to fit every module fitted on its own adapter interface.

The *DVI* functionality pins are at disposal on the adapter connectors and/or on EVK connectors.

The following paragraphs summarize the DVI ports pin positions on the EVK and/or adapters connectors (for further information, refer to EVK2 User Guide).

5.1. HE863 Family

5.1.1. HE863 EVK

		EVK_KS0127x	
DVI Function	Pin Function	PL101	PL102
PCM_CLK	PCM_CLK		13
PCM_SYNC	PCM_SYNC/TGPIO_17	19	
PCM_RX	PCM_RX/TGPIO_18	17	
PCM_TX	PCM_TX/TGPIO_10		7

6. DVI implementation examples

6.1. HE863 Family

Two modules are cross connected (Data Input   Data Output) to Base Station Simulators: one is MASTER configured and the second is SLAVE configured (using DVI#1 port).

7.   Interfacing an external codec

Here we described a possible application of the DVI: the audio signals are sent to and received from of an external Codec, the MAX9853 ® from MAXIM.
This device is a stereo audio codec with two digital interfaces, supporting various audio formats and has the **voice mode compatible with the module's** DVI.

The figure below shows the typical block level schematic.
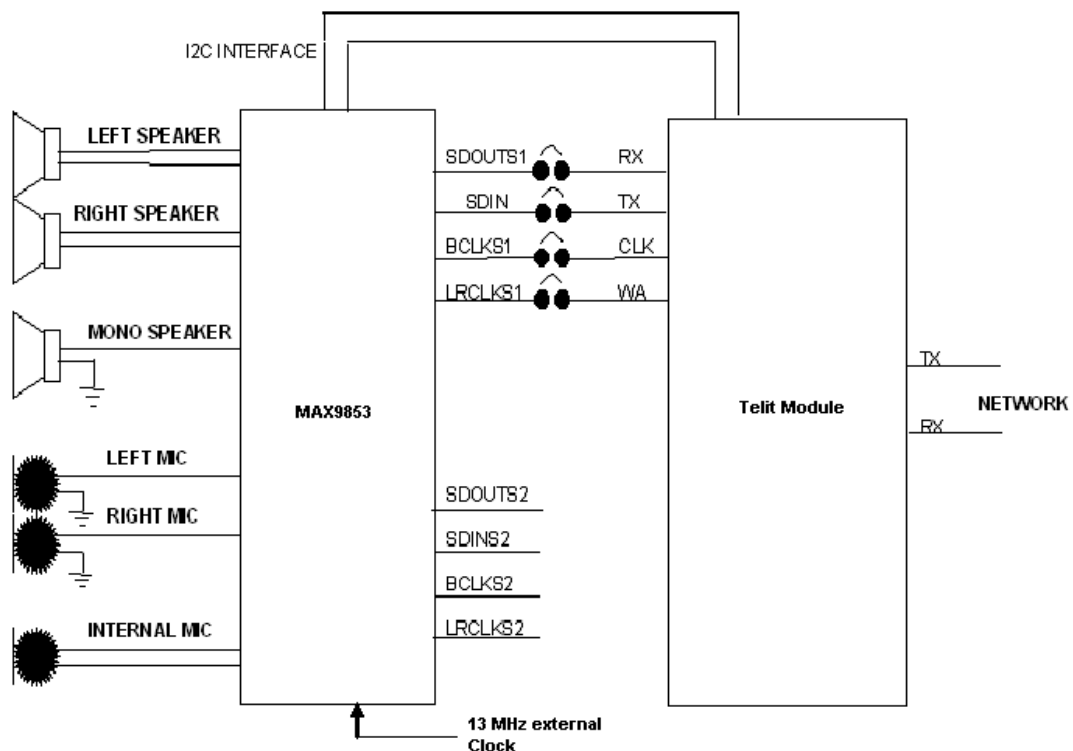
This application has been realized with the module configured as Master, at 136 KHz clock rate, enabling the #1 serial digital interface of the codec, set as Slave in 8 KHz voice mode.

As power supply to the analog (AVdd) and digital (DVdd) part of the codec could be used the external voltages, while the positive supply for the speakers (PVdd) could be the *VBatt*.

The user can configures and controls the external codec through an I2C interface as follow table.

I2C Device address	Register address	Data	Description
0x20	0x03	0xca	Enable digital audio 8 KHz mono voice mode on left channel
	0x04	0x20 *or* 0x00	Digital interface as slave and clock polarity
	0x0a	0x22	Enable left microphone input
	0x0b	0x10	Left DAC to analog output
	0x18	0x10	Enable only left speaker
	0x1a	0xf5	System Clock control
	0x1b	0xa2	Enable ADC and DAC
	0x12	0x07	Microphone control
	0x08	0x22	Mix the digital interface 1

7.1. Connections with HE863-Family Modules

A Codec shall be used external I2C bus to control like MAX9853 and so on.

8.   SAFETY RECOMMENDATIONS

NOTE. Read this section carefully to ensure the safe operation.

Be sure the use of this product is allowed in the country and in the environment required. The use of this product may be dangerous and has to be avoided in the following areas:

- Where it can interfere with other electronic devices in environments such as hospitals, airports, aircrafts, etc

- Where there is risk of explosion such as gasoline stations, oil refineries.

It is responsibility of the user to enforce the country regulation and the specific environment regulation.

Do not disassemble the product; any mark of tampering will compromise the warranty validity.

We recommend following the instructions of the hardware user guides for a correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to be conforming to the security and fire prevention regulations.

The product has to be handled with care, avoiding any contact with the pins because electrostatic discharges may damage the product itself. Same cautions have to be taken for the SIM, checking carefully the instruction for its use. Do not insert or remove the SIM when the product is in power saving mode.

The system integrator is responsible of the functioning of the final product; therefore, care has to be taken to the external components of the module, as well as of any project or installation issue, because the risk of disturbing the GSM network or external devices or having impact on the security. Should there be any doubt, please refer to the technical documentation and the regulations in force.

Every module has to be equipped with a proper antenna with specific characteristics. The antenna has to be installed with care in order to avoid any interference with other electronic devices and has to guarantee a minimum distance from the body (20

cm). In case of this requirement cannot be satisfied, the system integrator has to assess the final product against the SAR regulation EN 50360.

The European Community provides some Directives for the electronic equipments introduced on the market. All the relevant information is available on the European Community website:

http://europa.eu.int/comm/enterprise/rtte/dir99-5.htm

The text of the Directive 99/05 regarding telecommunication equipments is available, while the applicable Directives (Low Voltage and EMC) are available at:

http://europa.eu.int/comm/enterprise/electr_equipment/index_en.htm