HE910 Family Digital Voice Interface

Application Note

80000NT10050A Rev. 1 – 2012-02-16

APPLICABILITY TABLE

NOTICE: *the features covered by the present document are supported by the products having a software version equal or greater than the version showed on the following tables. The* ***software version*** *is indicated by the digits in bold style.*

HE910 Family	Platform Version	Hardware User Guide Refer to chapter 1.6
HE910-xx	12.**00**.xx**1**	[1]

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Contents

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Tables

1. Introduction

The present document provides the reader with a guideline concerning the use of the Digital Voice Interface developed on the Modules of the HE910 family. The document deals with the Digital Voice Interface configurations and its audio formats. To describe them some examples will be showed with the relating timing figures.

1.1. Scope

This Application Note covers the configurations of the Digital Voice Interface, e.g.: the selections of the voice sampling frequency, the bit number of the voice sample, the audio formats, etc. In addition, the document shows the configuration of a popular Audio Codec connected to the Module. These activities are accomplished via I^2S and I^2C buses; the hardware characteristics of the two buses are beyond the scope of the document.

1.2. Audience

The document is intended for those users that need to develop applications dealing with signal voice in digital format.

1.3. Contact Information, Support

For general contact, technical support, to report documentation errors and to order manuals, contact Telit Technical Support Center (TTSC) at:

TS-EMEA@telit.com
TS-NORTHAMERICA@telit.com
TS-LATINAMERICA@telit.com
TS-APAC@telit.com

Alternatively, use:

http://www.telit.com/en/products/technical-support-center/contact.php

For detailed information about where you can buy the Telit Modules or for recommendations on accessories and components visit:

http://www.telit.com

To register for product news and announcements or for product questions contact Telit Technical Support Center (TTSC).
Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.
Telit appreciates feedback from the users of our information.

1.4. Document Organization

This document contains the following chapters addressing the listed main topics.

Chapter 1: introduction, scope, target audience, contact and support information;

Chapter 2: Digital Voice Interface introduction and configuration;

Chapter 3: Application examples.

Annex 4: Some ancillary topics

1.5. Text Conventions

Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

1.6. Related Documents

[1] HE910 Hardware User Guide, code: 1vv0300925
[2] MAX9867 Ultra-Low Power Stereo Audio Codec, MAXIM
[3] HE910 AT Commands Reference Guide, code 80378ST10091A

1.7. Document History

Revision	Date	Changes
0	2011-07-11	First issue
1	2012-02-16	The present revision supersedes Rev. 0

1.8. Abbreviations and Acronyms

DTE	Data Terminal Equipment
DVI	Digital Voice Interface
GPIO	General Purpose Input/Output
I^2C	Inter-Integrated Circuit
I^2S	Inter-IC Sound
MSB	Most Significant Bit

2. Digital Voice Interface Use

Before dealing with the configuration and technical aspects of the Telit' Digital Voice Interface (DVI) it is useful to illustrate briefly where and how this interface can be used.

Refer to fig. 1: the voice coming from the downlink, in digital format, is in some way captured by the dedicated software running on the Module and directed to the Digital Voice Interface. At this point it is responsibility of the Audio Codec to decode the voice and send it to the speaker. The other way round the voice captured by the microphone is coded by the Audio Codec and directed through the Digital Voice Interface to the Module that collects the received voice, in digital format, and send it on the uplink.

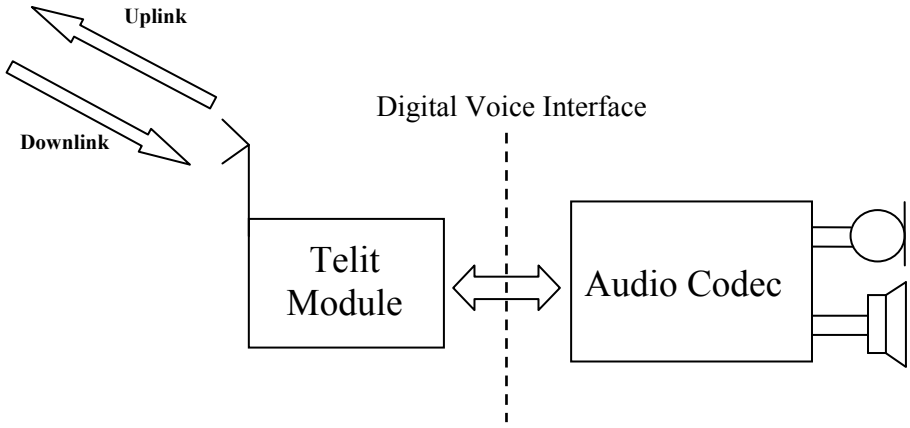


fig. 1: Example of Digital Voice Interface Use

2.1. DVI Introduction

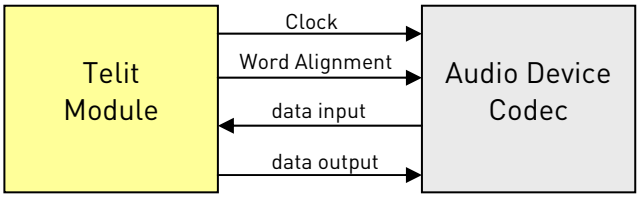
The physical DVI interface is based on the I²S Bus provided by the Module to perform digital Audio transfer. An I²S overview is reported on chapter 4.1. Tab. 1 summarizes the DVI signals and a short description for each one. Information concerning the electrical characteristics and signal pin-out is showed on [1].

I²S Signal	DVI Signal	Description
Clock	DVI_CLK	Data Clock
Word Alignment	DVI_WAO	Frame Synchronism
serial audio data input	DVI_RX	Received Data
serial audio data output	DVI_TX	Transmitted Data

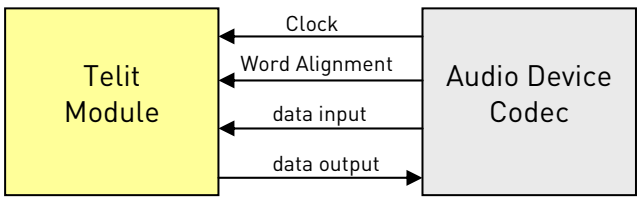
Tab. 1: DVI Signals

The figures below show the two basic configurations of the DVI interface relating the Word Alignment and Clock signals. These configurations are derived from the concepts of the first I²S bus design described on chapter 4.1. When the Module is Master the Clock and Word Alignment signals (also called Word Alignment Output WAO) are generated by the Module itself, instead when it is Slave, both signals are generated by the connected device: the Codec.

E.g.: before establishing a call it is possible, via AT commands furnished by Telit [3], to select one of the two configurations and properly setting the Module and the Codec.



Module = Master



Module = Slave

fig. 2: Master and Slave configurations

2.1.1. DVI Configurations

Several DVI audio bus configurations are available via AT#DVI and AT#DVIEXT commands as summarized by the following tables.

AT#DVI =<mode>,<dviport>,<clockmode>		
<mode>	<dviport>	<clockmode>
0 →disable DVI	1 → reserved	0 → DVI slave
1 → enable DVI	2 → select DVI port 2	1 → DVI master
2 → reserved		

Tab. 2: DVI configuration via AT#DVI command

AT#DVIEXT=<config>,<samplerate>,<samplewidth>,<audiomode>,<edge>	
<samplerate>	<samplewidth>
0 → 8 [KHz] sampling frequency	0 → 16 bits per sample
1 → 16 [KHz] sampling frequency	1 → 18 bits per sample
	2 → 20 bits per sample
	3 → 24 bits per sample
	4 → 32 bits per sample

Tab. 3: DVI configuration via AT#DVIEXT command (con't)

DVI Modes	Audio format	WAO signal	AT#DVIEXT <remaining parameters>		
			<config>	<edge>	<audiomode>
Normal	I^2S	square-wave	1	0 (1 reserved)	0 - Mono[1] 1 – DualMono[1]
Burst	PCM	pulse	0	0 → WAO transition is synchronized with the CLK falling edge.	
				1 → WAO transition is synchronized with the CLK rising edge.	

Tab. 4: DVI configuration via AT#DVIEXT command

DVI audio bus supports Normal and Burst modes that are relating to the audio formats and the shape of the Word Alignment signal (WAO). The WAO signal is used to define the beginning of a frame, and may be programmed as either a pulse or a square-wave signal. For each DVI mode can be selected the Master or Slave configuration.

[1] Mono Mode and Dual Mode are equivalent in Normal mode.

3. Application Examples

The next chapters will show examples concerning some audio formats supported by the DVI audio bus in Master and Slave configurations. All the examples will refer to the sketch illustrated below.
I²C bus is used to configure the MAX9867 Codec[2] [2]: the user by means of suitable AT commands can completely control the Codec. The DVI bus provides the voice connection between the two devices, for a reference design see chapter 4.3.

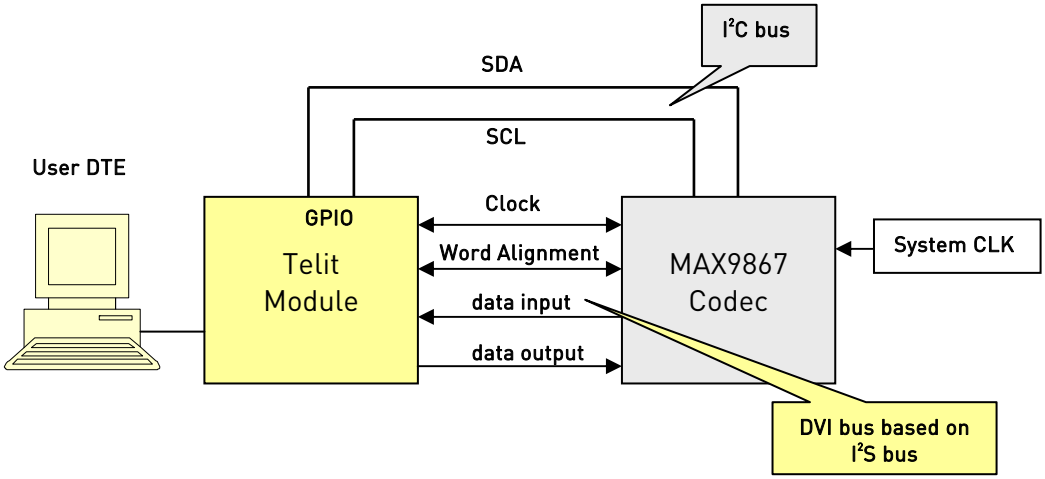


fig. 3: Telit Module/Codec Connections

[2] In order to make concrete examples we use the MAX9867 Codec, see chapter 4.3 for schematic reference design. The user is free to select the desired codec compliant with the technical characteristics provided by the modules of the Telit HE910 family.

3.1. Normal Mode (I^2S)

3.1.1. Module is Master

Refer to figure below: the MSB of the left channel is clocked on the second CLK rising edge after WAO transitions. When WAO is low, left channel data is transmitted and when WAO is high, right channel data is transmitted (right + left = 2 channels).

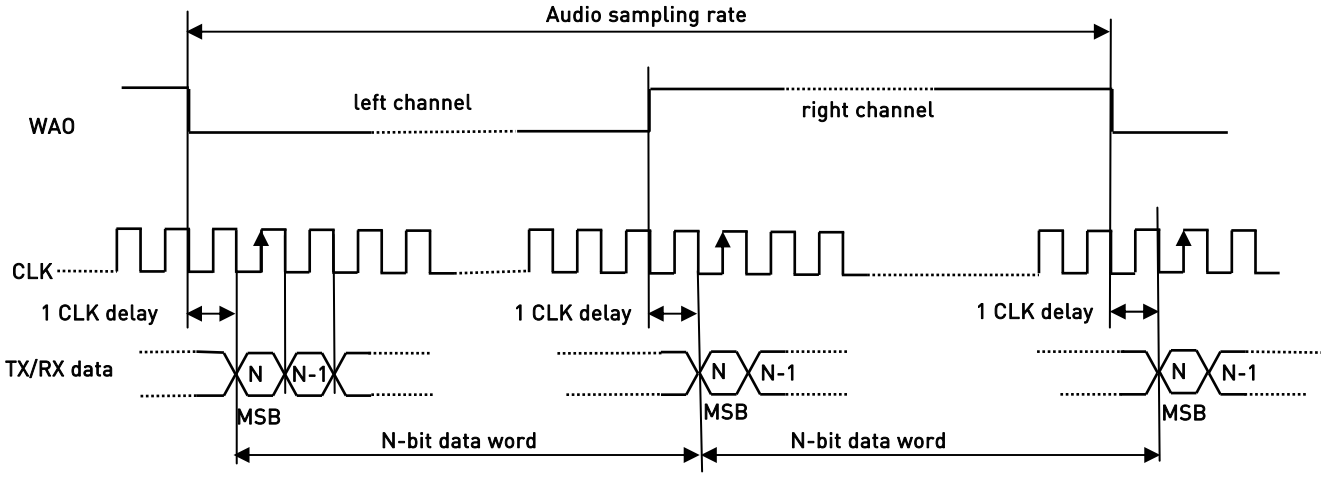


fig. 4: Timing Diagram of I^2S Audio Format

In general, the BitClockFrequency (CLK) is furnished by the following expression:

$$BitClockFrequency = DataWordBit \times ChannelNumber \times SamplingFrequency$$

Refer to Tab. 5 for the BitClockFrequency generated by the Module.

<samplewidth>	Data word bit	Left, right channels	Sampling frequency	
			8 KHz	16 KHz
			Bit Clock frequencies in KHz	
0	16	2	256	512
1	18	2	384	768
2	20	2		
3	24	2		
4	32	2	512	1024

Tab. 5: Bit Clock frequencies

Follow the lists of the AT commands used to cause the Module to enter Master configuration/I²S-compatible audio format and configure the Codec in accordance with the current Module setting. After each command, for reader convenience, is reported the meaning of the used parameters.

Configure the Module to operate with I²S-compatible audio format

AT#DVI=1,2,1
OK

DVI bus

1 enable DVI
2 use DVI port 2 (mandatory)
1 DVI Master (factory setting)

AT#DVIEXT=1,0,0,1,0
OK

1 Normal Mode (factory setting)
0 sample rate 8 KHz (factory setting)
0 16 bits per sample (factory setting)
1 Dual Mono (factory setting)
0 I²S

NOTICE: *in the timing showed on the fig. 4 the two N-bit data words are equals because the Dual Mono mode has been selected.*

Configure the Codec to operate with I²S audio format

I²C bus

AT#I2CWR=X,Y,30,4,19
>00109000100A330000330C0C09092424400060
OK

x	GPIO number used as SDA, refer to [3]
y	GPIO number used as SCL, refer to [3]
30	Device address on I²C, refer to [2]
4	Register address from which start the writing, refer to [2]
19	number of bytes to write
>00109000.....refer to [2]	

AT#I2CWR=X,Y,30,17,1
>8A
OK

x	GPIO number used as SDA, refer to [3]
y	GPIO number used as SCL, refer to [3]
30	Device address on I²C, refer to [2]
17	Register address where write data, refer to [2]
1	number of bytes to write
>8A	refer to [2]

The following figure shows the timing diagram, captured by an oscilloscope, concerning the above described example. The clock generated by the Module is 384 KHz.

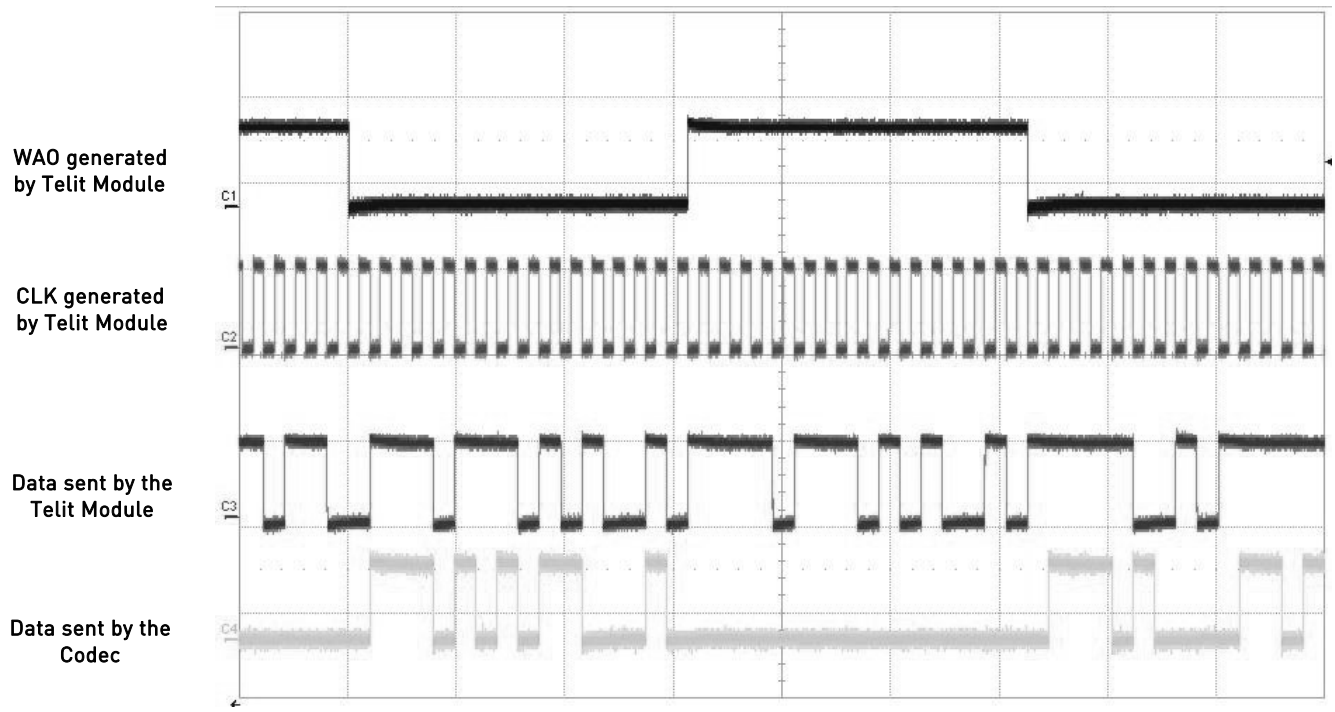


fig. 5: Timing Diagram of Module in Master configuration/Normal mode

3.1.2. Module is Slave

Refer to fig. 4 for basic timing diagram.

Follow the list of the AT commands used to cause the Module to enter Slave configuration/I²S audio format and configure the Codec in accordance with the current Module setting.

Configure the Module to operate with I²S-compatible audio format

DVI bus

AT#DVI=1,2,0
OK

1	enable DVI
2	use DVI port 2 (mandatory)
0	DVI Slave

AT#DVIEXT=1,0,3,1,0
OK

1	Normal Mode (factory setting)
0	sample rate 8 KHz (factory setting)
3	24 bits per sample
1	Dual Mono (factory setting)
0	I²C

NOTICE: *the used Codec, in Master configuration, generates a clock equal to 384 KHz therefore the selected number of bits per sample on Module is 24, see Tab. 5.*

Configure the Codec to operate with I²S audio format

I²C bus

AT#I2CWR=X,Y,30,4,19
>00101000900233000033OC0C09092424400060
OK

x	GPIO number used as SDA
y	GPIO number used as SCL
30	Device address on I²C
4	Register address from which start the writing
19	number of bytes to write
>00101000.....refer to [2]	

AT#I2CWR=X,Y,30,17,1
>8A
OK

x	GPIO number used as SDA
y	GPIO number used as SCL
30	Device address on I²C
17	Register address where write data
1	number of bytes to write
>8A	refer to [2]

The following figure shows the timing diagram, captured by an oscilloscope, concerning the above described example. The clock generated by the Codec is 384 KHz.

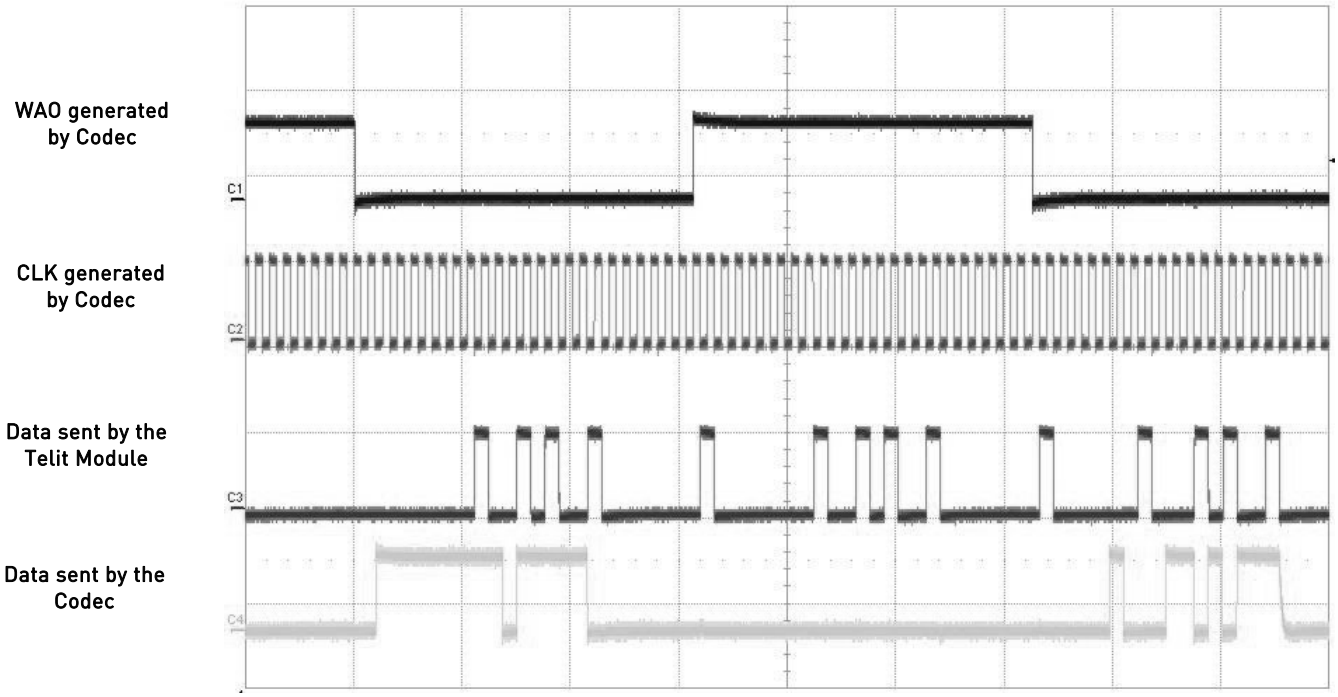


fig. 6: Timing Diagram of Module in Slave configuration/Normal mode

3.2. Burst Mode (PCM)

3.2.1. Module is Master

In PCM audio format the MSB of the channel included in the frame (WAO) is clocked on the third CLK falling edge after the WAO pulse rising edge. The period of the WAO signal (frame) lasts for Data word bit + 2 clock pulses.

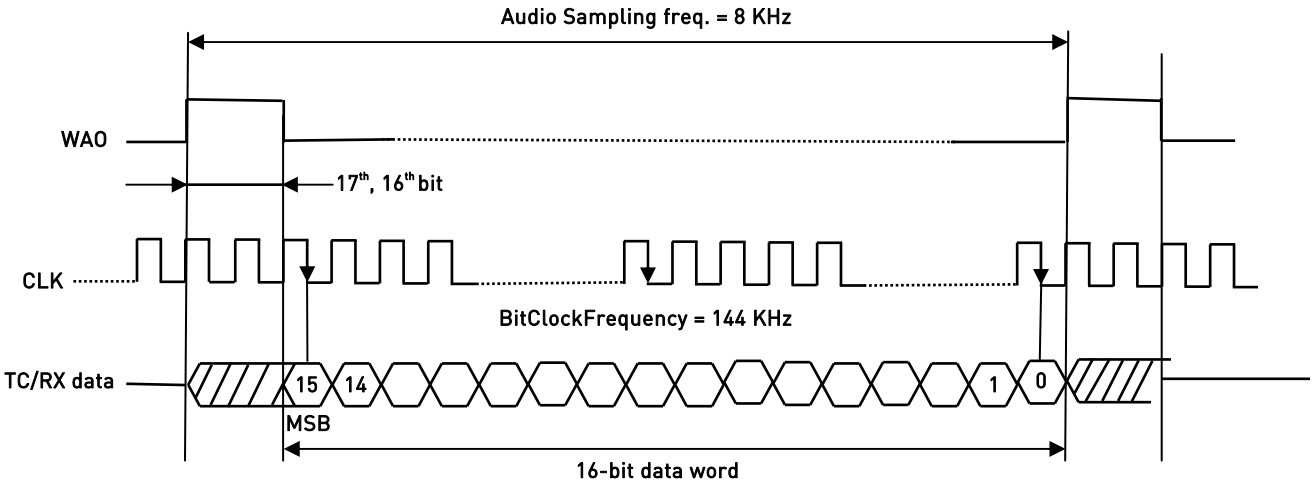


fig. 7: Timing Diagram of PCM Audio Format (Burst mode) /Mono Mode

In general, the BitClockFrequency (CLK) is furnished by the following expression:

$$BitClockFrequency = \left(\ DataWordBit + 2 \ \right) \times SamplingFrequency$$

Refer to Tab. 6 for the BitClockFrequency generated by the Module.

<samplewidth>	DataWordBit	Sampling freq. 8 [KHz] BitClockFrequency [KHz]	Sampling freq. 16 [KHz] BitClockFrequency [KHz]
0	16 + 2	144	288
4	32 + 2	272	544

Tab. 6: Bit Clock frequency in burst mode

Hereafter are listed the AT commands used to cause the Module to enter Master configuration/PCM audio format (Burst mode).

Configure the Module to operate with PCM audio format (Burst mode)

DVI bus

AT#DVI=1,2,1
OK

1	enable DVI
2	use DVI port 2 (mandatory)
1	DVI Master (factory setting)

AT#DVIEXT=0,0,0,0,1
OK

0	Burst Mode
0	sample rate 8 KHz (factory setting)
0	16 bits per sample (factory setting)
0	Mono Mode
1	WAO transition is synchronized with the CLK rising edge.

No AT Commands example is give for the CODEC.

3.2.2. Module is Slave

In PCM audio format the MSB of the channel is clocked on the second CLK falling edge after the WAO pulse rising edge.

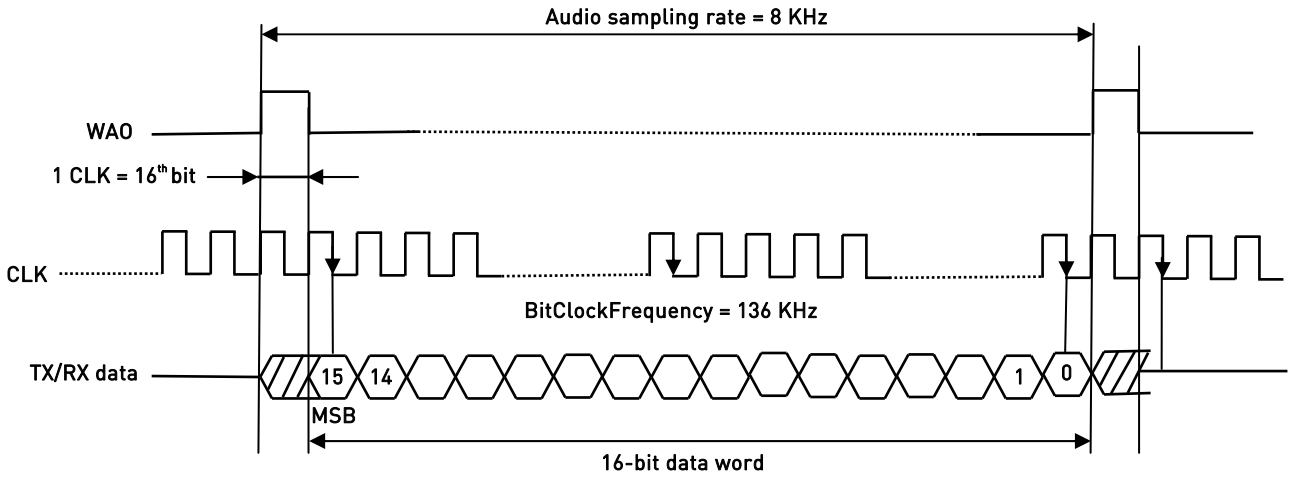


fig. 8: Timing diagram of PCM Audio Format (Burst mode) /Mono Mode

In general, the lower BitClockFrequency (CLK) is furnished by the following expression:

$$BitClockFrequency = (\ DataWordBit + 1 \ ) \times SamplingFrequency$$
$$BitClockFrequency = (\ 16 + 1 \ ) \times 8 = 136 \, KHz$$

Hereafter are listed the AT commands used to cause the Module to enter Slave configuration/PCM audio format (Burst mode) and configure the Codec in accordance with the current Module setting.

Configure the Module to operate with PCM audio format.

DVI bus

AT#DVI=1,2,0
OK

1	enable DVI
2	use DVI port 2 (mandatory)
0	DVI Slave

AT#DVIEXT=0,0,0,0,1
OK

0	Burst Mode
0	sample rate 8 KHz (factory setting)
0	16 bits per sample (factory setting)
0	Mono Mode
1	WAO transition is synchronized with the CLK rising edge.

Configure the Codec to operate with PCM audio format.

I^2C bus

AT#I2CWR=X,Y,30,4,19
> 00101000A40A330000330C0C09092424400060
OK

x	GPIO number used as SDA
y	GPIO number used as SCL
30	Device address on I^2C
4	Register address from which start the writing
19	number of bytes to write
>00101000.....refer to [2]	

AT#I2CWR=X,Y,30,17,1
>8A
OK

x	GPIO number used as SDA
y	GPIO number used as SCL
30	Device address on I^2C
17	Register address where write data
1	number of bytes to write
>8A	refer to [2]

The following figure shows the timing diagram, captured by an oscilloscope, concerning the above described example. The clock generated by the Codec is 384 KHz.

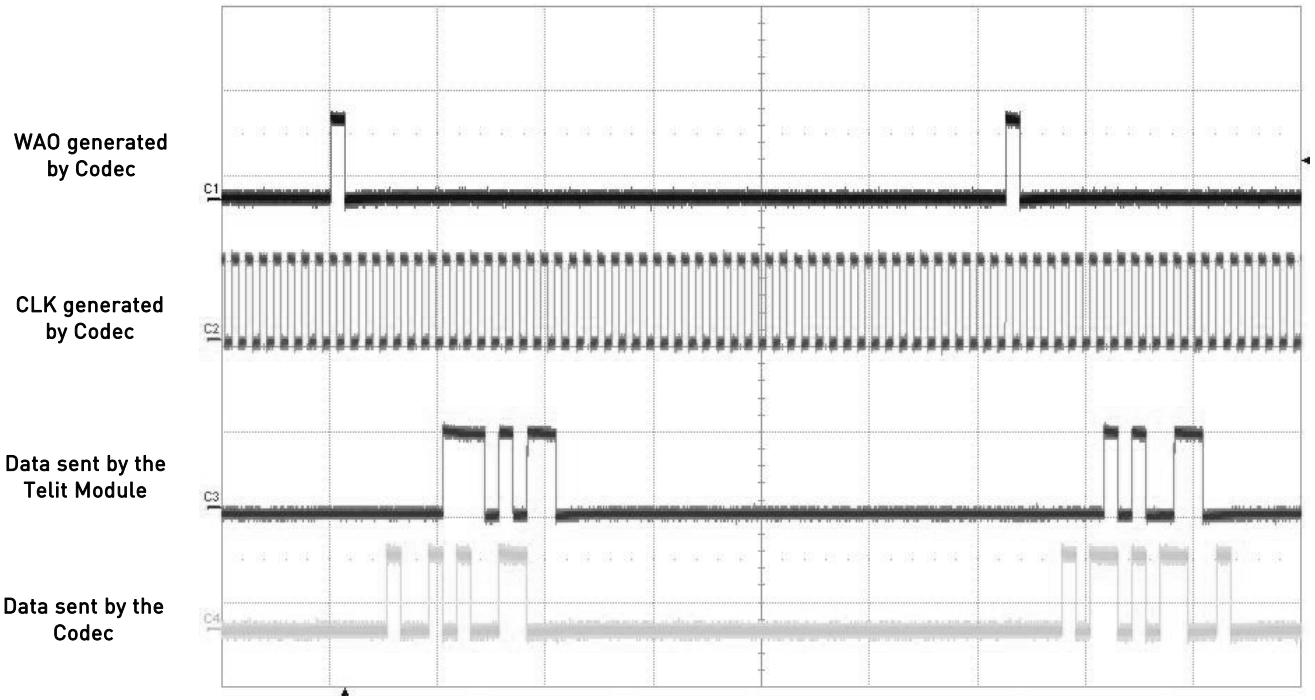


fig. 9: Timing Diagram of Module in Slave configuration/Burst mode

4. Annex

4.1. I²S Overview

This chapter furnishes a short description of the basic concept of the I²S bus in order to introduce the reader into the argument relating the digital audio transmission. This concept suitably modified is used by the I²S bus implemented on the HE910 family.

The I²S is an electrical serial bus designed for connecting digital audio devices. This popular serial bus has been developed by Philips® in 1986 as a 3-wire bus for interfacing to audio chips such as Codecs. It is a simple data interface, without any form of address or device selection.

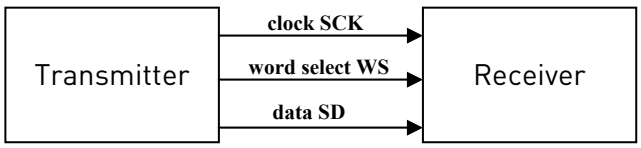
Refer to fig. 10: the I²S design handles audio data separately from clock signals. On an I²S bus, there is only one bus master and one transmitter.

In high-quality audio applications involving a Codec, the Codec is typically the master so that it has precise control over the I²S bus clock.

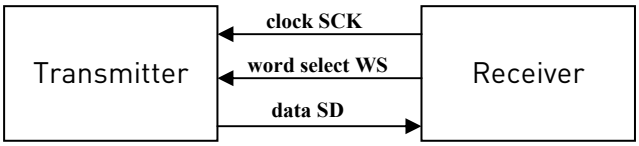
An I²S bus design consists of the following serial bus lines:

- SD: Serial Data
- WS: Word Select
- Serial Clock: SCK

The I²S bus carries two channels (left and right) 8 bit long, which are typically used to carry stereo audio data streams. The data alternates between left and right channels, as controlled by the word select signal driven by the bus master.



Transmitter = Master



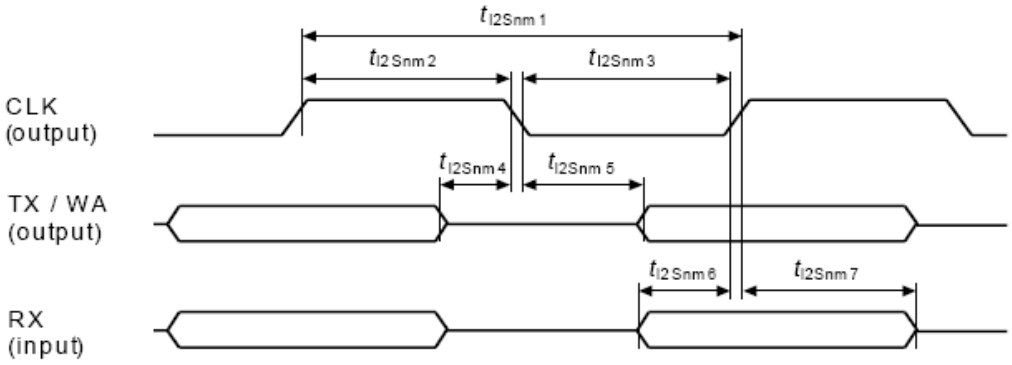
Receiver = Master

fig. 10: Simple I^2S bus configurations

4.2. DVI Timings

4.2.1. Normal Master Mode

The following diagram is showing the timings on the main DVI signals when in Normal Master Mode:



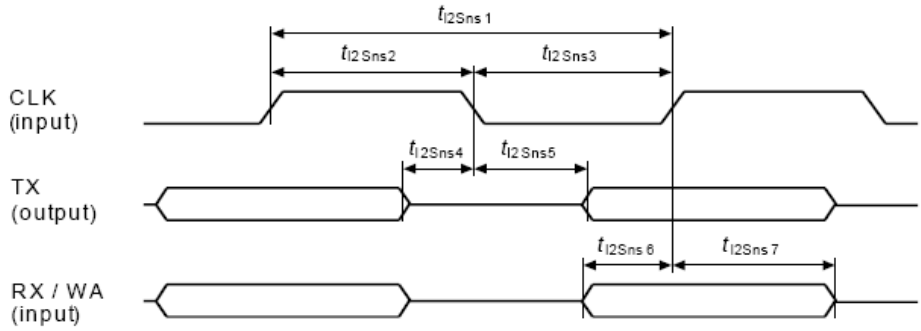
Normal Master Mode Parameters

Parameter	symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max		
CLK clock period	*t*I2Snm1	T-4ns	T	–	ns	T=M_T
CLK high time	*t*I2Snm2	T/2 - 20	T/2	–	ns	T=M_T
CLK low time	*t*I2Snm3	T/2 - 20	T/2	–	ns	T=M_T
TX invalid before CLK high end (before shifting edge of CLK)	*t*I2Snm4	–	–	24	ns	
TX valid after CLK low begin (after shifting edge of CLK)	*t*I2Snm5	–	–	2×tCP + 12	ns	tCP=9.6 ns
RX setup time before CLK low end (before latching edge of CLK)	*t*I2Sn m6	tCP + 50	–	–	ns	tCP=9.6 ns
RX hold time after CLK high begin (after latching edge of CLK)	*t*I2Snm7	10	–	–	ns	

NOTE: T corresponds to the audio sampling rate (16 kHz and 8 kHz) and to the frame length (16bit, 18bit, 20bit, 24bit or 32bit).

4.2.2. Normal Slave Mode

The following diagram is showing the timings on the main DVI signals when in Normal Slave Mode:



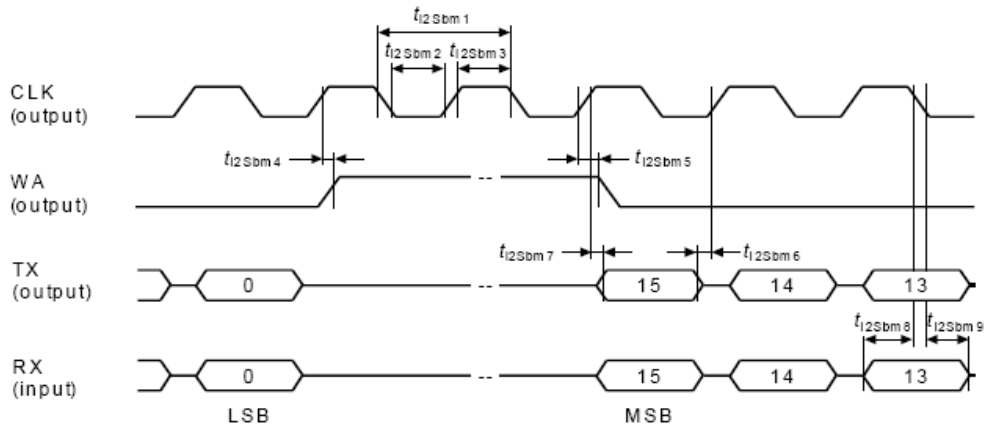
Normal Slave Mode Parameters

Parameter	symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max		
CLK clock period	*t*I2Sns1	T	–	–	ns	T=M_T
CLK high time	*t*I2Sns2	120	–	–	ns	
CLK low time	*t*I2Sns3	120	–	–	ns	
TX invalid before CLK falling edge	*t*I2Sns4	–	–	12	ns	
TX (continued) valid after CLK falling edge	*t*I2Sns5	–	–	3×tCP + 50	ns	tCP=9.6 ns
RX setup time before CLK rising edge (before latching edge of CLK)	*t*I2Sns6	tCP + 12	–	–	ns	tCP=9.6 ns
RX hold time after CLK rising edge (after latching edge of CLK)	*t*I2Sns7	24	–	–	ns	

NOTE: T corresponds to the audio sampling rate (16 kHz and 8 kHz) and to the frame length (16bit, 18bit, 20bit, 24bit or 32bit).

4.2.3. PCM Master Mode

The following diagram is showing the timings on the main DVI signals when in PCM Master Mode:



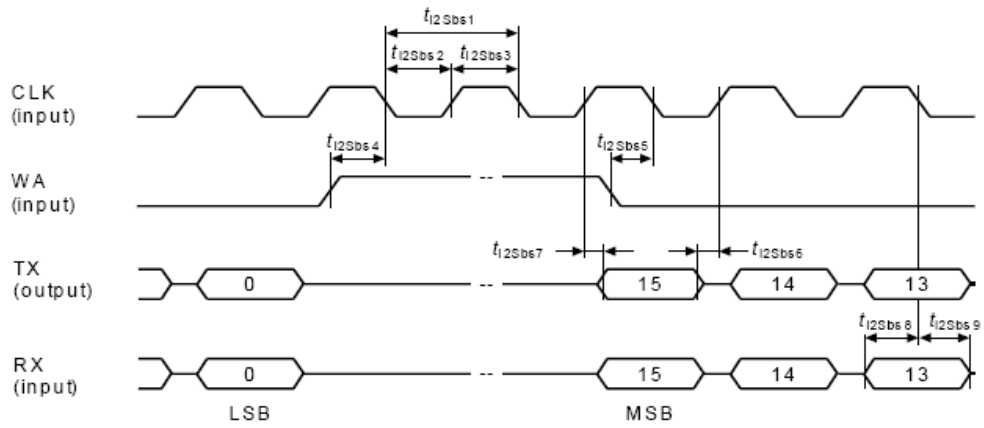
PCM Master Mode Parameters

Parameter	symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max		
CLK clock period	*t*I2Sbm1	T-4	T	–	ns	T=M_T
CLK low time	*t*I2Sbm2	T/2 - 20	T/2	–	ns	T=M_T
CLK high time	*t*I2Sbm3	T/2 - 20	T/2	–	ns	T=M_T
WA high begin after clock CLK high begin	*t*I2Sbm4	-24	–	2×tCP + 12	ns	tCP=9.6 ns
WA high end after CLK low end	*t*I2Sbm5	-24	–	2×tCP + 12	ns	tCP=9.6 ns
TX invalid before CLK low-end	*t*I2Sbm6	–	–	24	ns	
TX valid after CLK high begin	*t*I2Sbm7	–	–	tCP + 12	ns	tCP=9.6 ns
RX setup time before CLK high end	*t*I2Sb m8	tCP + 50	–	–	ns	tCP=9.6 ns
RX hold time after CLK low begin	*t*I2Sbm9	12	–	–	ns	

NOTE: T corresponds to the audio sampling rate (16 kHz and 8 kHz) and to the frame length (16bit, 18bit, 20bit, 24bit or 32bit).

4.2.4. PCM Slave Mode

The following diagram is showing the timings on the main DVI signals when in PCM Slave Mode:



PCM Slave Mode Parameters

Parameter	symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max		
CLK clock period	*t*I2Sbs1	T	–	–	ns	T=M_T
CLK low time	*t*I2Sbs2	120	–	–	ns	
CLK high time	*t*I2Sbs3	120	–	–	ns	
WA high begin before CLK low begin (latching edge of CLK)	*t*I2Sbs4	2×tCP + 17	–	–	ns	tCP=9.6 ns
WA low begin before CLK low begin (latching edge of CLK)	*t*I2Sbs5	2×tCP + 17	–	–	ns	tCP=9.6 ns
TX invalid before CLK rising edge (shifting edge of CLK)	*t*I2Sbs6	–	–	12	ns	
TX valid after CLK rising edge (shifting edge of CLK)	*t*I2Sbs7	–	–	3×tCP + 50	ns	tCP=9.6 ns
RX setup time before CLK falling edge	*t*I2Sb s8	tCP + 12	–	–	ns	tCP=9.6 ns
RX hold time after CLK falling edge	*t*I2Sbs9	24	–	–	ns	

NOTE: T corresponds to the audio sampling rate (16 kHz and 8 kHz) and to the frame length (16bit, 18bit, 20bit, 24bit or 32bit).

4.3. Schematic

A schematic example of an interface between the HE910 Telit Modules and the MAX9867 CODEC could be the following:

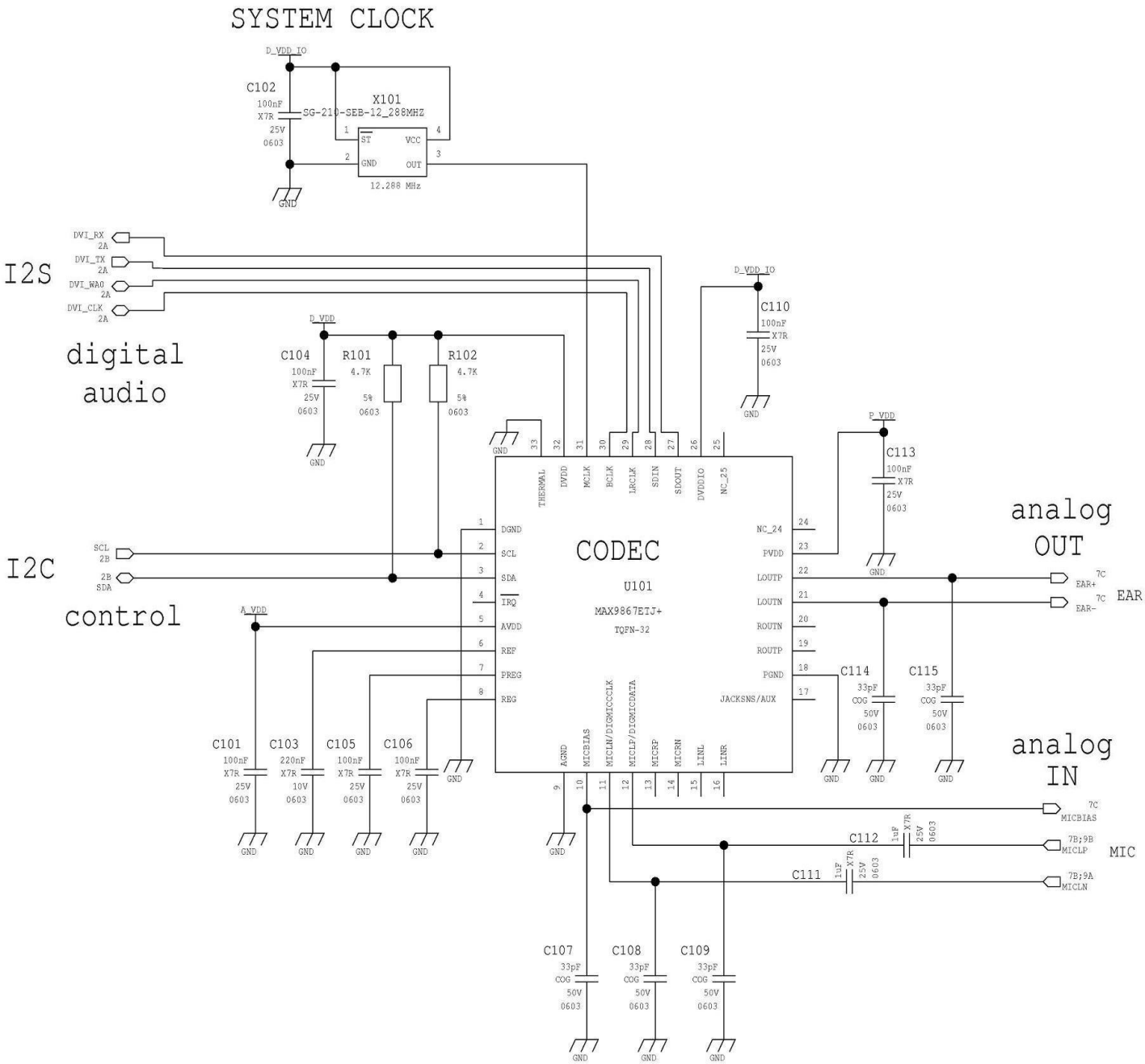


fig. 11: Schematic for Reference Design