Digital Voice Interface Application Note

80000NT10004a Rev. 4– 2010-10-04

Making machines talk.

APPLICABILITY TABLE

PRODUCT
GM862-QUAD
GM862-QUAD-PY
GM862-GPS
GC864-QUAD
GC864- PY
GC864-QUAD -C2
GC864- PY-C2
GE864-QUAD V2
GC864-QUAD V2
GE863-GPS
GE863- PY
GE863-QUAD
GE863-SIM
GE864- PY
GE864- QUAD
GE864-QUAD Automotive
GE864-QUAD Automotive V2
GE865-QUAD
GL865-DUAL

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Contents

1. Introduction

1.1. Scope

The aim of this document is the description of the *Digital Voice Interface* feature offered by the Telit modules that could be used in several applications, as example to connect the Wireless Module to a Bluetooth device.

1.2. Audience

This document is intended for helping Telit modules customer integrators.

1.3. Contact Information, Support

For general contact, technical support, to report documentation errors and to order manuals, contact Telit's Technical Support Center (TTSC) at:

TS-EMEA@telit.com
TS-NORTHAMERICA@telit.com
TS-LATINAMERICA@telit.com
TS-APAC@telit.com

Alternatively, use:

http://www.telit.com/en/products/technical-support-center/contact.php

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

http://www.telit.com

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Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

1.4. Document Organization

This document contains the following chapters.

Chapter 1: "*Introduction*" provides a scope for this document, target audience, contact and support information, and text conventions.

Chapter 2: "*Overview*" provides an overview of the document.

Chapter 3: "*Digital Interface Description*" . Physical, technical and protocol description.

Chapter 4: "*DVI on GM862, GE863 and GE864 families*". Deals with pinout of the DVI ports available in GM862, GE863 and GE864 Families .

Chapter 5: "*DVI on GE/GC864 V2 and GE865 families*". Deals with pinout of the DVI ports available in GE865 and GE864 V2 families.

Chapter 6: "*AT commands*". Deals with AT commands to use with DVI interface.

Chapter 7: "*Module interfacing*". Some suggestion about the use of the modules with a MAXIM ® codec .

Chapter 8: "*DVI pin positions on EVK2 adapters*" Deals with EVK2 adapters pinout.

Chapter 9: "*DVI implementations*".

Chapter 10 "*SAFETY RECOMMENDATIONS*".

1.5. Text Conventions

Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

1.6. Related Documents

- Telit's GSM/GPRS Family Software User Guide, 1vv0300784
- Audio settings application note , 80000NT10007a
- AT Commands Reference Guide, 80000ST10025a

1.7. Document History

Revision	Date	Changes
ISSUE#0	12/09/2007	First release
ISSUE#1	18/09/2008	Updated P/N list applicability table Added GE864-QUAD Automotive to Applicability List Updated protocol description Updated description of DVI port setting in Slave mode
ISSUE#2	15/01/2009	Updated applicability table Modified chapter 3 due to GE865-QUAD Automotive pin out description
ISSUE#3	16/03/2010	Document updated to general Telit template Chapter1 & 2 updated to general Telit template The chapter 3 is new Chapter 4 is the previous Chapter 8 but modified Chapter 5 is the previous Chapter 4 but modified The chapter 6 is new The chapter 7 is new Chapter 8 is the previous Chapter 9 but modified
ISSUE#4	2010-10-04	Added GL865-DUAL to the applicability table

2. Generality

This document cannot embrace the whole hardware solutions and products that may be designed. The suggested hardware configurations shall not be considered mandatory; instead the information given shall be used as a guide or a starting point for properly developing your product with the Telit modules.

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The following information can be applied both GM862, GE863 and GE/GC864 families and GE865 and GE/GC864 QUAD V2 families.

2.1. I2S Overview

The I2S Audio Interface (I2SBus or IISBus or I2SBus) is a serial bus designed for digital audio devices. This popular serial bus has been developed by Philips ® in 1986 as a 3-wire bus for interfacing to audio chips such as codecs. It is a simple data interface, without any form of address or device selection.

The I2S design handles audio data separately from clock signals. On an I2S bus, there is only one bus master and one transmitter: the master may be a transmitter, a receiver, or a controller for data transfers between other devices acting as transmitter and receiver.

In high-quality audio applications involving a codec, the codec is typically the master so that it has precise control over the I2S bus clock.

An I2S bus design consists of the following serial bus lines:

- a line with two time-division multiplexing (TDM) data channels **[SD]**
- a *word select* line **[WS]** , also called *Word Alignment* signal **[WA]**
- a clock line **[SCK]**

Data is transmitted two's complement (MSB first) and sent from the transmitter while the data synchronization is either the *high-to-low* or *low-to-high* transition of the clock signal ,the receiver latches the data on the *leading edge* of the clock signal.

The I2S bus carries two channels (left and right) 8 bit long, which are typically used to carry stereo audio data streams. The data alternates between left and right channels, as controlled by the word select signal driven by the bus master.

The Word Alignment signal **[WA]** is sent one clock before the useful data.

The I2S Bus uses standard TTL logic levels.

2.2. DVI description

The Digital Voice Interface is an I2S Audio Interface that works in PCM at 8 KHz Mono voice data.
It provides a bidirectional, synchronous, serial interface to off-chip audio devices.

The Telit Modules support the Digital Voice Interface (from here onwards DVI), which can be used to transfer digital audio data to and from the module itself.

In the rest of this document we will refer to it as DVI port.

WARNING: the Telit Modules can have one or two DVI ports, but only one can be active at the time. The choice between these two ports depends by the configuration of the alternate function of the interface pins on the customer applications.

Please refer to the pin-out section (or to User Guide of the module that you are using) for the available DVI ports.

WARNING: The DVI can be configured either as MASTER (clock output) or SLAVE (clock input), SLAVE mode being allowed only on DVI#1 port.

Both the analog audio block and the digital Audio block can be enabled at the same time (see AT command paragraph). This means that is the audio signals can be forwarded to AFE (microphone and loudspeaker) and to DVI, but the input signal comes from DVI only and not from analog input (microphone lines), while the output signal is sent to both DVI and analog output (headphone lines).

The DVI Volume is controlled by the same AT command as for the analog interface: for more information refer to the AT Commands Reference Guide for the Telit modules.

The Echo canceller feature is active both for DVI and for the analog audio.

2.2.1. Features summary

Used mode .....PCM mono voice data
Data valid.....on falling edge of clock transition
Operations mode..... Master and Slave
Transmission.....bi-directional (independent receiver and transmitter)
Sampling rate..... 8 kHz
Mode supported..... burst and continuous transmission
WA pulse length.....one clock cycle

2.3. Hint on PCM

Although analog communication is ideal for human communication, analog transmission is neither robust nor efficient at recovering from line noise.
As example in the early telephony network, when analog transmission was passed through amplifiers to boost the signal, not only was the voice boosted but the line noise was amplified, as well. This line noise resulted in an often-unusable connection.
It is much easier for digital samples, which are comprised of 1 and 0 bits, in order to be separated from line noise. Therefore, when analog signals are regenerated as digital samples, a clean sound is maintained.
PCM converts analog sounds into digital form by sampling the analog sounds 8000 times per second and converting each sample into a numeric code. If you sample an analog signal at twice the rate of the highest frequency of interest, you can accurately reconstruct that signal back into its analog form (Nyquist theorem). Because most speech content is below 4000Hz, a sampling rate of 8000 times per second (8KHz that means 125 µsec between samples) is required.

2.4. Signals

The DVI can be set to allow PCM data to be transferred from and to other devices. Only four signals are needed, because the Clock and Word Alignment are used for both receive and transmit direction. The Word Alignment signal (called WAO in the rest of this document) acts as frame synchronization signal, avoiding a continuous data transfer.

I2S Signal function	DVI Signal function	Description
Clock	DVI_CLK	Data Clock
Word Alignment	DVI_WAO	Frame Synchronism
serial audio data input	DVI_RX	Received Data
serial audio data output	DVI_TX	Transmitted Data

DVI signals table.

2.4.1. Electrical Characteristics

	Minimum	Maximum	Unit
V_{IL}	-0.2	0.55	V
V_{IH}	1.92	3.3	V
V_{OL}		0.2	V
V_{OH}	2.42		V

2.5. Mode of operation

The DVI operates in 16-bit data burst mode, starting with the most significant bit (MSB).

GSM voice is 13-bit 2's complement but the output of the speech decoder is saved on 16-bit 2's complement (Q15 format). The last 3 LSBs are equal to 0.

The data transmit operation works as follows:
At each falling edge of CLK, the state on the WAO line is checked. After a high level on WAO has been detected (syncro capture condition) the MSB of the transmit data is put on the TX line at the next rising edge of CLK.
Now the interface waits until a low level on WAO is detected during the falling edge of CLK (start bits shifting condition).

If this condition has been revealed, the interface shifts out the remaining data bits , one bit at each rising edge of CLK. As soon as all 16 bits have been transmitted a new data sample is transferred immediately from the TX buffer to a shift register. Thus, a continuous data transfer can be achieved.

The data receive operation works in nearly the same way.

The frame lasts for 17 clock pulses, because one more clock pulse is needed for the frame synchronization of the signal WAO.

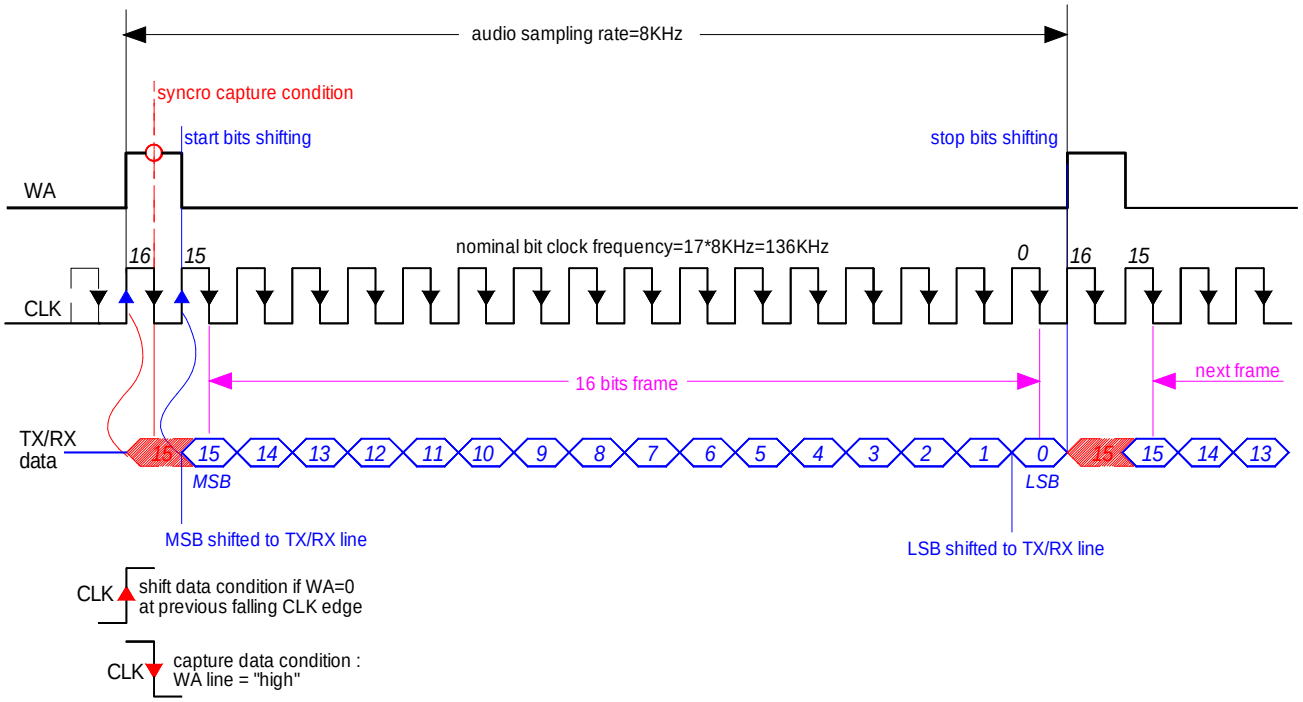


Figure 1 . Timing of Digital Voice Interface signal in PCM mode

2.6. Master mode Clock frequency

As described, in PCM mode each frame contains 16 data bits+1 WAO cycle; this results in a frame length of 17 shift clock cycles. Reminding that the audio sampling rate is 8KHz, the nominal bit clock frequency will be:

$$fclk = 8KHz * 17 = 136KHz$$

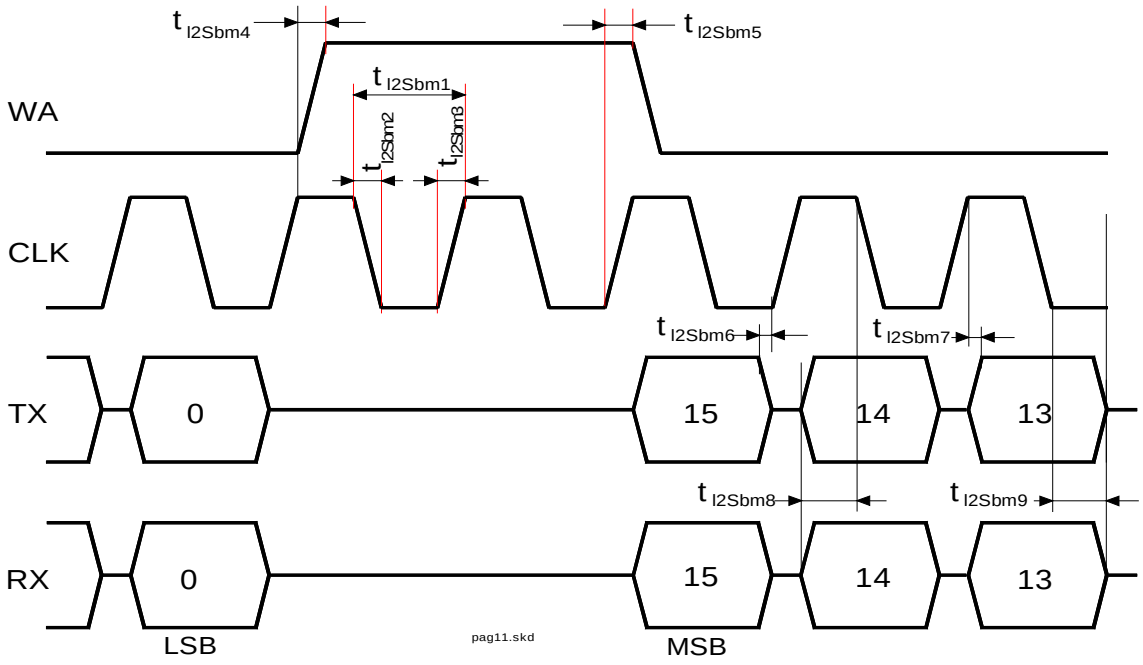
2.7. Timing characteristics

The DVIs can be configured both MASTER (the clock signal is internally generated) and SLAVE (the clock signal is externally generated) .

WARNING: with GM862, GE863 and GE/GC864 modules input), SLAVE mode is allowed on DVI#1 port only .

2.7.1. Master Mode

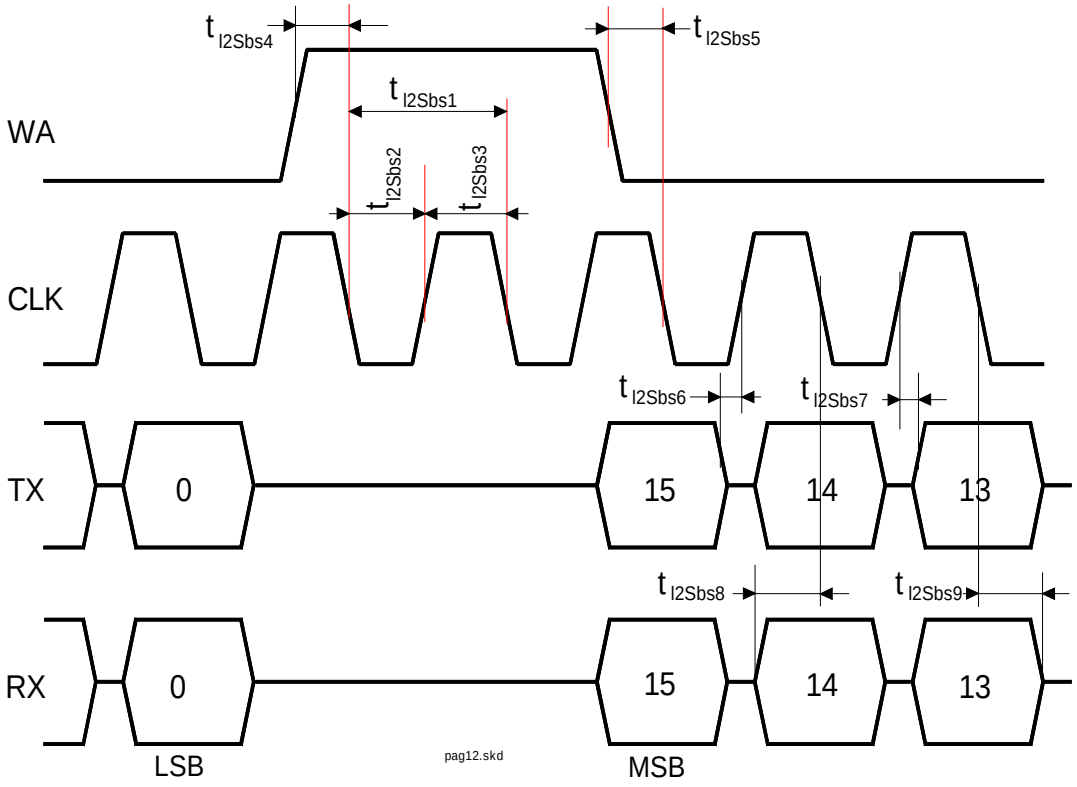
Parameter	Symbol	Limit Values			Unit
		Min	typ	Max	
DVI_CLK clock period	t_{I2Sbm1}	-	7,35[1]	-	µs
DVI_CLK low time	t_{I2Sbm2}	61			ns
DVI_CLK high time	t_{I2Sbm3}	61			ns
DVI_CLK low begin to DVI_WA high begin	t_{I2Sbm4}	-24		24	ns
DVI_WA low begin to DVI_CLK low begin	t_{I2Sbm5}	-24		24	ns
DVI_TX invalid before DVI_CLK0 low end	t_{I2Sbm6}			24	ns
DVI_TX valid after DVI_CLK0 high begin	t_{I2Sbm7}			24	ns
DVI_RX setup time before DVI_CLK1 high end	t_{I2Sbm8}	27			ns
DVI_RX hold time after DVI_CLK1 low begin	t_{I2Sbm9}	0			ns



[1] In MASTER mode the DVI provides CLK *(136KHz)* and WA *(8KHz)* signals.

2.7.2. Slave Mode

Parameter	Symbol	Limit Values		Unit
		Min	Max	
DVI_CLK clock period	t_{I2Sbs1}	306[2]	7,35	µs
DVI_CLK low time	t_{I2Sbs2}	n.a.		ns
DVI_CLK high time	t_{I2Sbs3}	n.a.		ns
DVI_CLK low begin to DVI_WA high begin	t_{I2Sbs4}	36		ns
DVI_WA low begin to DVI_CLK low begin	t_{I2Sbs5}	36		ns
DVI_TX invalid before DVI_CLK low end	t_{I2Sbs6}		0	ns
DVI_TX valid after DVI_CLK high begin	t_{I2Sbs7}		80	ns
DVI_RX setup time before DVI_CLK1 high end	t_{I2Sbs8}	24		ns
DVI_RX hold time after DVI_CLK1 low begin	t_{I2Sbs9}	24		ns



[2] Values of clock rate are from 136KHz to 3.25 MHz

3. AT Commands

The following table shows the *AT commands* which activate and control all *DVI* functions .

#DVI - Digital Voiceband Interface	
AT#DVI=<mode>[,<dviport>,<clockmode>]	Set command enables/disables the Digital Voiceband Interface. Parameters: **<mode>** - enables/disables the DVI. 0 - disable DVI; audio is forwarded to the analog line; DVI pins can be used for other purposes, like GPIO, etc. (factory default) 1 - enable DVI; audio is forwarded to the DVI block 2 - enable DVI; audio is forwarded both to the DVI block and to the analog lines (Note: analog input disabled) **<dviport>** 1 - DVI port 1 will be used (factory default) 2 - DVI port 2 will be used (see Test Command for availability of this port) **<clockmode>** 0 - DVI slave 1 - DVI master (factory default) Note: setting **<clockmode>=0** has full effect only if **<dviport>=1** NOTE: DVI slave is available only on port 1 NOTE: for further information see "Digital Voice Interface Application Note" (Rev. 2)
AT#DVI?	Read command reports last setting, in the format: **#DVI: <mode>,<dviport>,<clockmode>**
AT#DVI=?	Test command reports the range of supported values for parameters **<mode>,<dviport>** and **<clockmode>**
Example	AT#DVI=2,1,1 OK *Both analog and DVI activated for audio. DVI is configured as master providing on DVI Port #1*

4. Modules Pin-out

In the following paragraphs you can find the cross list between the ***DVI*** signals and their physical positions on the Telit modules.

4.1. GM862, GE863 and GE/GC864 Families

4.1.1. GM862

The GM862-QUAD/PY Modules family has **DVI#1 port** available on the system interface.
Bear in mind that activating the **DVI** on the GM862 modules restricts commonly used functions on the module , such as the trace serial port and the DSR signal on the AT command port.
Remember also that the GM862-GPS module **does NOT support** the **DVI,** due to physical interface restrictions.
The connections to the application are made through SO602, a 50-pins PTH connector.

4.1.1.1. DVI Port1 pin-out

DVI Function	Module Function	SO602
DVI1_CLK	I2S1-CLK0	35
DVI1_ WAO	I2S1-WAO	41
DVI1_ RX	I2S1-RX	33
DVI1_TX	I2S1-TX	46

4.1.2. GE863 family

Due to physical interface restrictions, the GE863 Modules family (GE863-GPS, GE863-PY, GE863-SIM and GE863-QUAD) has only the ***DVI# 2*** port available on the system interface.

The connections to the application is made through the BGA system

4.1.2.1. DVI Port#2 pinout

DVI Function	Module Function	Ball
DVI2_CLK	I2S2-CLK0	32
DVI2_WAO	I2S2-WAO	59
DVI2_RX	I2S2-RX	76
DVI2_TX	I2S2-TX	4

4.1.3. GE864-QUAD/PY

The ***GE864-QUAD/PY*** has two ***DVI*** ports at disposal on the system interface, selectable and active one at time only.
The choice depends by the use of the alternate function of the interface ***DVI*** pins on the customer applications. However Telit suggests in *"Master Mode" the* use of the ***DVI#2*** port to minimize the impact on the module functionality on applications.

The connections to the application is made through the BGA system

4.1.3.1. DVI Port#1 pinout

DVI Function	Module Function	Ball
DVI1_CLK	I2S1-CLK0	D11
DVI1 _WAO	I2S1-WAO	F10
DVI1 _RX	I2S1-RX	E11
DVI1_TX	I2S1-TX	C6

4.1.3.2. DVI Port#2 pinout

DVI Function	Module Function	Ball
DVI2_CLK	I2S2-CLK0	D7
DVI2_WAO	I2S2-WAO	H5
DVI2_RX	I2S2-RX	K7
DVI2_TX	I2S2-TX	H3

4.1.4. GC864-QUAD

This Module has two ***DVI ports*** on the system interface.
The connection to the application is made through PL301, a 80 pin SMT connector.

Only one port can be selected and active at the time, depending by the use of the alternate function of the interface ***DVI*** pins on the customer applications. However Telit suggests the use of the ***DVI#2*** port to minimize the impact on the module functionality on applications.

4.1.4.1. DVI Port#1 pinout

DVI Function	Module Function	PL301
DVI1_CLK	I2S1-CLK0	24
DVI1 _WAO	I2S1-WAO	23
DVI1 _RX	I2S1-RX	27
DVI1_TX	I2S1-TX	35

4.1.4.2. DVI Port#2 pinout

DVI Function	Module Function	PL301
DVI2_CLK	I2S2-CLK0	36
DVI2_WAO	I2S2-WAO	71
DVI2_RX	I2S2-RX	65
DVI2_TX	I2S2-TX	63

4.1.5. GE864-QUAD Automotive

The ***GE864-QUAD Automotive*** has only ***DVI #2 port***.
The connections to the application are made through the ***BGA*** system.

4.1.5.1. DVI Port#2 pinout

DVI Function	Module Function	Ball
DVI2_CLK	I2S2-CLK0	D7
DVI2_WAO	I2S2-WAO	H5
DVI2_RX	I2S2-RX	K7
DVI2_TX	I2S2-TX	H3

4.1.6. GC864-C2

Due to physical interface restrictions, the GC864-QUAD/PY C2 family has only DVI***#1 port*** at disposal on the system interface.
The connection to the application is made through PL103, a 60 pin SMT connector.

4.1.6.1. DVI Port#1 pinout

DVI Function	Module Function	PL103
DVI1_CLK	I2S1-CLK0	52
DVI1 _WAO	I2S1-WAO	51
DVI1 _RX	I2S1-RX	47
DVI1_TX	I2S1-TX	48

4.2. GE865 and GE/GC864 QUAD V2 variants

4.2.1. GE864-QUAD V2, GE864-QUAD Automotive V2

The GE864-QUAD V2 (and also Automotive V2) has only ***DVI#1*** port available on the system interface.
The connection to the application is made through the BGA system.

4.2.1.1. DVI Port#1 pinout

DVI Function	Module Function	Ball
DVI1_CLK	SSC0_CLK	D7
DVI1 _WAO	SSC0_MTSR	H5
DVI1 _RX	SSC0_MRST	K7
DVI1_TX	DISP_REST	H3

4.2.2. GC864-QUAD V2

The GC864-QUAD V2 has only ***DVI#1*** port available on the system interface.
The connection to the application is made through PL301, a 80 pins SMT connector.

4.2.2.1. DVI Port#1 pinout

DVI Function	Module Function	PL301
DVI1_CLK	SSC0_CLK	B4
DVI1 _WAO	SSC0_MTSR	C5
DVI1 _RX	SSC0_MRST	B5
DVI1_TX	DISP_REST	B3

4.2.3. GE865-QUAD

The GE865-QUAD V2 has only ***DVI#1*** port available on the system interface.
The connections to the application are made through the BGA system.

4.2.3.1. DVI Port#1 pinout

DVI Function	Module Function	Ball
DVI1_CLK	SSC0_CLK	D4
DVI1 _WAO	SSC0_MTSR	D3
DVI1 _RX	SSC0_MRST	D2
DVI1_TX	DISP_REST	E4

5. DVI pin positions on EVK2 adapters

Before designing their own applications, Telit offers to the customers the possibility to evaluate the module performance using THE an Evaluation kit EVK2 , on which it is possible to fit every module fitted on its own adapter interface .

The ***DVI*** functionality pins are at disposal on the adapter connectors and/or on EVK2 connectors.

The following paragraphs summarize the DVI ports pin positions on the EVK2 and/or adapters connectors (for further information, refer to EVK2 User Guide).

5.1. GE862, GE863, GE/GC864 families

5.1.1. GM862 adapter CS1150b

		EVK2	CS1150b
DVI Function	**Pin Function**	**SO101**	**PL103**
DVI1_CLK	TX_TRACE/TX_GPS	2	
DVI1 _WAO	RX_TRACE/RX_GPS	3	
DVI1 _RX	C107/DSR	20	
DVI1_TX	GPIO03/CAM_SCL_IIC_SCL		14

5.1.2. GE863 adapter CS1151a

		CS1151a	
DVI Function	**Pin Function**	**PL103**	**PL104**
DVI2_CLK	GPIO4/CAM_SDA/IIC_SDA		13
DVI2_WAO	GPIO17/PCM_WA0	19	
DVI2_RX	GPIO18/PCM_RX	17	
DVI2_TX	GPIO10/PCM_TX		7

5.1.3. GE864 adapter CS1152b

		EVK2	CS1152b	
DVI Function	**Pin Function**	**SO101**	**PL101**	**PL102**
DVI1_CLK	TX_TRACE	2		
DVI1 _WA	RX_TRACE	3		
DVI1 _RX	C107/DSR	20		
DVI1_TX	CAM_SCL/IIC_SCL			14
DVI2_CLK	CAM_SDA/IIC_SDA			13
DVI2_WA	TGPIO_17/PCM_WA0		19	
DVI2_RX	TGPIO_18/PCM_RX		17	
DVI2_TX	TGPIO_10/PCM_TX			7

5.1.4. GE864-QUAD Automotive adapter CS1302

		CS1302d	
DVI Function	**Pin Function**	**PL101**	**PL102**
DVI1_CLK	CAM_SDA/IIC_SDA		13
DVI1_WA0	TGPIO_17	19	
DVI1_RX	TGPIO_18	17	
DVI1_TX	TGPIO_10		7

5.1.5. GC864 adapter CS1203b

		EVK2	CS1203b	
DVI Function	**Pin Function**	**SO101**	**PL101**	**PL102**
DVI1_CLK	TX_TRACE	2		
DVI1 _WA	RX_TRACE	3		
DVI1 _RX	C107/DSR	20		
DVI1_TX	CAM_SCL/IIC_SCL			14
DVI2_CLK	CAM_SDA/IIC_SDA			13
DVI2_WA	TGPIO_17/PCM_WA0		19	
DVI2_RX	TGPIO_18/PCM_RX		17	
DVI2_TX	TGPIO_10/PCM_TX			7

5.1.6. GC864-C2 adapter CS1231

		EVK2	CS1231	
DVI Function	Pin Function	SO103	PL101	PL102
DVI1_CLK	TX_TRACE	52		13
DVI1 _WAO	RX_TRACE	51	19	
DVI1 _RX	C107/DSR	47	17	
DVI1_TX	CAM_SCL/IIC_SCL	48		7

5.2. GE865 and GE/GC864 QUAD V2, QUAD Automotive variant families

5.2.1. GE865-QUAD V2 adapter CS1324a

		CS1324a
DVI Function	Pin Function	PL104
DVI1_CLK	GPIO08	4
DVI1 _WAO	GPIO01	2
DVI1 _RX	GPIO02	1
DVI1_TX	GPIO03	3

5.2.2. GE864-QUAD V2 adapter CS1152b

		CS1152b	
DVI Function	Pin Function	PL101	PL102
DVI1_CLK	CAM_SDA/IIC_SDA		13
DVI1 _WAO	TGPIO_17	19	
DVI1 _RX	TGPIO_18	17	
DVI1_TX	TGPIO_10		7

5.2.3. GE864-QUAD Automotive V2 adapter CS1302d

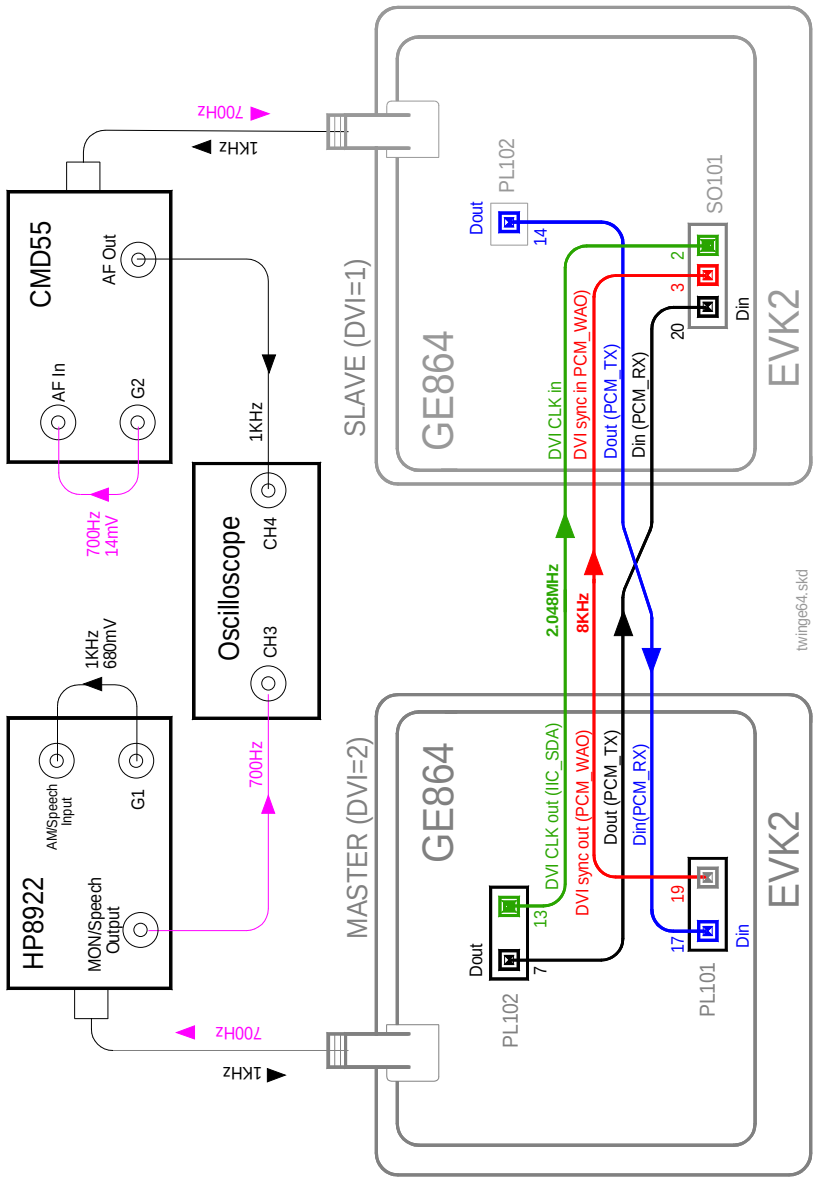
		CS1302d	
DVI Function	**Pin Function**	**PL101**	**PL102**
DVI1_CLK	CAM_SDA/IIC_SDA		13
DVI1 _WAO	TGPIO_17	19	
DVI1 _RX	TGPIO_18	17	
DVI1_TX	TGPIO_10		7

5.2.4. GC864-QUAD V2 adapter CS1203b

		CS1203b	
DVI Function	**Pin Function**	**PL101**	**PL102**
DVI1_CLK	CAM_SDA/IIC_SDA		13
DVI1 _WA	TGPIO17	19	
DVI1 _RX	TGPIO18	17	
DVI1_TX	TGPIO10		7

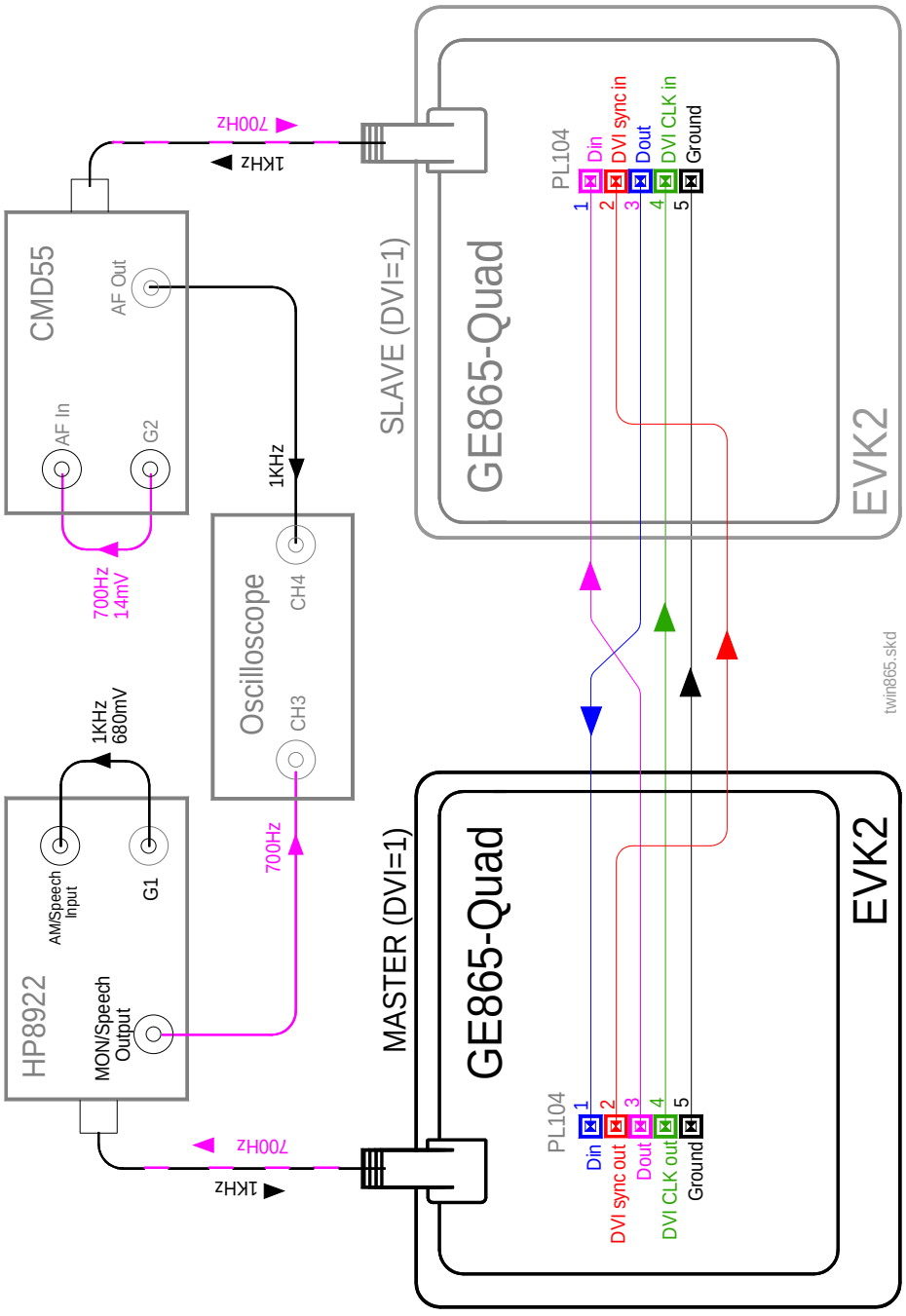
6. DVI implementation examples

6.1. GM862,GE863 and GE/GC864 families

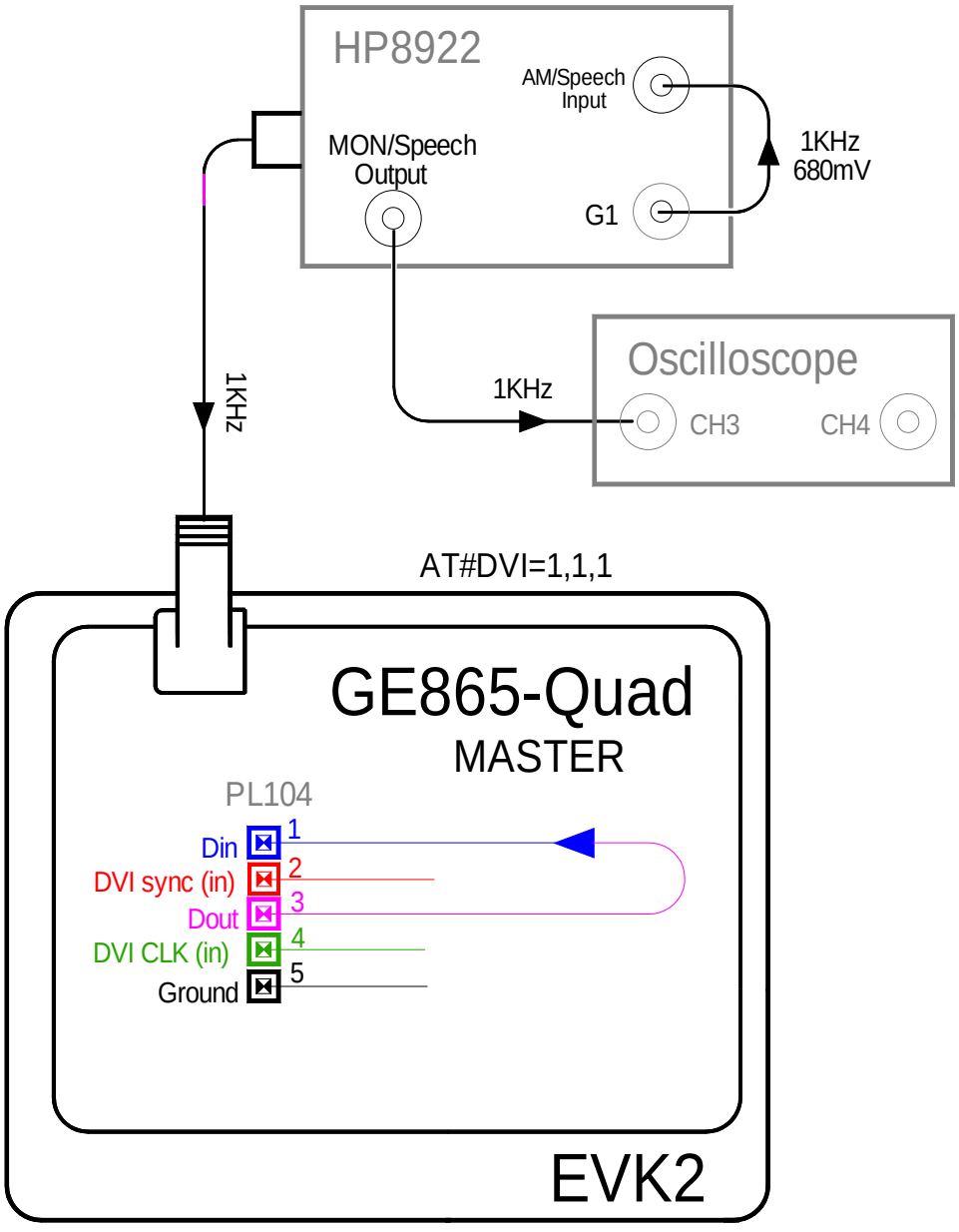


Two modules are cross connected (Data Input ⟷ Data Output) to Base Station Simulators : one is MASTER configured and the second is SLAVE configured (using DVI#1 port) .

6.2. GE865 and GE/GC864-QUAD V2 and Automotive V2 variant

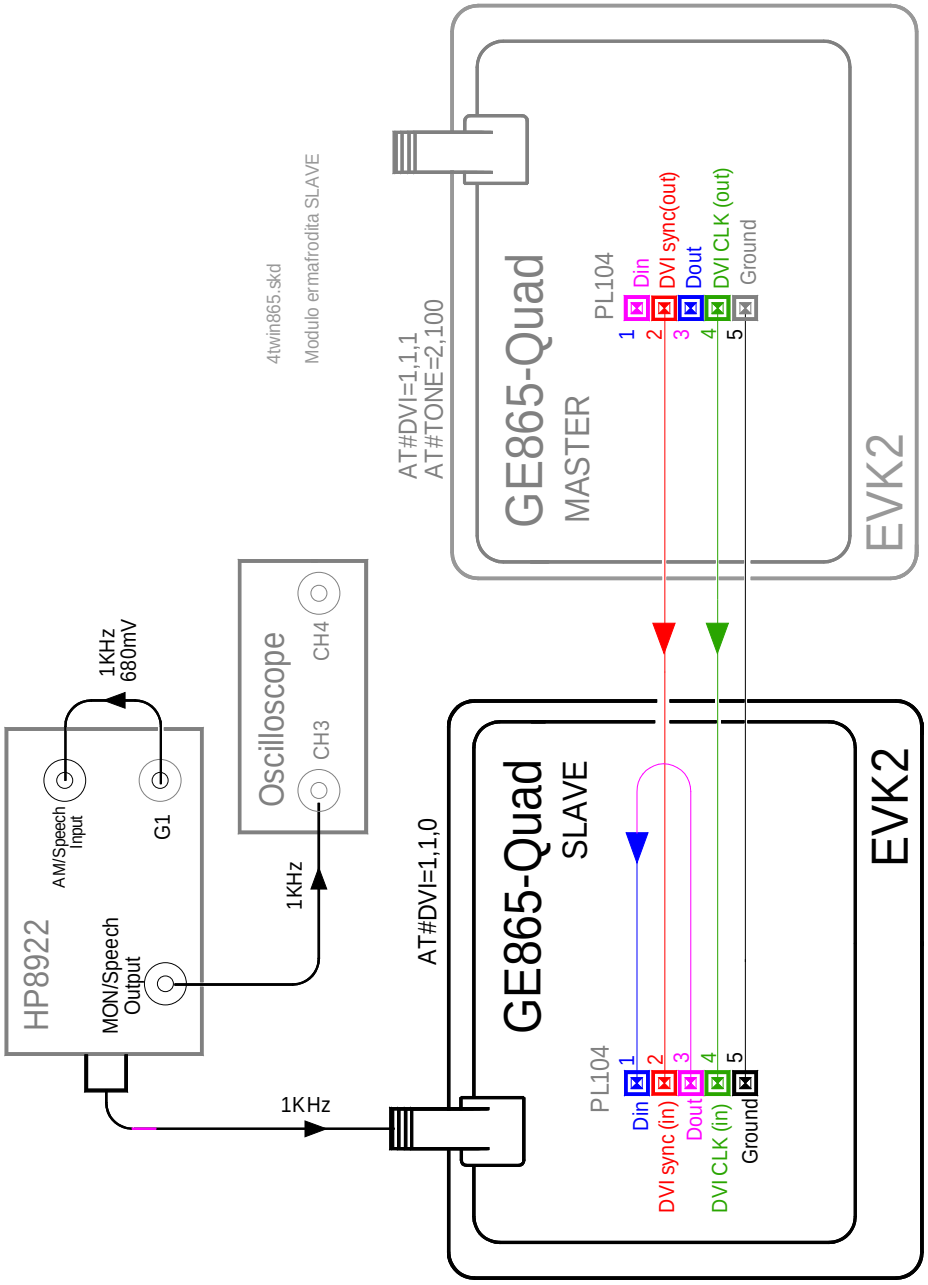


One Module works in MASTER mode; the second one works in SLAVE mode.
They are cross connected (Data Input ↔ Data Output) to the Base Station Simulators.
Both modules use the DVI#1 port.



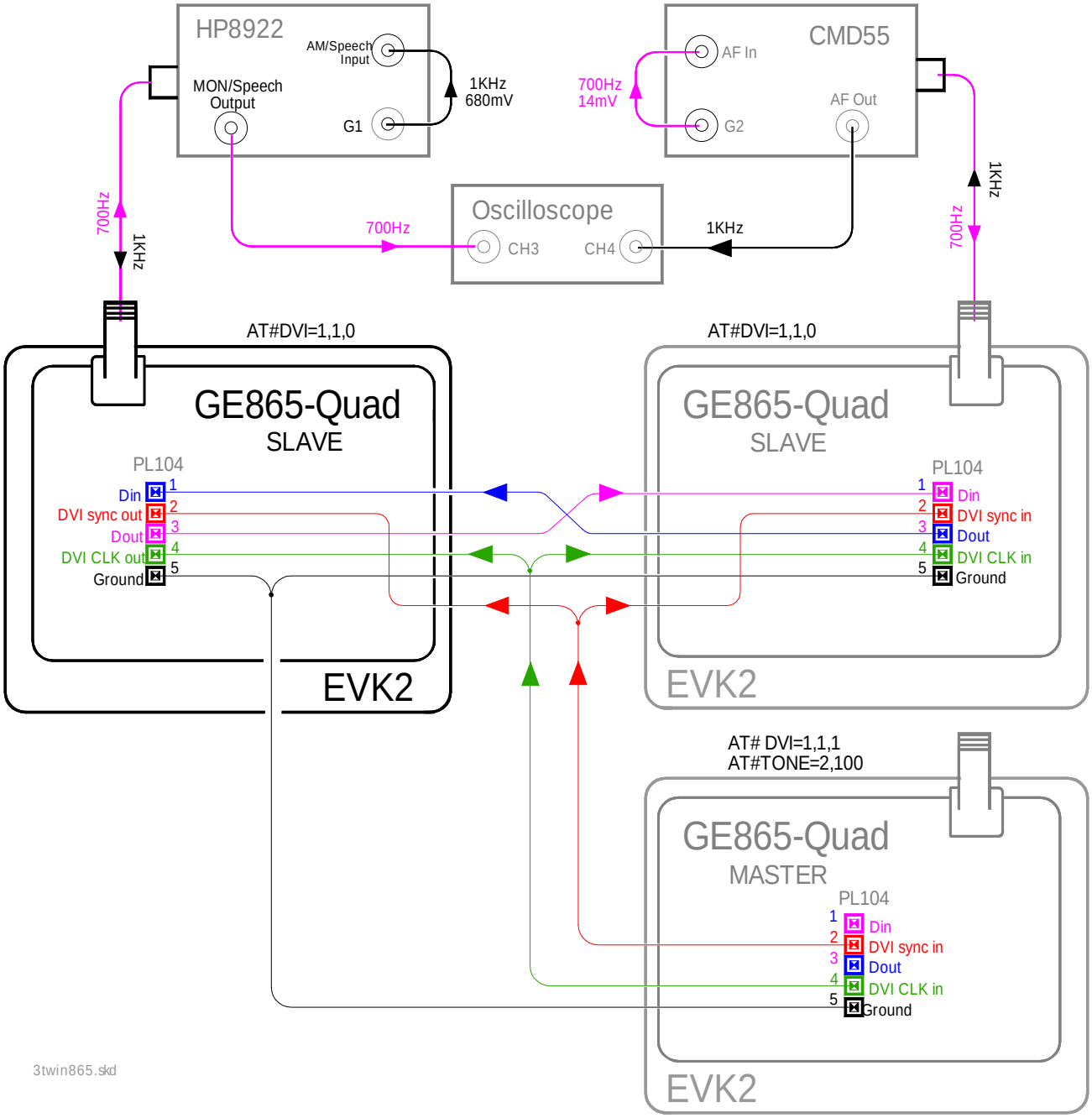
5twin865.skd
Modulo ermafrodita MASTER

The single Module works in Master Mode (DVI#1 enabled) .
It is configured as "hermaphrodite" (its output data pin is connected to its own input data pin) and connected to a Base Station Simulator.
In such a way the audio signal injected to *BSS* AF Input is outputted at *BSS* AF Output.

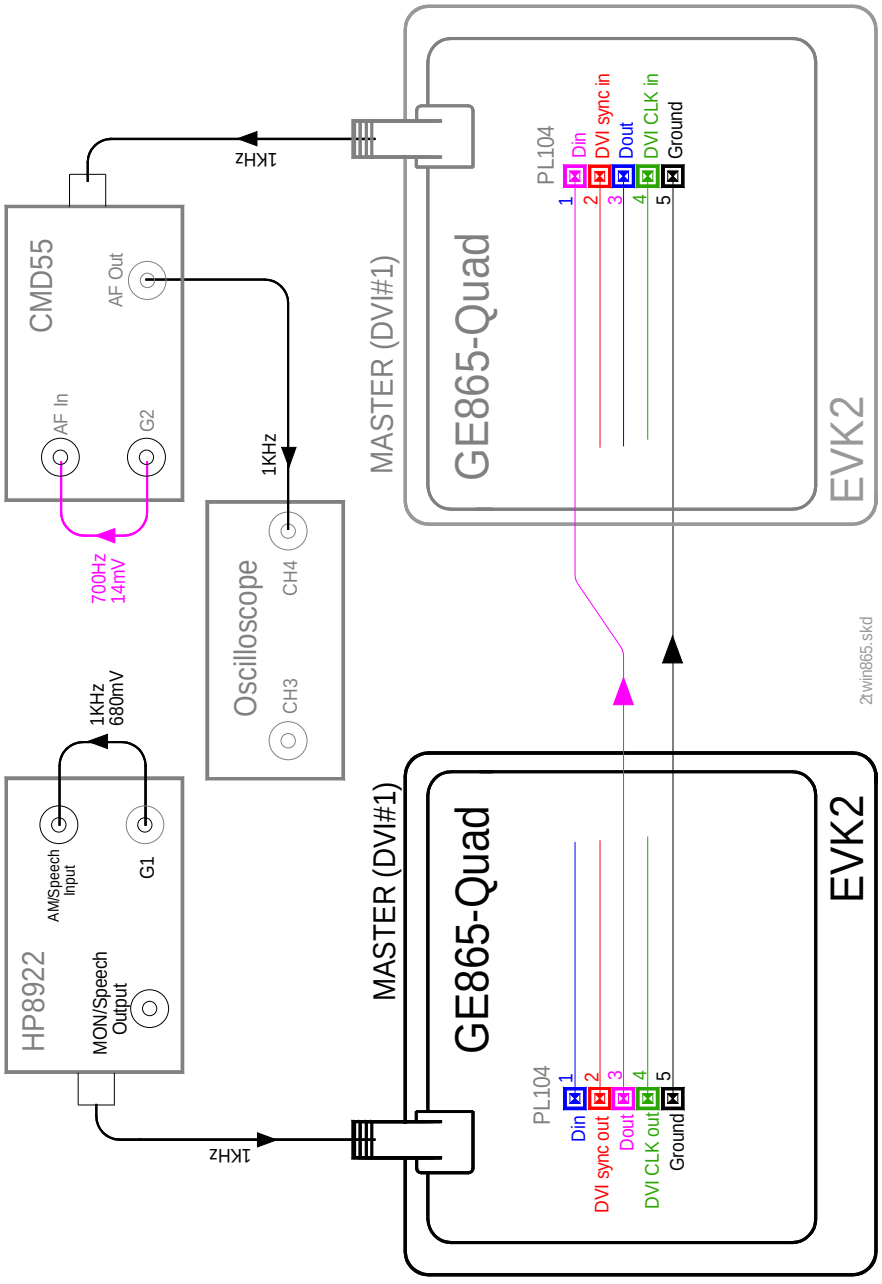


One "hermaphrodite configured" Module (its output data pin is connected to its own input data pin) works in SLAVE mode and it is connected to the Base Station Simulator.
A second Module works in MASTER Mode, supplying the Clock and Sync signals to the previous one.

Both Modules use the ***DVI#1*** port



One module works in MASTER Mode: it supplies the clock and sync signals to 2 Modules, connected to the Base Station Simulators.
All three modules use the ***DVI#1*** port.

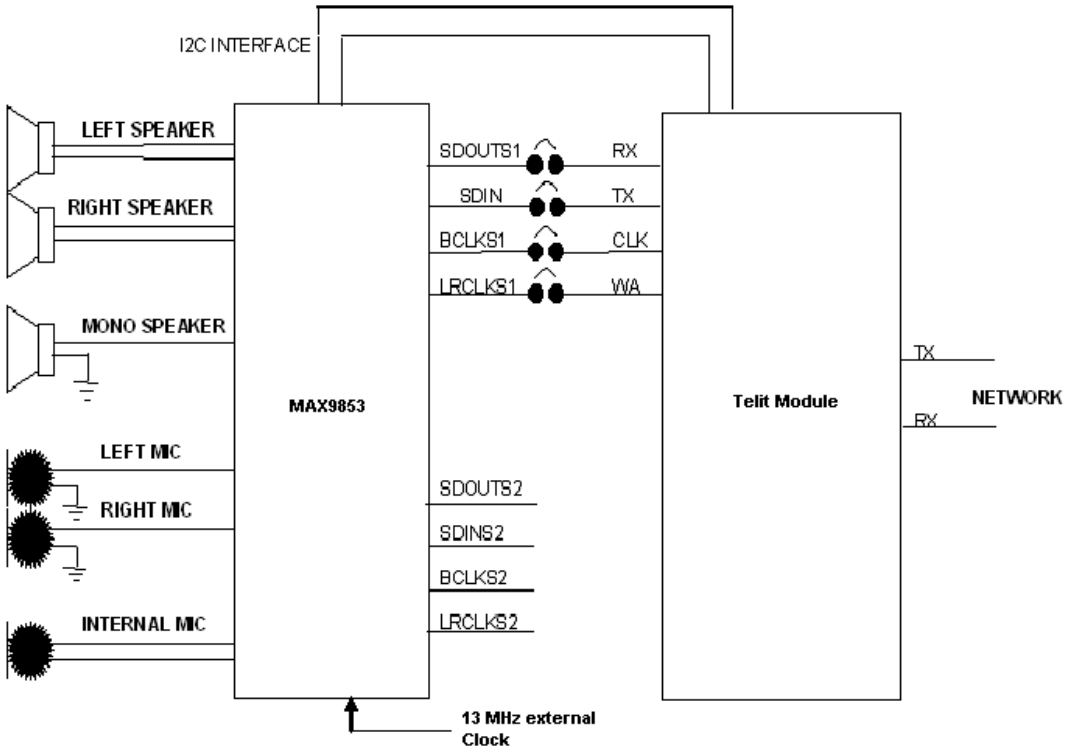


Two modules working in MASTER mode are connected to Base Station Simulators; the ***DVI#1*** port is activated on and both devices .

7. Interfacing an external codec

Here we described a possible application of the DVI: the audio signals are sent to and received from of an external Codec , the MAX9853 ® from MAXIM.
This device is a stereo audio codec with two digital interfaces, supporting various audio formats and has the voice mode compatible with the module's DVI.

The figure below shows the typical block level schematic.



This application has been realized with the module configured as Master, at 136 KHz clock rate, enabling the #1 serial digital interface of the codec, set as Slave in 8KHz voice mode.

As power supply to the analog (AVdd) and digital (DVdd) part of the codec could be used the ***VAUX1*** voltage from the module, while the positive supply for the speakers (PVdd) could be the ***VBatt***.

Because the GM862 family modules, GE865 and GE/GC864 family modules do not provide the *VAUX1* power supply, in this case it will be necessary to add an external LDO.

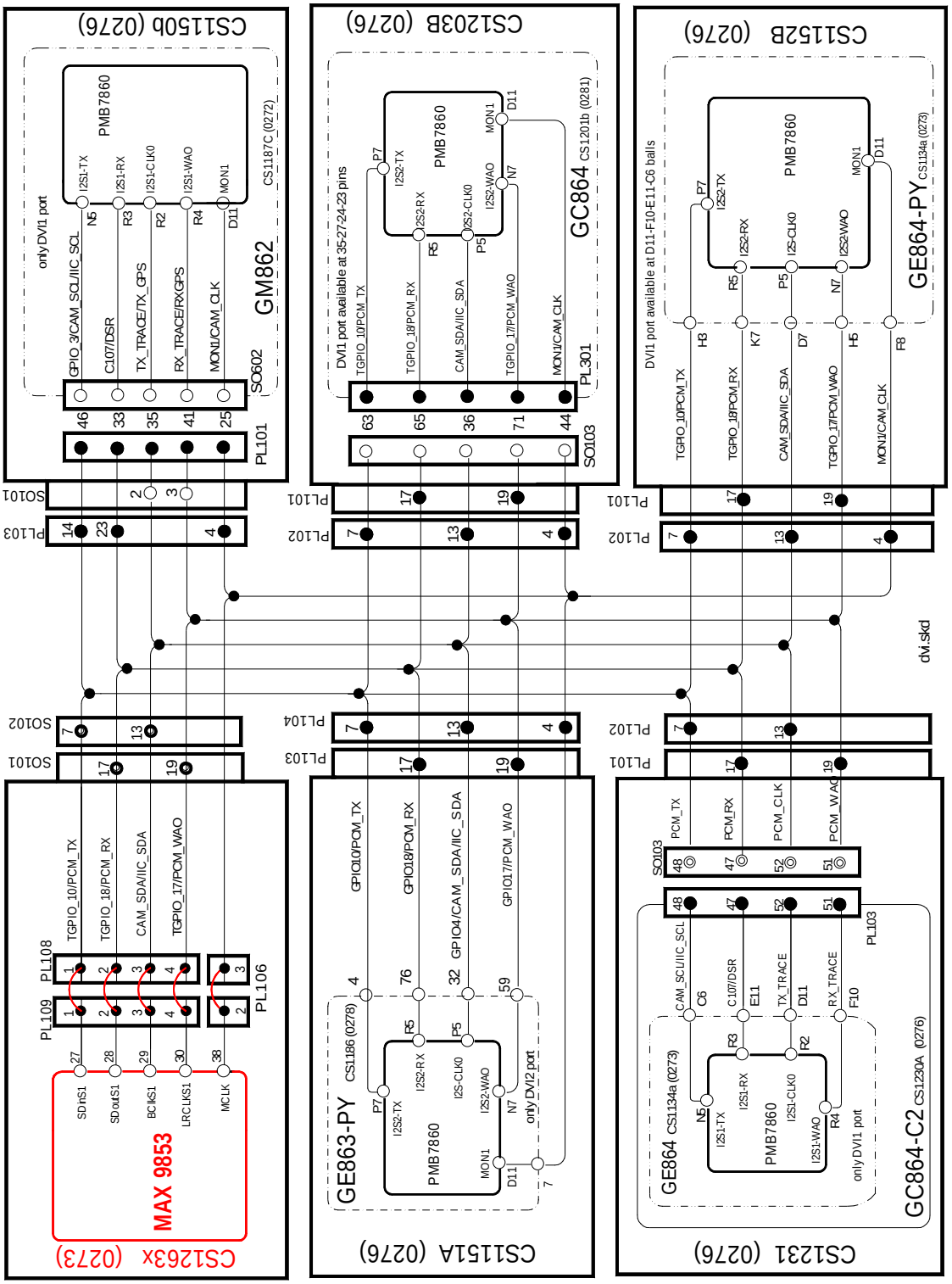
The Telit module configures and controls the external codec through an I2C interface (this is done in a Python script using 2 GPIOs).

Refer to the Telit module's HW User Guide for all information regarding the GPIOs to be used and to the document Easy Script in Python regarding the script needed for the I2C communication.

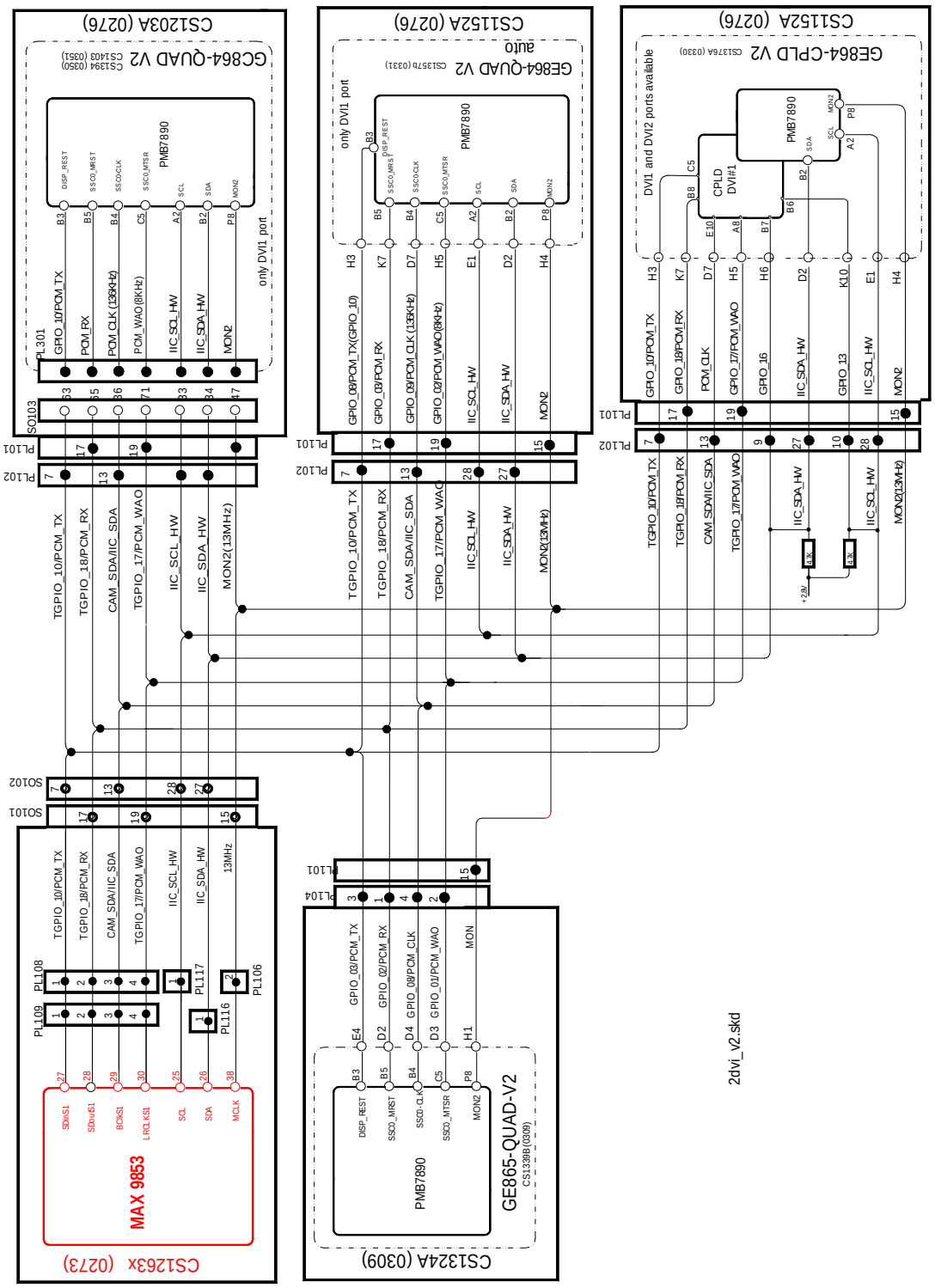
The following I2C commands are sent to the codec to configure it this example:

I2C Device address	***Register address***	***Data***	***Description***
0x20	0x03	0xca	Enable digital audio 8 KHz mono voice mode on left channel
	0x04	0x20 *or* 0x00	Digital interface as slave and clock polarity
	0x0a	0x22	Enable left microphone input
	0x0b	0x10	Left DAC to analog output
	0x18	0x10	Enable only left speaker
	0x1a	0xf5	System Clock control
	0x1b	0xa2	Enable ADC and DAC
	0x12	0x07	Microphone control
	0x08	0x22	Mix the digital interface 1

7.1. Connections with GM862,GE863 and GE/GC864 Modules



7.2. Connections with GE865 and GE/CG864 QUAD V2 Modules



8. SAFETY RECOMMENDATIONS

NOTE. Read this section carefully to ensure the safe operation.

Be sure the use of this product is allowed in the country and in the environment required. The use of this product may be dangerous and has to be avoided in the following areas:

- Where it can interfere with other electronic devices in environments such as hospitals, airports, aircrafts, etc
- Where there is risk of explosion such as gasoline stations, oil refineries.

It is responsibility of the user to enforce the country regulation and the specific environment regulation.

Do not disassemble the product; any mark of tampering will compromise the warranty validity.

We recommend following the instructions of the hardware user guides for a correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to be conforming to the security and fire prevention regulations.

The product has to be handled with care, avoiding any contact with the pins because electrostatic discharges may damage the product itself. Same cautions have to be taken for the SIM, checking carefully the instruction for its use. Do not insert or remove the SIM when the product is in power saving mode.

The system integrator is responsible of the functioning of the final product; therefore, care has to be taken to the external components of the module, as well as of any project or installation issue, because the risk of disturbing the GSM network or external devices or having impact on the security. Should there be any doubt, please refer to the technical documentation and the regulations in force.

Every module has to be equipped with a proper antenna with specific characteristics. The antenna has to be installed with care in order to avoid any interference with other electronic devices and has to guarantee a minimum distance from the body (20 cm). In case of this requirement cannot be satisfied, the system integrator has to assess the final product against the SAR regulation EN 50360.

The European Community provides some Directives for the electronic equipments introduced on the market. All the relevant information are available on the European Community website:

http://europa.eu.int/comm/enterprise/rtte/dir99-5.htm

The text of the Directive 99/05 regarding telecommunication equipments is available, while the applicable Directives (Low Voltage and EMC) are available at:

http://europa.eu.int/comm/enterprise/electr_equipment/index_en.htm