# RE866-EU
# Hardware User Guide

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# APPLICABILITY TABLE

## PRODUCTS

- RE866A1-EU

# Contents

# 1. INTRODUCTION

## 1.1. Scope

The aim of this document is the description of some hardware solutions useful for developing a product with the Telit RE866 module.

## 1.2. Audience

This document is intended for Telit customers, who are integrators, about to implement their applications using our RE866 modules.

## 1.3. Contact Information, Support

For general contact, technical support services, technical questions and report documentation errors contact Telit Technical Support at:

- TS-EMEA@telit.com
- TS-AMERICAS@telit.com
- TS-APAC@telit.com
- TS-SRD@telit.com

Alternatively, use:

https://www.telit.com/contact-us/

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

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Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

## 1.4. Text Conventions


Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

## 1.5. Related Documents

- RE866 AT Command Reference, 80555ST10865A

# 2. OVERVIEW

The aim of this document is the description of some hardware solutions useful for developing a product with the Telit RE866 module. In this document, all the basic functions of a mobile phone will be taken into account; for each one of them a proper hardware solution will be suggested and eventually the wrong solutions and common errors to be avoided will be evidenced. Obviously, this document cannot embrace the whole hardware solutions and products that may be designed. The wrong solutions to be avoided shall be considered as mandatory, while the suggested hardware configurations shall not be considered mandatory, instead the information given shall be used as a guide and a starting point for properly developing your product with the Telit RE866 module. For further hardware details that may not be explained in this document refer to the Telit RE866 Product Description document where all the hardware information is reported.

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NOTE:

(EN) The integration of the RE866 module within user application shall be done according to the design rules described in this manual.

(IT) L'integrazione del modulo RE866 all'interno dell'applicazione dell'utente dovrà rispettare le indicazioni progettuali descritte in questo manuale.

(DE) Die Integration des RE866 Mobilfunk-Moduls in ein Gerät muss gemäß der in diesem Dokument beschriebenen Konstruktionsregeln erfolgen.

(SL) Integracija RE866 modula v uporabniški aplikaciji bo morala upoštevati projektna navodila, opisana v tem priročniku.

(SP) La utilización del modulo RE866 debe ser conforme a los usos para los cuales ha sido deseñado descritos en este manual del usuario.

(FR) L'intégration du module cellulaire RE866 dans l'application de l'utilisateur sera faite selon les règles de conception décrites dans ce manuel.

(HE) האינטגרטור מתבקש ליישם את ההנחיות המפורטות במסמך זה בתהליך האינטגרציה של המודם הסלולרי RE866 עם המוצר.

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# 3. PINS ALLOCATION

## 3.1. General Pin-out

| Pin | Signal | I/O | Function | Type | Comment |
|---|---|---|---|---|---|
| Asynchronous Serial Port and Two Wire Interface | | | | | |
| A4 | UART-TXD | I | Serial data input from DTE | | |
| A5 | UART-RXD | O | Serial data output to DTE | | |
| A1 | UART-RTS# | I | Input for Request to send signal (RTS) from DTE | | |
| B1 | UART-CTS# | O | Output for Clear to Send signal (CTS) to DTE | | |
| C1 | TWI-SDA | I/O | TWI Data | | |
| C2 | TWI-SCL | I/O | TWI Clock | | |
| Miscellaneous Functions | | | | | |
| C4 | SWDIO | I/O | Serial wire debug input/output | | |
| B4 | SWCLK | I | Serial wire debug input | | |
| G4 | RESET# | I-PU | Reset input for the device | Active low | |
| D5 | NFCANT1 | - | NFC antenna connection | | |
| B5 | NFCANT2 | - | NFC antenna connection | | |
| G2 | LORA_ANT | - | RF Sub-GHz antenna connection | RF | |

| | | | | | |
|---|---|---|---|---|---|
| D6 | TESTMODE# | I | Force test mode at startup | Active low | See sec. 3.5 |
| C6 | BOOT0 | I | Force test mode at start up | | See sec. 3.5 |
| Power Supply | | | | | |
| E1 | VSUP1 | - | Main Power supply | Power | |
| E2 | VSUP2 | - | Main Power supply | Power | |
| C3 | GND | - | Ground | Power | |
| D1 | GND | - | Ground | Power | |
| D2 | GND | - | Ground | Power | |
| E3 | GND | - | Ground | Power | |
| F1 | GND | - | Ground | Power | |
| F2 | GND | - | Ground | Power | |
| F3 | GND | - | Ground | Power | |
| F6 | GND | - | Ground | Power | |
| G1 | GND | - | Ground | Power | |
| G3 | GND | - | Ground | Power | |
| General and reserved | | | | | |
| A2 | GPIO | I/O | General I/O | | |
| A3 | GPIO | I/O | General I/O | | |
| B2 | GPIO | I/O | General I/O | | |

| | | | |
|---|---|---|---|
| F4 | GPIO | I/O | General I/O |
| A6 | RESERVED | | RESERVED |
| A7 | RESERVED | | RESERVED |
| B3 | RESERVED | | RESERVED |
| B6 | RESERVED | | RESERVED |
| B7 | RESERVED | | RESERVED |
| C5 | RESERVED | | RESERVED |
| C7 | RESERVED | | RESERVED |
| D3 | RESERVED | | RESERVED |
| D4 | RESERVED | | RESERVED |
| D7 | RESERVED | | RESERVED |
| E4 | RESERVED | | RESERVED |
| E5 | RESERVED | | RESERVED |
| E6 | RESERVED | | RESERVED |
| E7 | RESERVED | | RESERVED |
| F5 | RESERVED | | RESERVED |
| F7 | RESERVED | | RESERVED |
| G5 | RESERVED | | RESERVED |
| G6 | RESERVED | | RESERVED |
| G7 | RESERVED | | RESERVED |

Warning – Reserved pins must not be connected.

## 3.2. Specific Pin-out for LoRa+Bluetooth version

Some pins are alternatively named and defined depending on firmware version. These pins are annotated in the following table.

| Pin | Signal | Direction | | |
|---|---|---|---|---|
| | Modes: | **Normal** | **UICP** | **System-off** |
| A1 | UART-RTS# | I-PD | I-PD | I-PD |
| A2 | IUR-IN# | DIS | I | DIS |
| A3 | IUR-OUT# | DIS | O | DIS |
| A4 | UART-TXD | I | I | I |
| A5 | UART-RXD | O-PP | O-PP | O-PP |
| B1 | UART-CTS# | O-PP | O-PP | O-PP |
| B2 | Reserved | DIS | DIS | DIS |
| C1 | TWI-SDA | DIS | DIS | DIS |
| C2 | TWI-SCL | DIS | DIS | DIS |
| C6 | BOOT0 | I-PD | DIS | DIS |
| D6 | TESTMODE# | I-PU | DIS | DIS |
| F4 | Reserved | Reserved | Reserved | Reserved |
| G4 | RESET# | I | I | I |

**Note: For all other pins, which are not listed in section 3.2, see general pin-out (Sec. 3.1)**

## 3.3. Specific Pin-out for LoRa+LUA version

Some pins are alternatively named and defined depending on firmware version. These pins are annotated in the following table.

| Pin | Signal | Direction |
|---|---|---|
| A1 | UART-RTS# | I |
| A2 | DIO4 / AIN3 | I/O |
| A3 | DIO3 / AIN2 | I/O |
| A4 | UART-TXD | I |
| A5 | UART-RXD | O |
| B1 | UART-CTS# | O |
| B2 | DIO1 | I/O |
| C1 | DIO6 / TWI-SDA | I/O |
| C2 | DIO5 / TWI-SCL | O |
| C6 | BOOT0 | I |
| D6 | TESTMODE# | I |
| F4 | DIO2 / AIN1 | I/O |
| G4 | RESET# | I |

**Note: For all other pins, which are not listed in section 3.3, see general pin-out (Sec. 3.1)**

Warning – Reserved pins must not be connected.

## 3.4. Handling of Unused Signals

Depending on the application, not all signals may be needed. The following list gives some hints how to handle unused signals.

| Pin/Signal | Handling |
|---|---|
| G4: RESET# | If no external Reset is needed: Leave open |
| C6: BOOT0 | Leave open (1) |
| A4: UART-TXD<br>A5: UART-RXD | If UART Bus is not used: On UART-TXD, add a pullup (e.g.100kΩ) to VSUP (1); leave UART-RXD open (1) |
| A1: UART-RTS#<br>B1: UART-CTS# | If neither flow control nor UICP is used: Leave open (1)(2) |
| D5: NFCANT1<br>B5: NFCANT2 | If no NFC antenna is connected: Leave open |
| D6: TESTMODE# | Leave open (1) |
| C4: SWDIO<br>B4: SWCLK | Leave open. Only needed for debug purposes |
| Unused GPIOs | Leave open |

Please note, to keep compatibility with future feature enhancements, unused signals shall not be connected directly to VSUP or GND. Leave open.

(1) Signals must be accessible during the homologation process, refer to 3.5 Test Mode.

(2) It is strongly recommended to use hardware flow control in both directions.
Not using flow control can cause a loss of data.

## 3.5. Test Mode

For homologation purposes, the ability of test mode operation like “RE866 Test mode” or “Direct two wire UART Test mode” (DTM) is mandatory. The Direct Test Mode (as defined by the Bluetooth SIG) and RE866 Test mode are part of the RE866. For EMC measurements, the use of the RE866 Test mode is recommended.

For enabling the different test modes, the RE866 provides two IO pins.

- The pin TESTMODE# is low active. Active means connect to GND.
- The pin BOOT0 is high active. Active means connect to VSUP.
- The other two combinations start the bootloader for firmware update of the programmed firmware. These two modes are not scope of this document.

The following table shows the possible combinations:

| Testmode# | Boot0 | Mode |
|---|---|---|
| Active | Inactive | Test mode |
| Active | Active | DTM |
| Inactive | Active | Bootloader |
| Inactive | Inactive | Firmware |

To enter and use RE866 Test mode or DTM, access to the following signals is required:

- BOOT0
- TESTMODE#
- UART-RXD
- UART-TXD
- UART-RTS#
- UART-CTS#
- GND

These pins shall be routed to some test pads on an outer layer but can be left open during normal operation when not used.

Please note the UART is required for operation of test modes. During the homologation process, UART-RXD, UART-TXD, UART-RTS# and UART-CTS# must be freely accessible.

## 3.6. LGA Pads General Layout

| | A | B | C | D | E | F | G |
|---|---|---|---|---|---|---|---|
| 1 | UART-RTS# | UART-CTS# | TWI-SDA | GND | VSUP1 | GND | GND |
| 2 | GPIO | GPIO | TWI-SCL | GND | VSUP2 | GND | LORA_ANT |
| 3 | GPIO | Reserved | GND | Reserved | GND | GND | GND |
| 4 | UART-TXD | SWCLK | SWDIO | Reserved | Reserved | GPIO | RESET# |
| 5 | UART-RXD | NFCANT2 | Reserved | NFCANT1 | Reserved | Reserved | Reserved |
| 6 | Reserved | Reserved | BOOT0 | TESTMODE# | Reserved | GND | Reserved |
| 7 | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |

**TOP VIEW**

# 4. ELECTRICAL CHARACTERISTICS

## 4.1. Power Supply Requirements

The external power supply must be connected to VBATT signals and must fulfil the following requirements:

| Power Supply | Value |
|---|---|
| Nominal Supply Voltage | 3.3V |
| Normal Operating Voltage Range | 2.1V ÷ 3.6V |

The Operating Voltage Range MUST never be exceeded; care must be taken when designing the application's power supply section to avoid having an excessive voltage drop.

If the voltage drop is exceeding the limits it could cause a Power Off of the module.

Please note that the operating voltage limits MUST never be exceed, including voltage overshoots and drops.

## 4.2. Environmental Requirements

| Temperature Range | Value |
|---|---|
| Storage Temperature Range | -40°C to +115°C |
| Normal Operating Voltage Range | -40°C to +85°C |

## 4.3. Power Consumption

The following values are typical power consumption values in different states of operation. RE866 configured as a peripheral device.

VSUP = 3,3V, $T_{amb}$ = 25°C, all GPIO lines left open

| Mode | Condition | Note | Current Consumption ($I_{Avg}$) Tx power: 0dBm (max) | Unit |
|---|---|---|---|---|
| System off | CPU off, Radio inactive, 32k clock off, SRAM Retention off | | 0,4 | µA |
| Reset | Device hold in Reset | | 2,3 | mA |
| UICP active *and* serial interface down | Standby, Advertising Off (Radio inactive) | | 10 | µA |
| | Standby, Advertising, 3 channels advertising interval: 1.28s | | 19 | µA |
| | Connected, connection interval: 1.28s | (1) | 17 | µA |
| UICP not active *or* serial interface up | Idle, Advertising Off (Radio inactive) | | 1,3 | mA |
| | Advertising, 3 channels advertising interval: 1.28s | | 1,3 | mA |
| | Connected, connection interval: 1.28s | (1) | 1,3 | mA |
| LoRa | Transmission Mode @ +14dBm | (2) | 62 | mA |
| | Receive Mode | | 19,5 | mA |

(1) Parameters are setup by the central device when connection is established
(2) Continuous TX with modulated signal

## 4.4. RF Performance

### 4.4.1. BLE RF Performance

| | |
|---|---|
| Receiver sensitivity at room and extreme temp | -96dBm (conducted mode) |
| Transmit power at room and extreme temp | +5dBm (conducted mode) |

### 4.4.2. LoRa® RF Performance

| | |
|---|---|
| LoRa® Receiver sensitivity | -136 dBm (SF12, BW 125Khz) |
| LoRa® Transmitter signal strength | +14 dBm conducted |
| LoRa® Frequency band | 863,000 MHz to 870,000 MHz |
| Supported Modulation schemes | FSK, LoRa® 125kHZ and 250kHz |
| Supported Spreading Factor Range | 7 to 12 |
| ETSI Duty Cycle Management | Yes |
| Raw Data Rates | 250bps to 50kbps |

The TX power table in the LoRaWAN regional parameters specification gives values in dBm EIRP, which includes the customer specific antenna gain. Antenna performance is customer design dependent. Therefore, the RE866-EU output power can only be given as conducted values in dBm.

| Programmed TXPOWER | Conducted Power RE866-EU | LoRaWAN Specification |
|---|---|---|
| 0 | +14 dBm | Max. EIRP |
| 1 | +12 dBm | Max. EIRP - 2 dB |
| 2 | + 10dBm | Max. EIRP – 4 dB |
| 3 | + 8 dBm | Max. EIRP – 6 dB |
| 4 | +6 dBm | Max. EIRP – 8 dB |
| 5 | +4 dBm | Max. EIRP – 10 dB |
| 6 | +2 dBm | Max. EIRP – 12 dB |
| 7 | 0 dBm | Max. EIRP – 14dB |

| | |
|---|---|
| TX Output Power variation vs. Tamb (-40°C - +85°C) | -2dB typ. |
| TX output Power variation vs. VSUPPLY (+2,1V to +3,6V) | -5dB to +1dB typ. |

The harmonized ETSI standard EN 300 220-2 “Short Range Devices operating in the frequency range 25 MHz to 1000 MHz” Annex B defines the allowed TX power per band in mW ERP, whereas the LoRaWAN regional parameters specification defines the TX power in EIRP. The difference is ERP = EIRP – 2,15dB. This should be considered when comparing numbers.

Customer should take care that the conducted TX power + customer specific antenna gain generates TX power levels below the limits given in the harmonized ETSI standard EN 300 220-2 “Short Range Devices operating in the frequency range 25 MHz to 1000 MHz” Annex B.

The RX sensitivity of the LoRa/FSK receiver is depending on the modulation bandwidth and the spreading factor setting as given in the following table.

| Programmed Data Rate | Modulation SF/BW | Phys. Bit Rate bit/s | RX Sensitivity /dBm |
|---|---|---|---|
| 0 | SF12 / 125 kHz | 250 | -136,0 |
| 1 | SF11 / 125 kHz | 440 | -133,5 |
| 2 | SF10 / 125 kHz | 980 | -131,0 |
| 3 | SF9 / 125 kHz | 1.760 | -128,5 |
| 4 | SF8 / 125 kHz | 3.125 | -125,5 |
| 5 | SF7 / 125 kHz | 5.470 | -122,5 |
| 6 | SF7 / 250 kHz | 11.000 | -119,0 |
| 7 | FSK 50kbps | 50.000 | tbd |

### 4.4.3. NFC RF Performance

| | |
|---|---|
| Input Frequency | 13,56 MHz |
| Bit Rate | 106 kbps |
| TX via passive load modulation | |
| Input resistance when load modulating | 8 Ω to 22 Ω |
| Wake-on-field detection | |

## 4.5. Module placement recommendation

In this chapter recommendation about the module placement will be indicate in order to have the better performance for the BLE integrated antenna that in any case it is only for maintenance purpose.

### 4.5.1. BLE Antenna Gain and Radiation Pattern

TBD: To be defined

### 4.5.2. NFCT Antenna Recommendations

The NFCT antenna coil must be connected differential between NFC1 and NFC2 pins of RE866Two external capacitors Ctune1/2 connected between the NFCx pins and GND should be used to tune the resonance of the antenna circuit to 13.56 MHz.

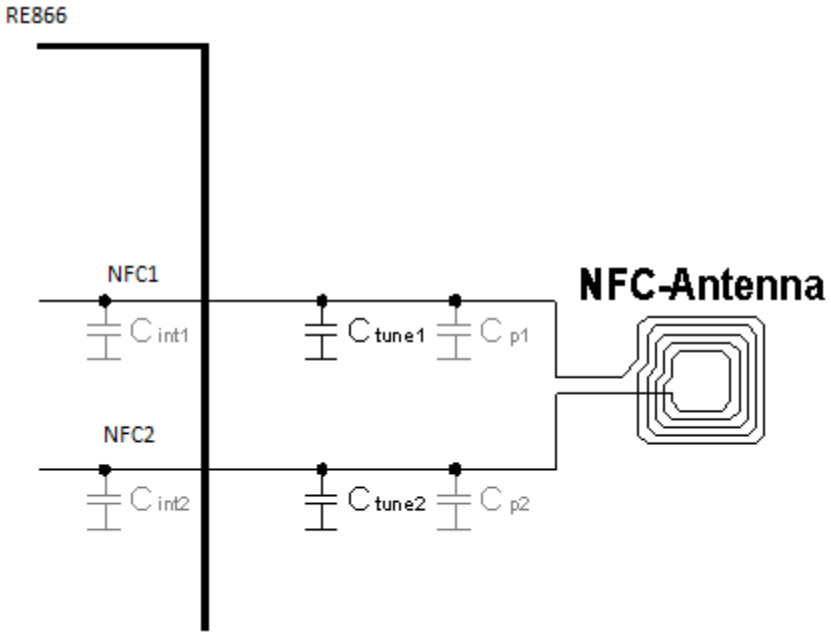



*Figure 1: RE866 NFC Antenna Tuning*

$$C_{tune} = \frac{2}{(2\pi \times 13{,}56MHz)^2 \times L_{ant}} - C_p - C_{int}$$

$$C_{tune} = C_{tune1} = C_{tune2}$$

$$C_p = C_{p1} = C_{p2}\ (antenna\ track\ capacitance)$$

$$C_{int} = C_{int1} = C_{int2} = 4pF$$

## 4.6. General Design Rules

The principal guidelines for the Power Supply Design embrace three different design steps:

- The electrical design
- The thermal design
- Thermal PCB layout

### 4.6.1. Electrical Design Guidelines

The electrical design of the power supply depends strongly on the power source from which this power is drained. We will distinguish them into three categories:

- +5V input (typically PC internal regulator output)
- +12V input (typically automotive)
- Battery

#### 4.6.1.1. +5V Source Power Supply Design Guidelines

- Because of the small difference between the input and output voltage, a switching converter is not the best choice, therefore a low-dropout regulator is required.
- When using a linear regulator, a proper heat sink must be provided in order to dissipate the power generated.
- A low-ESR, bypass capacitor of adequate capacity must be provided in order to cut the current absorption peaks close to the RE866, a 100µF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- A protection diode should be inserted close to the power input, in order to save the RE866 from power polarity inversion.

#### 4.6.1.2. +12V Source Power Supply Design Guidelines

- In this case, better efficiency of switching regulators can be exploited to generate the required VBat
- Switching frequencies of 500kHz or above are preferable, because of the smaller inductor size and the faster transient response.
- For car Pb battery, the input voltage can rise up to 15.8V and this should be kept in mind when choosing components: all components in the power supply must withstand this voltage. A spike protection diode has to be inserted close to the power input.
- A low-ESR, bypass capacitor of adequate capacity must be provided in order to cut current absorption peaks. 100µF, 10V is usually enough.
- A protection diode should be inserted close to the power input, to avoid damage to the RE866 from polarity inversion. This can be the same diode used for spike protection.

### 4.6.2. Power Supply PCB layout Guidelines

As seen on the electrical design guidelines, the power supply shall have a low-ESR capacitor on its output, to cut the current peaks, and a protection diode on its input, to protect the VBATT pins from polarity inversion. The placement of these components is crucial to ensure the correct working of the circuitry. A misplaced component can be useless, or even detrimental to the power supply performances.

- The low-ESR, bypass capacitor must be placed close to the RE866 VBATT pads, or close to the inductor if a switching regulator is used.

- The protection diode must be placed close to the input power connector.
- The PCB power traces must be wide enough to ensure negligible voltage drop even at the highest rated current consumption for the RE866.
- Use of a good, common ground plane is recommended.

# 5. DIGITAL SECTION

## 5.1. Logic Levels

The following table shows the logic level specifications use in RE866:

$T_{amb}$ = 25°C

| Symbol | Item | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{IL}$ | Low-Level Input Voltage | VSUP = 2.1 to 3.6V | - | VSUP *0.3 | V |
| $V_{IH}$ | High-Level Input Voltage | VSUP = 2.1 to 3.6V | VSUP*0.7 | VSUP | V |
| $V_{OL}$ | Low-Level Output Voltage | $I_{OL}$ = 0.5mA (1)<br>$I_{OL}$ = 5.0mA (2), (3) | - | 0.4<br>0.4 | V |
| $V_{OH}$ | High-Level Output Voltage | $I_{OH}$ = -0,5 mA (1)<br>$I_{OH}$ = -5,0 mA (2), (3) | VSUP -0.4<br>VSUP-0.4 | VSUP<br>VSUP | V |
| $I_{OL}$ | Low –Level Output Current | $V_{OL}$ ≤ 0,4V | - | -0.5(1)<br>5.0(2),(3) | mA |
| $I_{OH}$ | High-Level Output Current | VSUP-0,3V ≤ $V_{OH}$ ≤ VSUP | - | 0.5 (1)<br>5.0mA (2),(3) | mA |

(1) drive = std
(2) drive = high
(3) maximal number of pins (per package) with high drive is 3

## 5.2. RESET signal

Input RESET has a Schmitt-Trigger characteristic and an internal pull-up resistor.

$T_{amb}$ = 25°C

| Symbol | Item | Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Low-Level Input Voltage | VSUP = 2.1 to 3.6V | - | 0.25* VSUP | - | V |
| $V_{IH}$ | High-Level Input Voltage | VSUP = 2.1 to 3.6V | VSUP* 0.7 | - | VSUP | V |
| $R_{pu}$ | Pull-up Resistor | | 11 | 13 | 16 | kΩ |
| $C_i$ | Input Capacitance | | | 3 | | pF |

## 5.3. Communication ports

### 5.3.1. UART

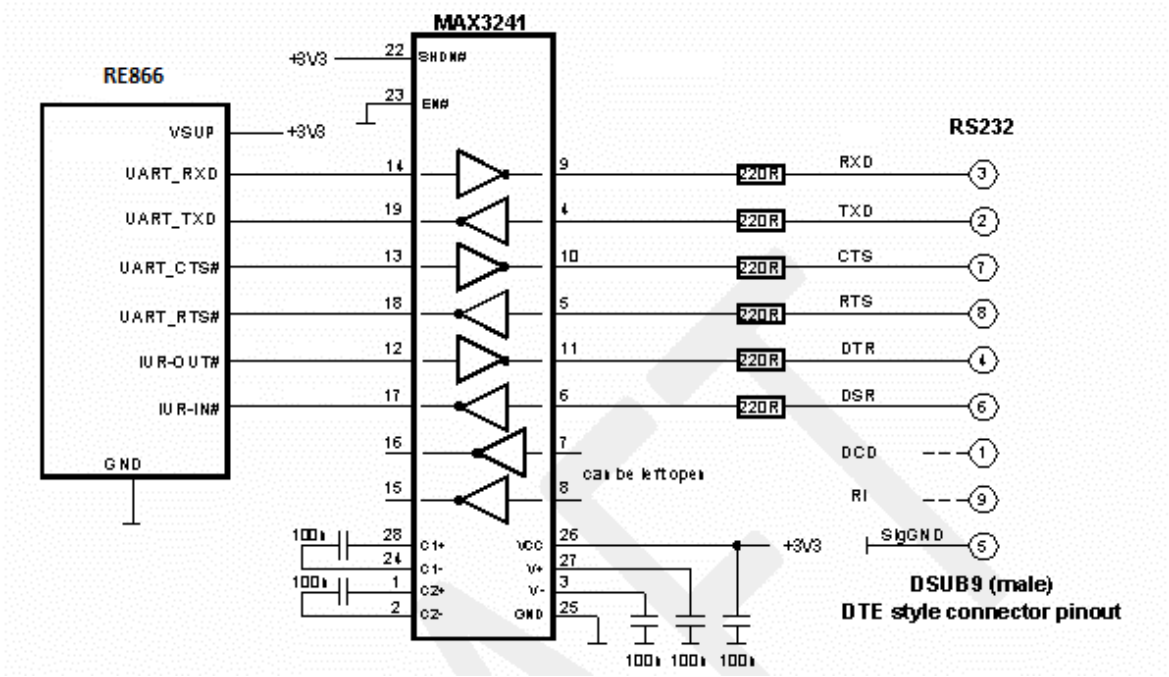
The factory default parameters for the UART operation can be found in chapter 0.

In the table below are listed the possible UART configurations of RE866.

| Property | RE866 Configuration |
|---|---|
| Baud rate | 1200 up to 1000000 bps (1Mbps), no auto-baud rate detection |
| Data bits | 8 bits |
| Flow control | UART-CTS# / UART-RTS# |
| Parity | None |
| Stop bits | 1 |

| PAD | Signal | I/O | Function |
|---|---|---|---|
| A1 | UART-RTS# | I-PD | Input for Request to send signal (RTS) from DTE |
| B1 | UART-CTS# | O-PP | Output for Clear to send signal (CTS) to DTE |
| A4 | UART-TXD | I | Serial data input (TXD) from DTE |
| A5 | UART-RXD | O-PP | Serial data output (RXD) to DTE |
| A2 | IUR_IN# | I-DIS | UICP control signal |
| A3 | IUR_OUT# | O-DIS | UICP control signal |

### 5.3.2. UART Example Circuits




RE866 Example Serial Interface (RS-232) Supporting UICP

# 6. RF SECTION

## 6.1. Antenna requirements

Special care must be taken during the design of the RF section on the application board.

RF performance degradation, and infringements of emission limits, may arise if the following recommendations are not respected.

A 50Ω antenna is required. Telit's RE866 interface features an SMA connector for an external antenna, but other choices are possible, such as a chip or a printed one. In case an integrated or printed antenna is used, it is recommended to place it on the edge of the application board.

Since it may be necessary to tune the antenna impedance to 50Ω, it is recommended to foresee a PI matching network between the RE866 and the antenna, at least during first prototyping: if not required, a series 0Ω-resistor can be used, leaving the two shunt components unpopulated.

### 6.1.1. ESD protection

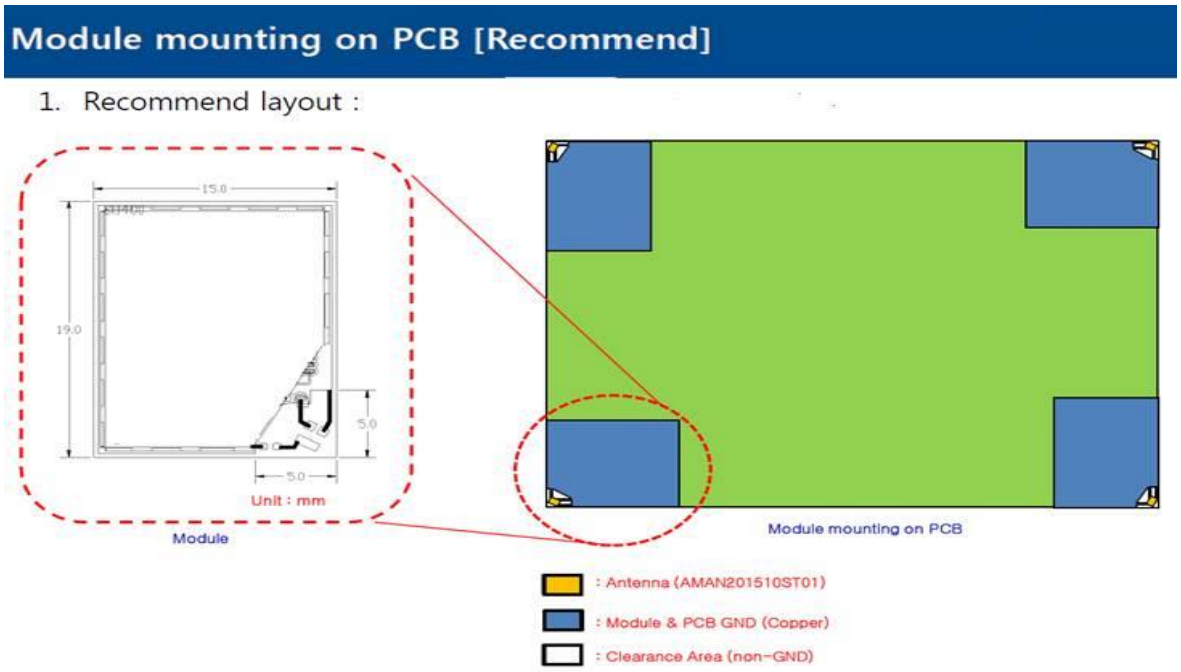
It is highly recommended to use a ESD protection between external antenna and Telit´s RE866 antenna interface. RF ESD protection diodes with low capacitance for 800-1000 MHz band and IEC61000-4-x compliance can be used. Furthermore, the protection diode must have low insertion loss. The protection diode should be placed very close to external antenna.

The selection of the ESD Protection should be done considering the deployment environment. As an example, please consider the following table:

| ESD-Protector | Typ. C (pF) | Characteristics |
|---|---|---|
| Infineon ESD112-B1-02 | 0.2 | IEC61000-4-2: ±20 kV (Air/Contact)<br>IEC61000-4-4: ±40 A (5/50 ns)<br>IEC61000-4-5: ±3 A (8/20 µs) |
| ST ESDAXLC6-1BU2K | 0.2 | IEC 61000-4-2: ±8 kV (Contact)<br>IEC 61000-4-2: ±15 kV (Air)<br>Peak pulse current: 1A (8/20 µs) |

### 6.1.2. BT antenna positioning

On the figure below, best position of the BT antenna has been shown.




### 6.1.3. PCB Design guidelines

The RE866 module provides a 50Ω antenna pad, which has to be routed to the antenna connector (or the integrated antenna) by means of a transmission line.

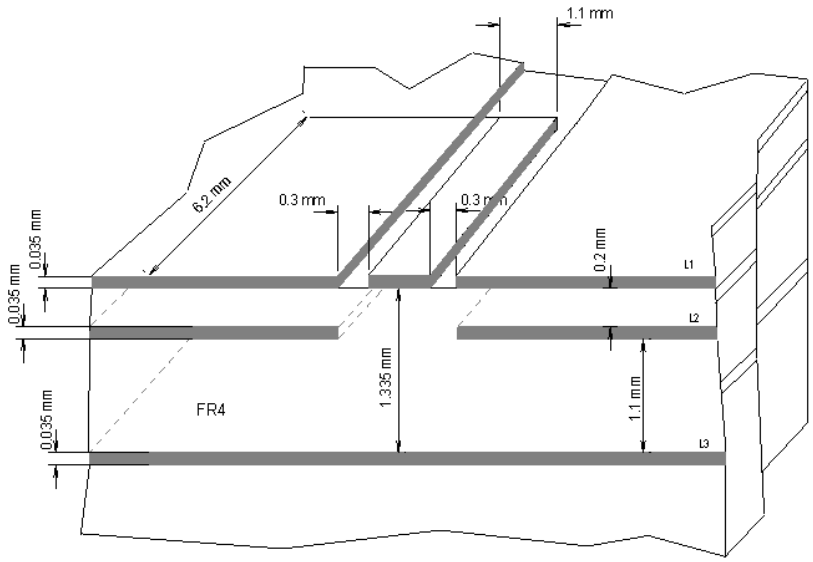
It is vital that the impedance of this line is controlled to 50Ω. The line should be as short as possible, and keep a constant cross section, without abrupt curves. It shall be isolated from any other noise source: in particular, trace shall not be crossed by other lines in adjacent layers. Instead, a continuous ground plane is recommended under the antenna trace, and a ground via curtain should connect it to the coplanar ground planes.

As an example of a possible implementation, the details of the antenna trace on the RE866 interface board are described in this section.

A Grounded Coplanar Waveguide (G-CPW) line has been chosen, since this kind of transmission line ensures good impedance control and can be implemented in an outer PCB layer as needed in this case. A SMA female connector has been used to feed the line.

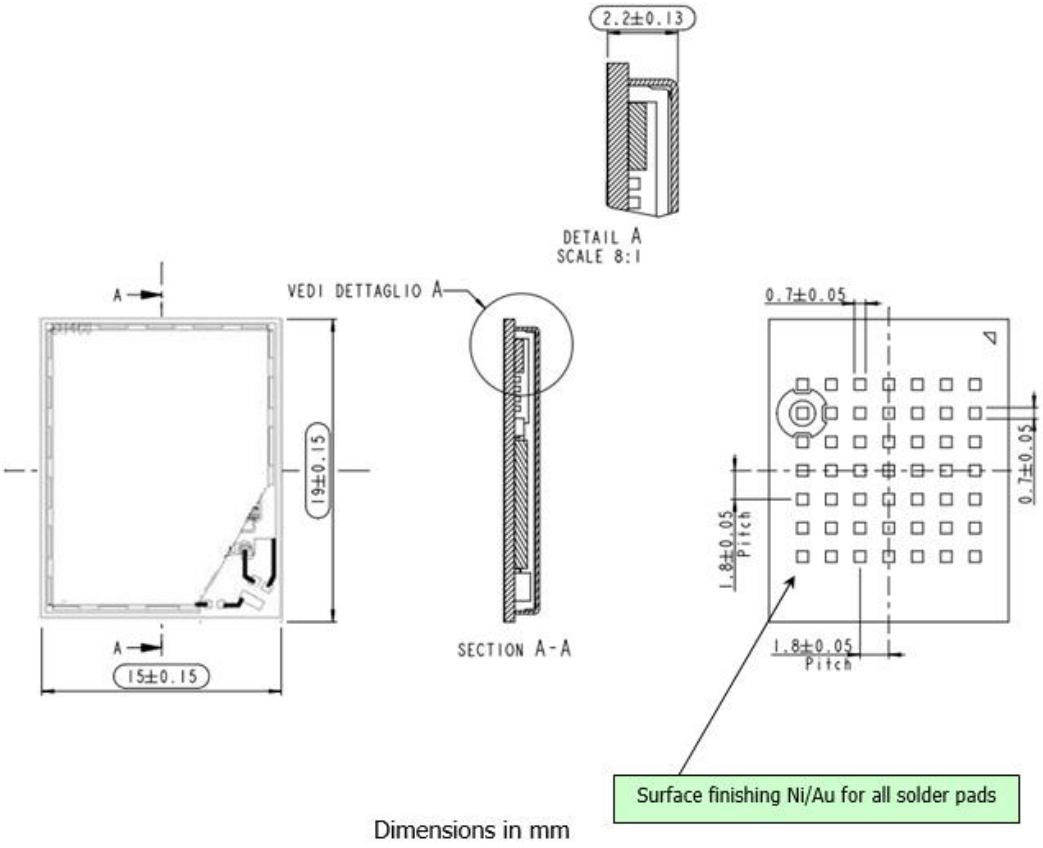
The interface board is realized on a FR4, 4-layers PCB. Substrate material is characterized by relative permittivity εr = 4.6 ± 0.4 @ 1 GHz, TanD= 0.019 ÷ 0.026 @ 1 GHz.

A characteristic impedance of nearly 50 Ω is achieved using trace width of 1.1 mm, clearance from coplanar ground plane = 0.3 mm each side. The line uses reference ground plane on layer 3, while copper is removed from layer 2 underneath the line. Height of trace above ground plane is 1.335 mm. Calculated characteristic impedance is 51.6 Ω, estimated line loss is less than 0.1 dB. The line geometry is shown below:


1.1 mm
6.2 mm
0.3 mm
0.3 mm
0.035 mm
0.035 mm
0.2 mm
L1
L2
1.335 mm
1.1 mm
FR4
0.035 mm
L3

# 7. MECHANICAL DESIGN

## 7.1. Drawing

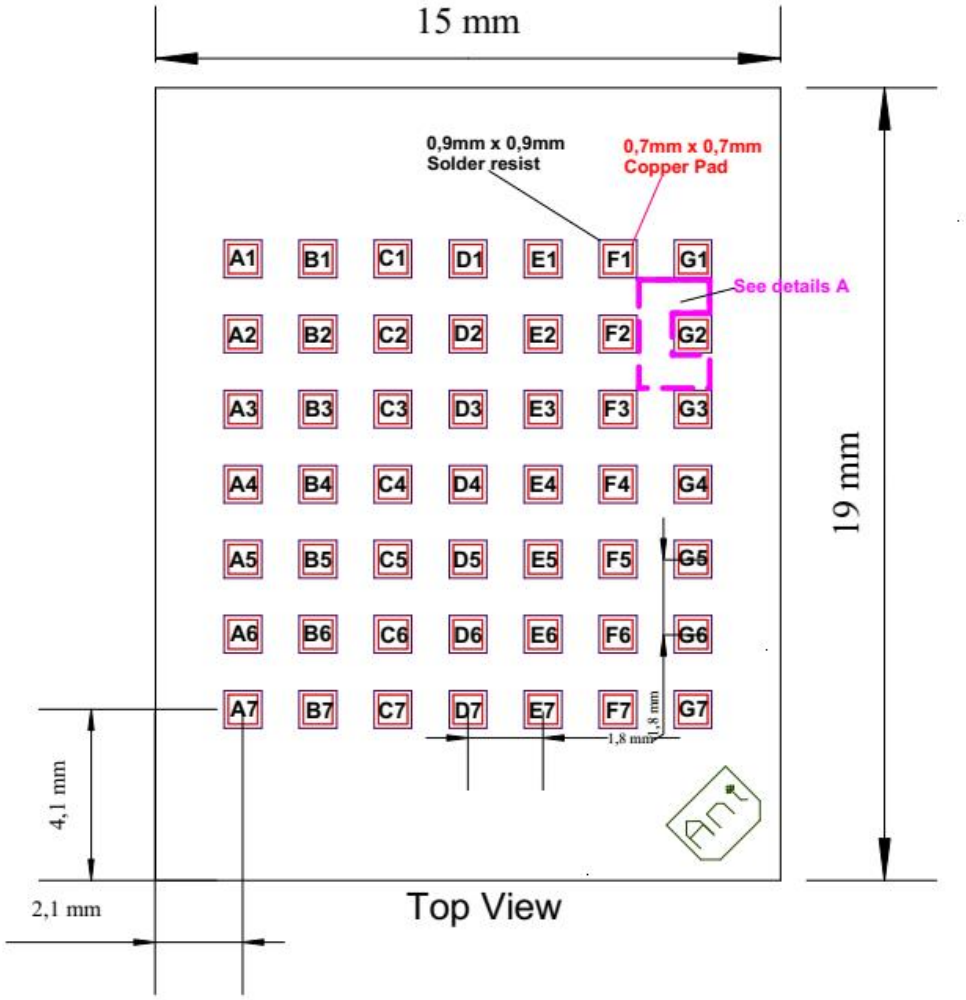


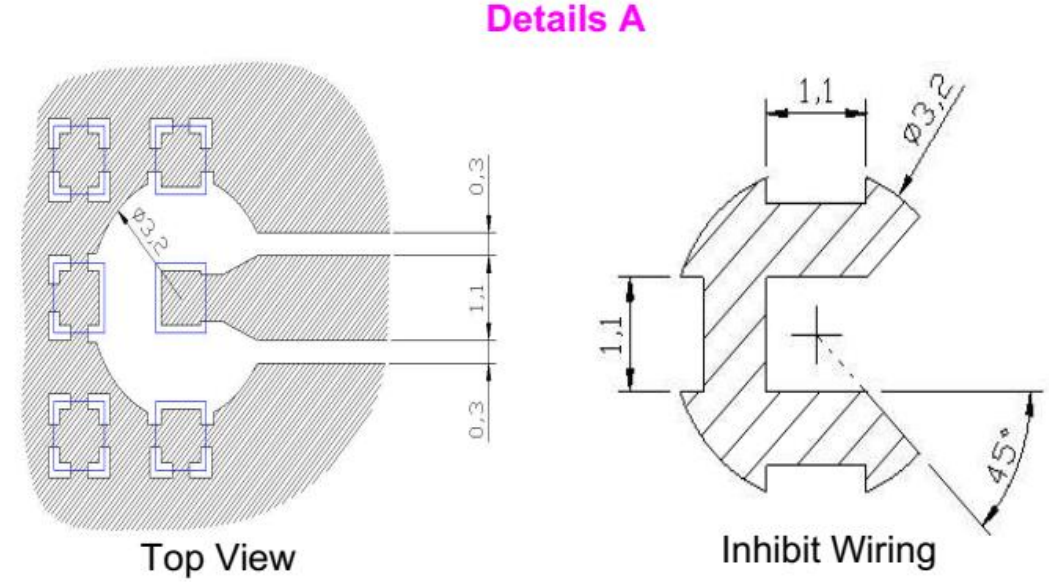

Dimensions in mm

# 8. APPLICATION PCB DESIGN

## 8.1. Footprint

Recommended footprint for the application:



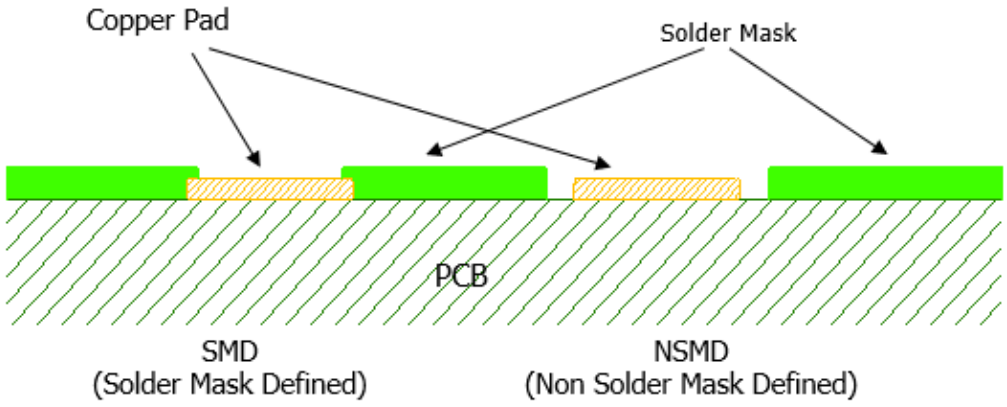
In order to easily rework the RE866 is suggested to consider on the application a 1.5 mm placement inhibit area around the module.

It is also suggested, as common rule for an SMT component, to avoid having a mechanical parts of the application in direct contact with the module.

Tip or Information – In the customer application, the region under WIRING INHIBIT (see figure above) must be clear from signal or ground paths.

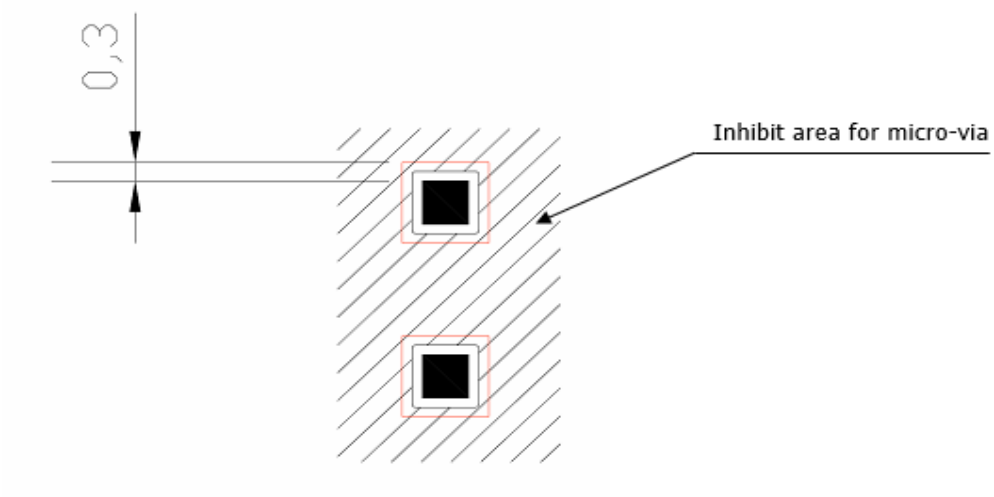
## 8.2. PCB pad design

Non solder mask defined (NSMD) type is recommended for the solder pads on the PCB.



## 8.3. PCB pad dimensions

It is not recommended to place via or micro-via not covered by solder resist in an area of 0.3 mm around the pads unless it carries the same signal of the pad itself (see following figure).




Holes in pad are allowed only for blind holes and not for through holes.

Recommendations for PCB pad surfaces:

| Finish | Layer thickness [µm] | Properties |
|---|---|---|
| Electro-less Ni / Immersion Au | 3 –7 / 0.03 – 0.15 | Good solderability protection, high shear force values |

The PCB must be able to resist the higher temperatures which are occurring at the lead-free process. This issue should be discussed with the PCB-supplier. Generally, the wettability of tin-lead solder paste on the described surface plating is better compared to lead-free solder paste.

It is not necessary to panel the application PCB, however in that case it is suggested to use milled contours and predrilled board breakouts; scoring or v-cut solutions are not recommended.

## 8.4. Stencil

Stencil's apertures layout can be the same of the recommended footprint (1:1), we suggest a thickness of stencil foil ≥ 120 µm.

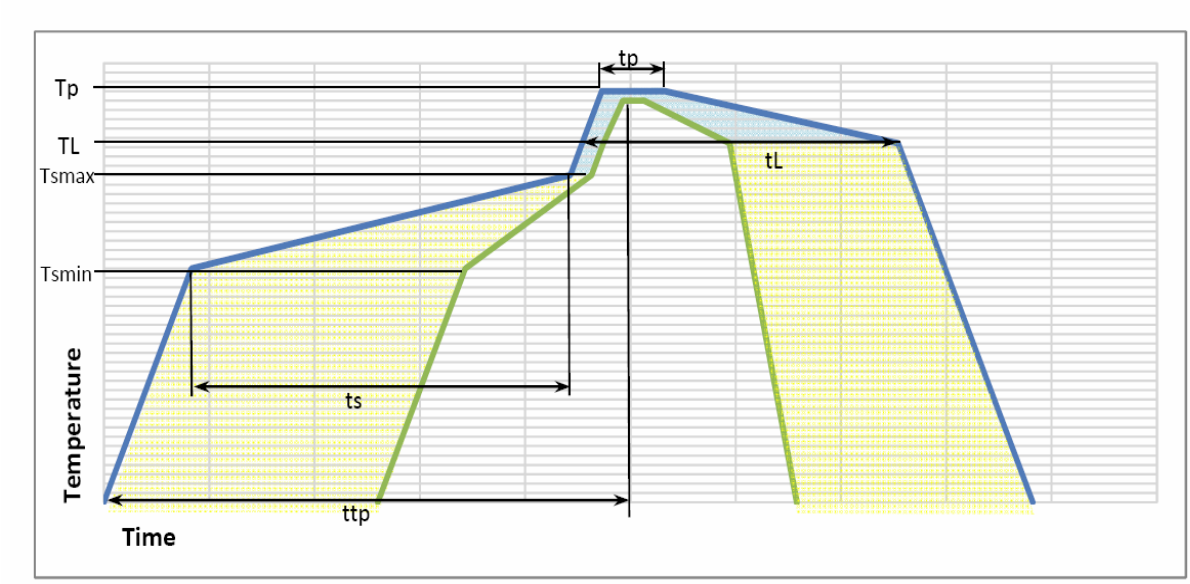
## 8.5. Solder paste

| | Lead free |
|---|---|
| Solder paste | Sn/Ag/Cu |

We recommend using only “no clean” solder paste in order to avoid the cleaning of the modules after assembly.

## 8.6. Solder Reflow

Recommended solder reflow profile



| Profile Feature | Pb-Free Assembly |
|---|---|
| Average ramp-up rate (TL to TP) | 3°C/second max |
| Preheat<br>– Temperature Min (Tsmin)<br>– Temperature Max (Tsmax)<br>– Time (min to max) (ts) | <br>150°C<br>200°C<br>60-180 seconds |
| Tsmax to TL<br>– Ramp-up Rate | <br>3°C/second max |
| Time maintained above:<br>– Temperature (TL)<br>– Time (tL) | <br>217°C<br>60-150 seconds |
| Peak Temperature (Tp) | 245 +0/-5°C |
| Time within 5°C of actual Peak Temperature (tp) | 10-30 seconds |
| Ramp-down Rate | 6°C/second max. |
| Time 25°C to Peak Temperature | 8 minutes max. |

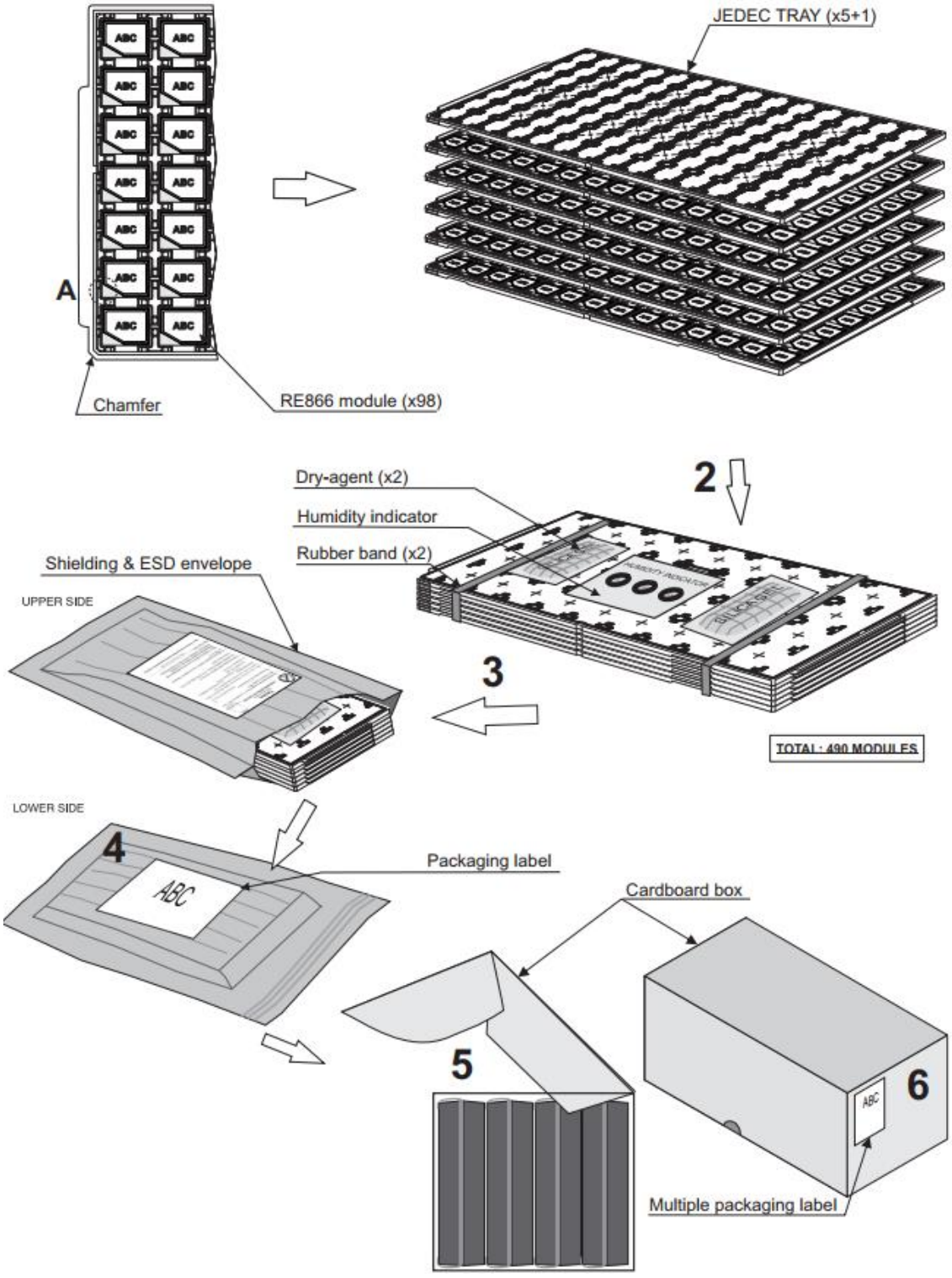
Tip or Information – All temperatures refer to topside of the package, measured on the package body surface.

Caution or Warning – RE866 module withstands one reflow process only.

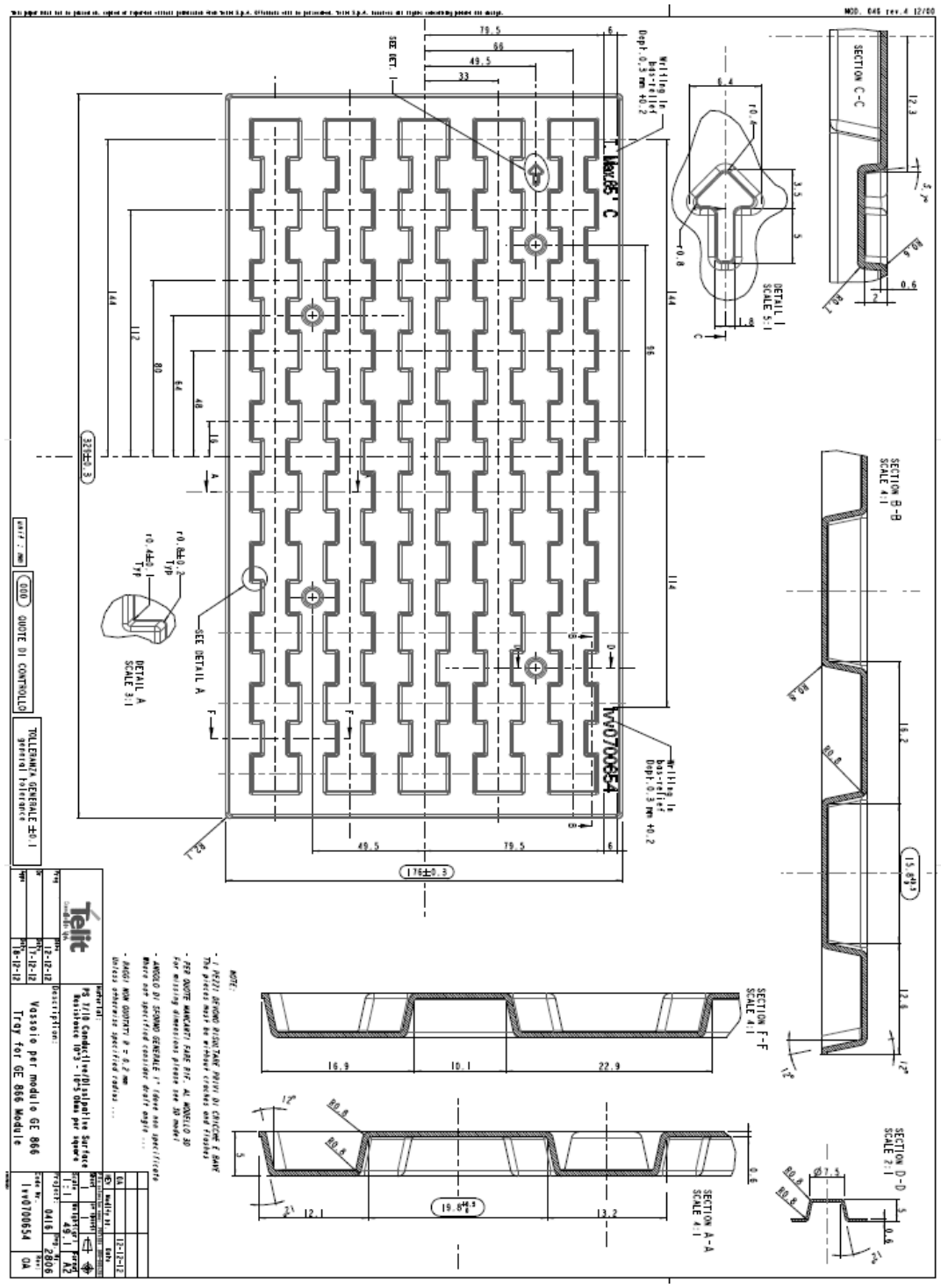
# 9. PACKAGING

## 9.1. Tray

The RE866 modules are packaged on trays when small quantities are required (i.e. for test and evaluation purposes). Trays are not designed to be used in SMT processes for pick and place handling.



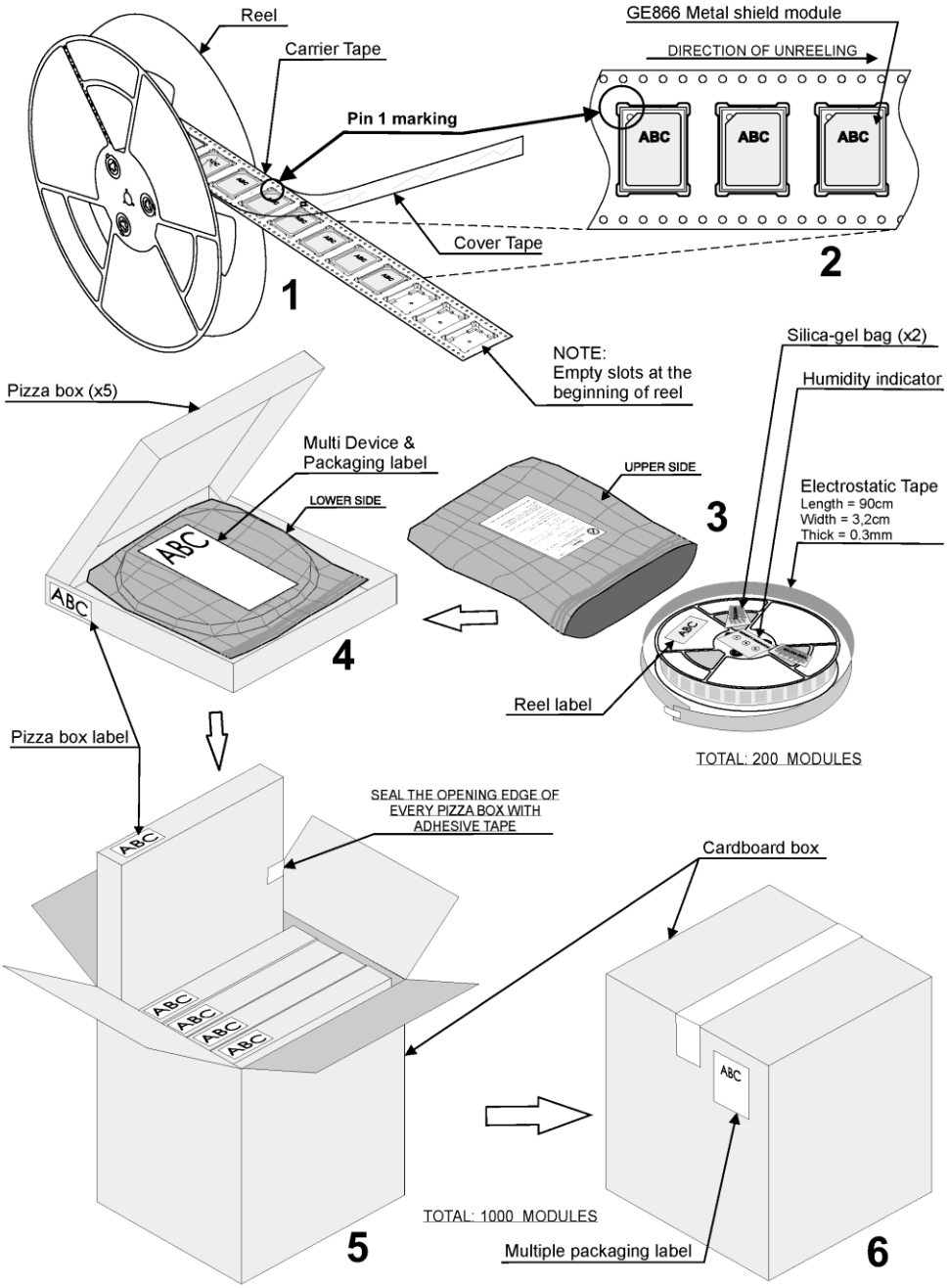
### 9.1.1. Tray mechanical drawing




Caution or Warning –These trays can withstand at the maximum temperature of 65°C.

## 9.2. Reel

The RE866 modules are packaged on reels of 200 pieces each, see picture below.



## 9.3. Moisture sensitivity

The moisture sensitivity level of the Product is “3” according with standard IPC/JEDEC J-STD-020, take care of all the relative requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

a) The shelf life of the Product inside of the dry bag is 12 months from the bag seal date, when stored in a non-condensing atmospheric environment of < 40°C and < 90% RH.
b) Environmental condition during the production: <= 30°C / 60% RH according to IPC/JEDEC J-STD-033B.
c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition b) “IPC/JEDEC J-STD-033B paragraph 5.2” is respected.
d) Baking is required if conditions b) or c) are not respected.
e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more.

# 10. COMPLIANCES

The RE866-EU has been tested to comply with the appropriate EU directives.

CE testing is intended for end products only. Therefore, CE testing is not mandatory for a Bluetooth module sold to OEM's. However, Telit provides CE tested modules for customers in order to ease CE compliance assessment of end products and to minimize test effort.

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All certifications and declarations, except RoHS and ReacH, are only valid for the RE866-EU running with Telit FW. If the FLASH is erased and a customer specific FW is loaded all certifications have to be re-evaluated or renewed.

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## 10.1. Declaration of Conformity CE

The RE866-EU fully complies with the essential requirements of the following EU directives:

- RED 2014/53/EU
- RoHS 2011/65/EC

The actual version of EU Declaration of Conformity (EU DoC) can be downloaded from

https://www.telit.com/RED

## 10.2. BTSIG BT Listing

The RE866-EU is a qualified design according to the Bluetooth Qualification Program Specification 4.2.

The Declaration ID is:

**D036715**

The Qualified Design ID is:

**111328**

For further information about marking requirements of your product attention should be paid the Bluetooth Brand Usage Guide at

https://www.bluetooth.org/en-us/bluetooth-brand/bluetooth-brand

According to the Bluetooth SIG rules (Bluetooth Declaration Process Document – DPD) you must complete a Product Listing and Declaration of Compliance (DoC) referencing the Qualified Design (QDID) for your product. For further information see www.Bluetooth.org or contact Telit.

# 11. SAFETY RECOMMENDATIONS

## 11.1. READ CAREFULLY

Be sure the use of this product is allowed in the country and in the environment required. The use of this product may be dangerous and has to be avoided in the following areas:

- Where it can interfere with other electronic devices in environments such as hospitals, airports, aircrafts, etc.
- Where there is risk of explosion such as gasoline stations, oil refineries, etc. It is the responsibility of the user to enforce the country regulation and the specific environment regulation.

Do not disassemble the product; any mark of tampering will compromise the warranty validity. We recommend following the instructions of the hardware user guides for correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to be conformed to the security and fire prevention regulations. The product has to be handled with care, avoiding any contact with the pins because electrostatic discharges may damage the product itself. Same cautions have to be taken for the SIM, checking carefully the instruction for its use. Do not insert or remove the SIM when the product is in power saving mode.

The system integrator is responsible for the functioning of the final product; therefore, care has to be taken to the external components of the module, as well as any project or installation issue, because the risk of disturbing the GSM network or external devices or having impact on the security. Should there be any doubt, please refer to the technical documentation and the regulations in force. Every module has to be equipped with a proper antenna with specific characteristics. The antenna has to be installed with care in order to avoid any interference with other electronic devices and has to guarantee a minimum distance from the body (20 cm). In case this requirement cannot be satisfied, the system integrator has to assess the final product against the SAR regulation.

The European Community provides some Directives for the electronic equipment introduced on the market. All of the relevant information is available on the European Community website.

# 12. ACRONYMS

| | |
|---|---|
| TTSC | Telit Technical Support Centre |
| USB | Universal Serial Bus |
| HS | High Speed |
| DTE | Data Terminal Equipment |
| UMTS | Universal Mobile Telecommunication System |
| WCDMA | Wideband Code Division Multiple Access |
| HSDPA | High Speed Downlink Packet Access |
| HSUPA | High Speed Uplink Packet Access |
| UART | Universal Asynchronous Receiver Transmitter |
| HSIC | High Speed Inter Chip |
| SIM | Subscriber Identification Module |
| SPI | Serial Peripheral Interface |
| ADC | Analog – Digital Converter |
| DAC | Digital – Analog Converter |
| I/O | Input Output |
| GPIO | General Purpose Input Output |
| CMOS | Complementary Metal – Oxide Semiconductor |
| MOSI | Master Output – Slave Input |
| MISO | Master Input – Slave Output |
| CLK | Clock |
| MRDY | Master Ready |

| | |
|---|---|
| SRDY | Slave Ready |
| CS | Chip Select |
| RTC | Real Time Clock |
| PCB | Printed Circuit Board |
| ESR | Equivalent Series Resistance |
| VSWR | Voltage Standing Wave Radio |
| VNA | Vector Network Analyzer |
| PU | Pull Up |
| PD | Pull Down |
| PP | Push pull |
| DIS | Disconnected |
| TWI | Two Wire Interface |
| UICP | UART Interface Control Protocol |
| DIO | Digital Input Output |
| AIN | Analog Input |
| DTM | Direct Test Mode |

# 13. DOCUMENT HISTORY

| Revision | Date | Changes |
|---|---|---|
| **4** | 2017-10-26 | First release |
| **5** | 2018-01-19 | Revised chapter 3 PINS ALLOCATION<br>Revised chapter 3.5 Test Mode<br>Revised chapter 0 power consumption values for LoRa<br>Revised chapter 5.1 logic levels<br>Revised chapter 5.2 RESET signal<br>Added chapter 6.1.1 ESD protection<br>Revised chapter 9.1 tray drawing |
| **6** | 2018-04-20 | Revised chapter 4.4 RF Performance<br>Revised chapter 10 COMPLIANCES<br>Revised chapter 8.1 Footprint<br>Revised chapter 3.5 Test Mode |
| **7** | 2018-08-23 | Revised chapter 4.4.2 LoRa® RF Performance<br>Revised chapter 4.3 Power Consumption<br>Revised chapter 10 COMPLIANCES |

# SUPPORT INQUIRIES

Link to **www.telit.com** and contact our technical support team for any questions related to technical issues.

## www.telit.com


Telit Communications S.p.A.
Via Stazione di Prosecco, 5/B
I-34010 Sgonico (Trieste), Italy

Telit IoT Platforms LLC
5300 Broken Sound Blvd, Suite 150
Boca Raton, FL 33487, USA

Telit Wireless Solutions Inc.
3131 RDU Center Drive, Suite 135
Morrisville, NC 27560, USA

Telit Wireless Solutions Co., Ltd.
8th Fl., Shinyoung Securities Bld.
6, Gukjegeumyung-ro8-gil, Yeongdeungpo-gu
Seoul, 150-884, Korea

Telit Wireless Solutions Ltd.
10 Habarzel St.
Tel Aviv 69710, Israel

Telit Wireless Solutions
Technologia e Servicos Ltda
Avenida Paulista, 1776, Room 10.C
01310-921 São Paulo, Brazil