xL865
Global Form Factor Application Note

80000NT11207A Rev. 2– 2018-12-04

TELIT
TECHNICAL
DOCUMENTATION

[01.2017]

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APPLICABILITY TABLE

PRODUCTS

- GL865-DUAL V3
- GL865-QUAD V3
- GL865-DUAL V3.1
- GL865-QUAD V3.1
- GL865-QUAD V4
- UL865-EUR
- UL865-EUD
- UL865-NAR
- UL865-NAD
- CL865-DUAL
- ML865C1

CONTENTS

1. INTRODUCTION

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1.1. Scope

Scope of this document is the description of some hardware solutions useful for developing an application compatible with the products of the xL865 family in order to highlight the minor differences between the above mentioned products.

1.2. Contact Information, Support

For general contact, technical support services, technical questions and report documentation errors contact Telit Technical Support at:

- TS-EMEA@telit.com
- TS-AMERICAS@telit.com
- TS-APAC@telit.com

Alternatively, use:

http://www.telit.com/support

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

http://www.telit.com

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

1.3. Text Conventions

Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

1.4. Related Documents

The following is a list of applicable documents downloadable from the Download Zone section of Telit's website http://www.telit.com

- UL865 Hardware User Guide 1VV0301050
- GL865 V3/V3.1 Hardware User Guide 1VV0301018
- CL865-DUAL Hardware User Guide 1VV0301104
- GL865-QUAD V4 HW User Guide 1VV0301518 rev.2
- ML865C1 Hardware User Guide 1VV0301493 rev.1 preliminary

2. OVERVIEW

In this document all the basic functions of a mobile phone will be taken into account; for each one of them a proper hardware solution will be suggested and eventually the wrong solutions and common errors to be avoided will be evidenced. Obviously, this document cannot embrace the whole hardware solutions and products that may be designed. The wrong solutions to be avoided shall be considered as mandatory, while the suggested hardware configurations shall not be considered mandatory, instead the information given shall be used as a guide and a starting point for properly developing your product with the described modules. For further hardware details that may not be explained in this document refer to the Telit Product Description documents where all the hardware information is reported.

The integration of the GL865 V3/UL865/CL865/ML865C1 and GL865 V4 cellular module within user application shall be done according to the design rules described in this manual.

The Unified Form Factor (UFF) is a concept of a products family characterized by the same mechanical and electrical form factor with different radio access technology.

This new approach protects customer's investment by giving you the possibility to migrate with the simple plug-and-play switch of your module with other wireless modules in the Unified Form Factor range without changing your application. In this way Telit offers easy access to different cellular technologies, certifications or bandwidth. For example if you develop applications based on today's mobile operator GSM/GPRS cellular technology if required it might be upgraded in the future to higher data speed capability such as UMTS/HSDPA.

The main advantages are summarized below:

- Increase of the efficiency in the use of the investments assigned to the development of the application (NRE), resulting in higher ROI, thus justifying the business choice of the UFF products;
- Products that are designed to bring technology enhancements to the integrators, such as higher data rates and new wireless standards while maintaining backwards compatibility in form factor and logical interfaces;
- Ease of integration;
- Telit as a single supplier of wireless modems;
- The customer can focus on its core business and application, not the management of operations and procurement required for wireless modems;
- One single application for different markets.

3. MECHANICAL DIMENSIONS

The Telit xE865 family overall dimensions are:

MODULE	LENGTH [MM]	WIDTH [MM]	THICKNESS [MM]
GL865 V3	24.4	24.4	2.6
GL865 V3.1	24.4	24.4	2.6
GL865 V4	24.4	24.4	2.6
UL865	24.4	24.4	2.6
CL865	24.4	24.4	2.45
ML865C1	24.4	24.4	2.6

In a common design application, which is going to use multiple models, we recommend to consider the highest dimensions as reference.

Note:

The 3D drawings/models versions are available separately, and they are provided in IGES format. Please contact the Telit Technical Support to get the models.

4. MODULE COMMON PINOUT

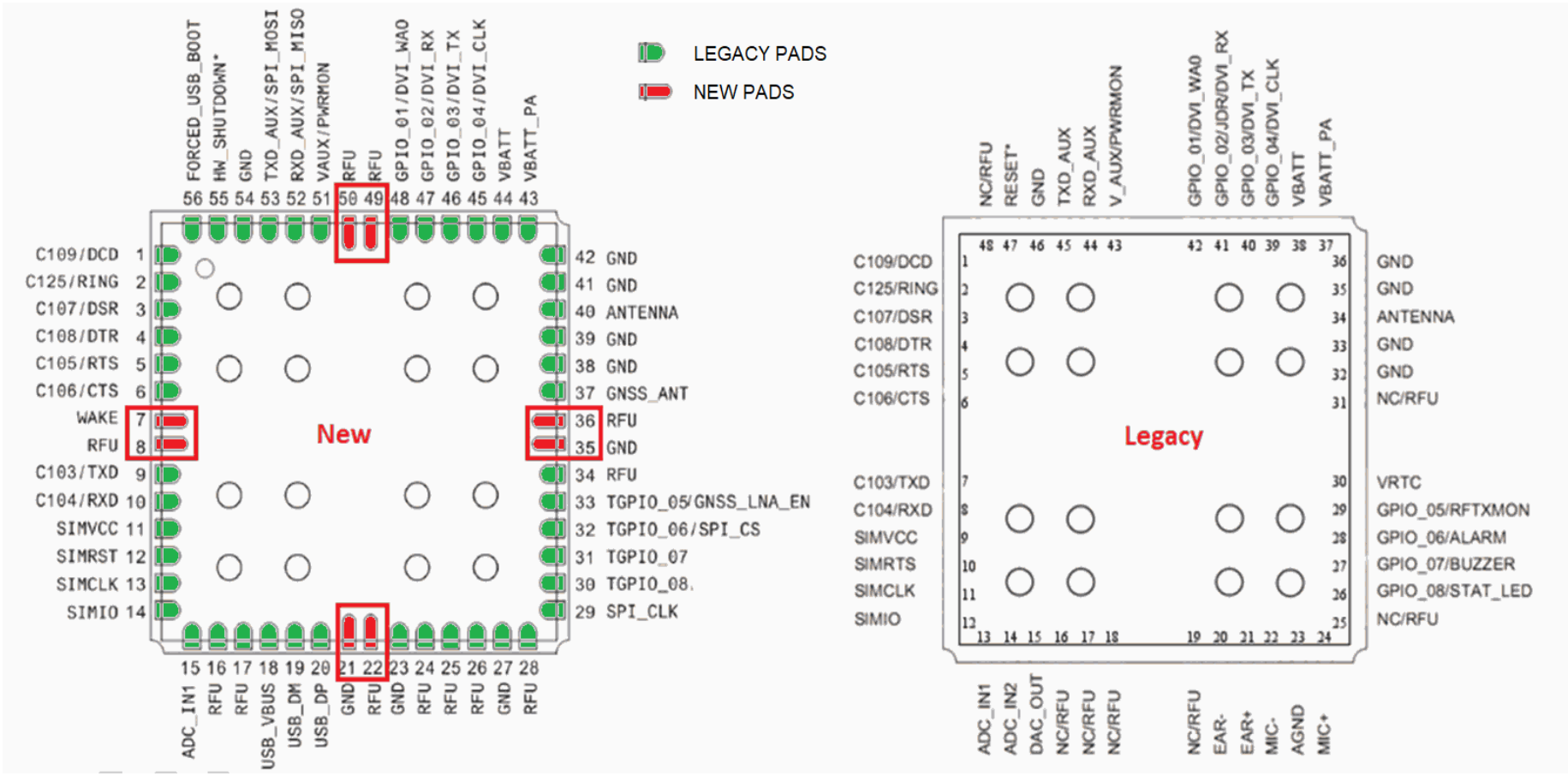
The new GL865-QUAD V4 and ML865C1 have 8 additional pads with respect to the other “legacy” products in the xL865 family, as a consequence the pin numbering changed.

Due to the fact that the pin numbering has changed, please refer to the physical pads and not only to the numbering.

“L” refer to = GL865-QUADV3,UL865,CL865 legacy products

“N” refer to =GL865-QUAD V4,ML865C1.

Red rectangular indicates the pin added for the ML865C1 and GL865-V4 FF.



Pin "L"	Pin "N"	Signal	I/O	Function	Type	Comment
				Power Supply		
38	**44**	VBATT	-	Main power supply (Baseband)	Power	
37	**43**	VBATT_PA	-	Main power supply (Radio PA)	Power	
23	**27**	AGND	-	Ground	Power	
32	**38**	GND	-	Ground	Power	
33	**39**	GND	-	Ground	Power	
35	**41**	GND	-	Ground	Power	
36	**42**	GND	-	Ground	Power	
46	**54**	GND	-	Ground	Power	
		SIM CARD Interface				

9	**11**	SIMVCC	-	External SIM signal – Power supply for the SIM	1.8 / 3V
10	**12**	SIMRST	O	External SIM signal – Reset	1.8 / 3V
11	**13**	SIMCLK	O	External SIM signal – Clock	1.8 / 3V
12	**14**	SIMIO	I/O	External SIM signal - Data I/O	1.8 / 3V
	Trace				
44	**52**	RXD_AUX	I	RX Data for debug monitor	CMOS 1.8V
45	**53**	TXD_AUX	O	TX Data for debug monitor	CMOS 1.8V
	Prog. / Data + Hw Flow Control				
1	**1**	C109/DCD	O	Output for Data carrier detect signal (DCD) to DTE	CMOS 1.8V
2	**2**	C125/RING	O	Output for Ring indicator signal (RI) to DTE	CMOS 1.8V
3	**3**	C107/DSR	O	Output for Data set ready signal (DSR) to DTE	CMOS 1.8V
4	**4**	C108/DTR	I	Input for Data terminal ready signal (DTR) from DTE	CMOS 1.8V

5	**5**	C105/RTS	I	Input for Request to send signal (RTS) from DTE	CMOS 1.8V
6	**6**	C106/CTS	O	Output for Clear to send signal (CTS) to DTE	CMOS 1.8V
7	**9**	C103/TXD	I	Serial data input (TXD) from DTE	CMOS 1.8V
8	**10**	C104/RXD	O	Serial data output to DTE	CMOS 1.8V
		Miscellaneous Functions			
43	**51**	VAUX/PWR MON	O	Supply Output for external accessories	CMOS1.8V
47	**55**	RESET*	I	HW unconditional shutdown (Active Low)	Open collector
30	**34**	VRTC 1)	AO	VRTC Backup capacitor	Power
		Telit GPIOs			
42	**48**	GPIO_01 / DVI_WA0	I/O	Telit GPIO_01 Configurable GPIO/ Digital Audio Interface (WA0)	CMOS 1.8V
41	47	GPIO_02 / JDR / DVI_RX	I/O	Telit GPIO_02 Configurable GPIO/ / Jammer Detect Report / Digital Audio Interface (RX)	CMOS 1.8V*

40	**46**	GPIO_03 / DVI_TX	I/O	Telit GPIO_03 Configurable GPIO/ Digital Audio Interface (TX)	CMOS 1.8V
39	45	GPIO_04/ TX Disable / DVI_CLK	I/O	Telit GPIO_04 Configurable GPIO/ TX Disable input / Digital Audio Interface (CLK)	CMOS 1.8V
29	**33**	GPIO_05 / RFTXMON	I/O	Telit GPIO_05 Configurable GPIO/ Transmitter ON monitor	CMOS 1.8V
28	32	GPIO_06 / ALARM	I/O	Telit GPIO_06 Configurable GPIO/ ALARM	CMOS 1.8V
27	**31**	GPIO_07 / BUZZER	I/O	Telit GPIO_07 Configurable GPIO/ Buzzer	CMOS 1.8V
26	30	GPIO_08/ STAT_LED	I/O	Telit GPIO_08 Configurable GPIO/ Status Led	CMOS 1.8V
		RF SECTION			
34	40	ANTENNA	I/O	GSM/EDGE/UMTS Antenna (50 ohm)	RF
		RESERVED			
		19, 31, 48			

(*) GL865-QUAD V4 digital pins are not CMOS 1.8V but CMOS 2.8V

Warning(*):

GL865-QUAD V4 digital pins are not CMOS 1.8V but CMOS 2.8V.

In order to design a board compatible with the other xL865 products , a level shifter should be considered.

Warning:

RESERVED pins reported above must not be connected.

Unlike other Telit's products the RTC feature of CL865 cannot be operated with VRTC only and the external RTC backup capacitor will be also useless.. VBATT must be connected to support RTC feature for CL865

The internal GPIO’s pull up/pull down could be set to the preferred status for the application using the AT#GPIO command.

Please refer for the AT Commands User Guide for the detailed command Syntax..

4.1. PIN-OUT differences UL865,GL865-V3,UL865

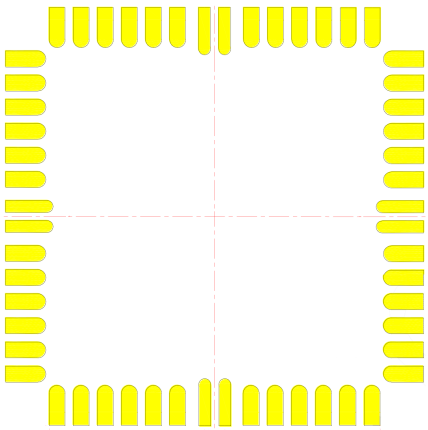
Pin	Module	Signal	I/O	Function
16	UL865	USB_VBUS	AI	Power sense for the internal USB transceiver.
16	GL865 V3	RESERVED	-	-
16	CL865	USB_VBUS	AI	Power for the internal USB transceiver.
17	UL865	USB_D-	I/O	USB differential Data (-)
17	GL865 V3	RESERVED	-	-
17	CL865	USB_D-	I/O	USB differential Data (-)
18	UL865	USB_D+	I/O	USB differential Data (+)
18	GL865 V3	RESERVED	-	-
18	CL865	USB_D+	I/O	USB differential Data (+)
20	UL865	RESERVED	-	-
20	GL865 V3	EAR-	AO	Earphone signal output, phase -
20	CL865	EAR-	AO	Earphone signal output, phase -

21	UL865	RESERVED	-	-
21	GL865	EAR+	AO	Earphone signal output, phase +
21	CL865	EAR+	AO	Earphone signal output, phase +
22	UL865	RESERVED	-	-
22	GL865	Mic-	AI	Mic. signal input; phase-
22	CL865	Mic-	AI	Mic. signal input; phase-
24	UL865	RESERVED	-	-
24	GL865	Mic+	AI	Mic. signal input; phase+
24	CL865	Mic+	AI	Mic. signal input; phase+
25	UL865	SPI_CLK	I/O	SPI_CLK
25	GL865	RESERVED	-	-
25	CL865	RESERVED	-	-

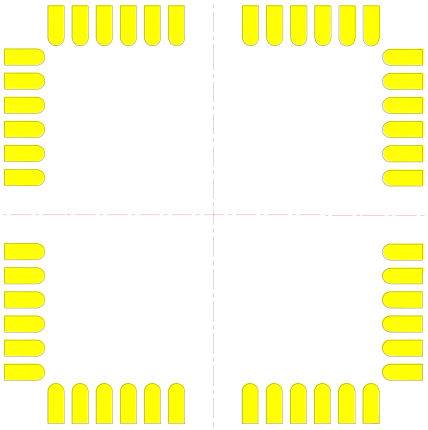
5. LEGACY VS NEW XL865 FORM FACTOR

In order to host in the same PCB the legacy GL865-QUAD V3/UL865/CL865 and the new ML865C1/GL865-QUAD V4 the ML865C1 pinout and form factor should be used.

Two different solder paste stencils are required in order to remove the solder paste from the pins 7,8,50,49,36,35,21,22 in the products where they are not present as shown in the following picture.



ML865C1/GL865-QUAD V4
PASTE STENCIL



GL865-QUAD V3/V3.1 / UL865 / CL865
PASTE STENCIL

Warning:

On the WAKE UP pin a zero ohm series resistor should be placed , between the AP and the module.The resistor shall be mounted for the ML865C1 and not populated for the other products.

Warning:

GL865-QUAD V4 digital pins are not CMOS 1.8V but CMOS 2.8V.

In order to design a board compatible with the other xL865 products , a level shifter shold be considered.

6. LOGIC LEVEL SPECIFICATION

The following tables show the logic level specifications for GL865 V3, UL865 and CL865:

Absolute Maximum Ratings -Not Functional

	GL865 V3		UL865		CL865	
Parameter	Min	Max	Min	Max	Min	Max
Input level on any digital pin (CMOS 1.8) with respect to ground	-0.3V	2.1V	-0.3V	2.3V	-0.3V	2.3V

	GL865-QUAD V4 (CMOS 2.8)		ML865C1 (CMOS 1.8)	
Parameter	Min	Max	Min	Max
Input level on any digital pin (CMOS 1.8) with respect to ground	-	-	-0.3V	2.1V
Input level on any digital pin (CMOS 2.8) with respect to ground	-0.3V	+3.1V	-	-

Operating Range - Interface levels (1.8V CMOS)

	GL865 V3 (1.8V CMOS)		UL865 (1.8V CMOS)		CL865 (1.8V CMOS)	
Parameter	Min	Max	Min	Max	Min	Max
Input high level	1.3V	1.9V	1.5V	1.9V	1.5V	2.1V
Input low level	0.0V	0.35V	0.0V	0.35V	0.0V	0.35V
Output high level	1.6V	1.9V	1.6V	1.9V	1.35V	1.8V
Output low level	0.0V	0.2V	0.0V	0.2V	0.0V	0.45V

	GL865-QUAD V4 (2.8V CMOS)		ML865C1 (1.8V CMOS)	
Parameter	Min	Max	Min	Max
Input high level	2.1V	3.1V	1.5V	1.9V
Input low level	0V	0.7V	0V	0.35V
Output high level	2.4V	3.1V	1.6V	1.9V
Output low level	0V	0.4V	0V	0.2V

Current characteristics

	GL865 V3	UL865	CL865
Parameter	Typical	Typical	Typical

Output Current	1mA	1mA	2mA
Input Current	1µA	1µA	30µA

	GL865 V4	ML865C1
Parameter	Typical	Typical
Output Current	1mA	1mA
Input Current	1mA	1uA

7. USB PORT

The UL865 and CL865 include an integrated universal serial bus (USB) transceiver, compliant with USB 2.0 specifications and supporting the USB Full-Speed (12Mb/s) mode. The UL865 supports also High-Speed (480Mb/s) mode. For this reason the signal traces should be routed carefully: trace lengths, number of vias and capacitive loading should be minimized and the characteristic impedance value should be as close as possible to 90 Ohms differential.

The impedance value of USB_DPLUS and USB_DMINUS signals for CL865 should be as close as possible to 100 Ohms differential.

Pins 16, 17 and 18 are internally unconnected on GL865 V3 so in a common design the USB port can be routed to the MCU in order to have the possibility to use it in case UL865 and CL865 are mounted.

If not used we suggest routing pins 16, 17 and 18 of xL865 to test points (or better to a mini USB connector not mounted).

Pin	Module	Signal	I/O	Function
16	UL865	USB_VBUS	AI	Power sense for the internal USB transceiver.
16	GL865 V3	RESERVED	-	-
16	CL865	USB_VBUS	AI	Power for the internal USB transceiver.
18	ML865C1	USB_VBUS	AI	Power for the internal USB transceiver.
18	GL865-QUAD V4	USB_VBUS	AI	Power for the internal USB transceiver.
17	UL865	USB_D-	I/O	USB differential Data (-)
17	GL865 V3	RESERVED	-	-
17	CL865	USB_D-	I/O	USB differential Data (-)
19	ML865C1	USB_D-	I/O	USB differential Data (-)

19	GL865-QUAD V4	USB_D-	I/O	USB differential Data (-)
18	UL865	USB_D+	I/O	USB differential Data (+)
18	GL865 V3	RESERVED	-	-
18	CL865	USB_D+	I/O	USB differential Data (+)
20	ML865C1	USB_D+	I/O	USB differential Data (+)
20	GL865-QUAD V4	USB_D+	I/O	USB differential Data (+)
20	UL865	RESERVED	-	-

8. SPI PORT

The UL865 module is provided with one 3 wire slave SPI interface. The AP has the master role i.e. it supplies the clock. The following table is listing the available signals:

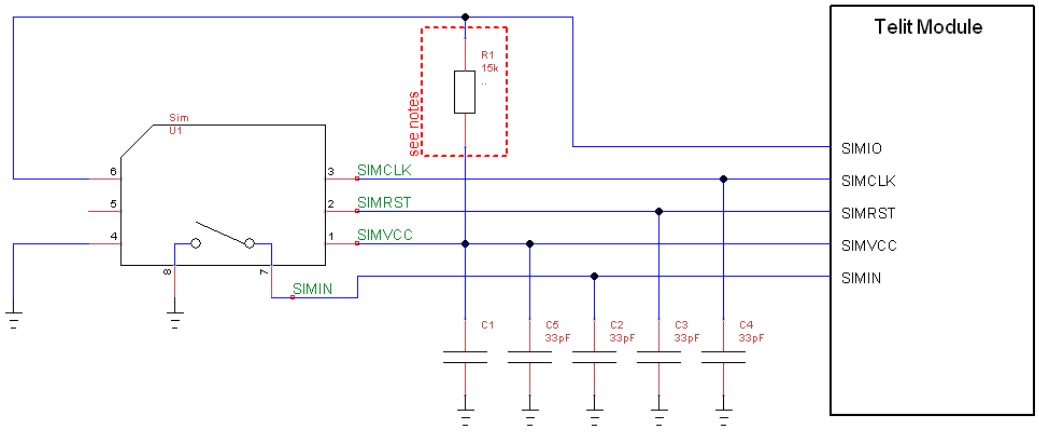
PAD	Model	Signal	I/O	Function	COMMENT
45	UL865	SPI_MOSI/ TX_AUX	I/O	SPI MOSI	Shared with TX_AUX
45	GL865	TX_AUX	O	Auxiliary UART (TX Data to DTE)	
45	CL865	TX_AUX	O	Auxiliary UART (TX Data to DTE)	
53	ML865C1	TXD_AUX/ SPI_MOSI	O	Auxiliary UART (TX Data to DTE	
44	UL865	SPI_MISO/ RX_AUX	I/O	SPI MISO	Shared with RX_AUX
44	GL865	RX_AUX	I	Auxiliary UART (RX Data from DTE)	
44	CL865	RX_AUX	I	Auxiliary UART (RX Data from DTE)	
52	ML865C1 GL864-V4	SPI_MISO	I	RX_AUX/SPI_ MISO	
25	UL865	SPI_CLK	I	SPI CLK	
25	GL865	RESERVED	-	-	-
25	CL865	RESERVED	-	RESERVED	
29	ML865C1	SPI_CLK	I	GPIO_08/GNSS_LNA_EN)	

Warning:
In a common design xL865 the SPI port should not be used.

Due to the shared functions, when the SPI port is used, it is not possible to use the AUX_UART port.

9. SIM CONNECTION

The figure below illustrates in particular how the application side should be designed, and what values the components should have.



The minimum value of C1 can vary depending on the module; in the table below you have the recommended values. The maximum for all modems is 1uF.

Module	C1
GL865-QUAD V3	220nF
UL865	100nF
GL865-QUAD V4	470nF
ML865C1	100nF to 1uF
CL865	100nF

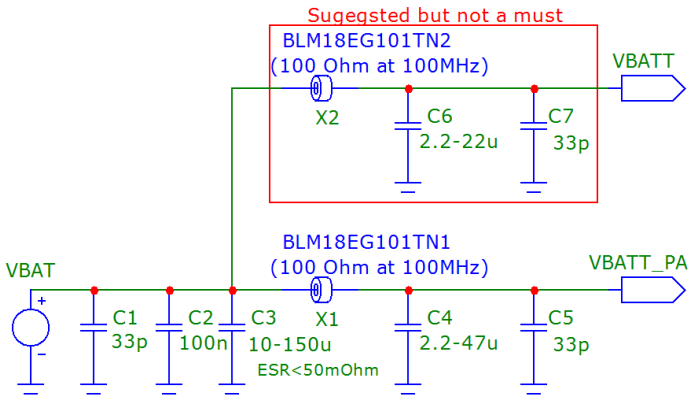
10. FREQUENCY BANDS

Module + Region Variant	LTE FDD	LTE TDD	3G	TD-SCDMA	2G	CDMA
GL865-QUAD V4	-	-	-	-	GSM850, 900 1800,1900	
GL865-QUAD v3					GSM850,900 1800,1900	
ML865C1-NA	B2,B4,B12, B13					
ML865C1-EA	B3, B8, ,B20				GSM850, 900 1800,1900	
UL865-EU			FDD B1,B8		GSM900, 1800	
UL865-NA			FDD B2, B5		GSM850, 1900	

11. POWER SUPPLY

The power supply circuitry and board layout are a very important part in the full product design and they strongly reflect on the product overall performances, hence read carefully the requirements and the guidelines that will follow for a proper design.

To improve EMI filtering an EMI suppression circuitry must be added on modem's VBATT_PA, and if possible also on VBATT. Follow schematic on figure below.



12. DOCUMENT HISTORY

Revision	Date	Changes
0	2013-10-07	Initial release
1	2014-01-08	Added CL865
2	2018-12-04	Updated template Added ML865C1 and GL865 V4

SUPPORT INQUIRIES

Link to **www.telit.com** and contact our technical support team for any questions related to technical issues.

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