LE910R1

HW Design Guide

1VV0301754 Rev. 1 – 2022-03-07

Telit Technical Documentation

APPLICABILITY TABLE

PRODUCTS
LE910R1-EU
LE910R1-BR

CONTENTS

1. INTRODUCTION

1.1. Scope

This document introduces the Telit LE910R1 module and presents possible and recommended hardware solutions for the development of a product based on the LE910R1 module. All the features and solutions described in this document are applicable to all LE910R1 variants, where "LE910R1" refers to the variants listed in the applicability table.

If a specific feature is applicable to a specific product only, it will be clearly marked.

Note: LE910R1 refers to all modules listed in the Applicability Table.

This document covers all the basic functions of a wireless module; it cannot include every hardware solution or every product that can be designed. Where the suggested hardware configurations are not to be considered mandatory, the information provided should be used as a guide and starting point to successfully develop the product with the Telit LE910R1 module.

Note: The integration of the GSM/GPRS/EGPRS/ LTE LE910R1 cellular module within a user application must be done according to the design rules described in this manual.

1.2. Audience

This document is intended for system integrators that are using the Telit LE910R1 module in their products.

1.3. Contact Information, Support

For technical support and general questions please e-mail:

- *TS-EMEA@telit.com*
- *TS-AMERICAS@telit.com*
- *TS-APAC@telit.com*

Alternatively, use:

https://www.telit.com/contact-us/

Product information and technical documents are accessible 24/7 on our web site:

https://www.telit.com

1.4. Symbol Conventions

⚠	**Danger:** This information MUST be followed or catastrophic equipment failure or personal injury may occur.
✋	**Warning:** Alerts the user on important steps about the module integration.
📌	**Note/Tip:** Provides advice and suggestions that may be useful when integrating the module.
⚠	**Electro-static Discharge:** Notifies the user to take proper grounding precautions before handling the product.

Table 1: Symbol Conventions

All dates are in ISO 8601 format, that is YYYY-MM-DD.

1.5. Related Documents

- 80672ST11051A LE910S1/LE910R1 AT Command Reference Guide

2. GENERAL PRODUCT DESCRIPTION

2.1. Overview

The LE910R1 is an industrial-grade, cost-optimized LTE Cat1 Bis module series ideal for IoT applications that need data and voice transmission, it also supports 2G fallback. The use of a Single Antenna reduces the hardware design complexity, bringing significant cost savings compared to LTE Cat 1 modules with two antennas, and allowing for the reduction of the overall device dimensions, making it possible to serve IoT applications with stringent size requirements.

LE910R1 is available in hardware variants as listed in Applicability Table. For differences in the designated RF band sets – refer to Section 6.1. Bands Variants.

Note:

(EN) The integration of the LE910R1 cellular module within user application shall be done according to the design rules described in this manual.

(IT) L'integrazione del modulo cellulare LE910R1 all'interno dell'applicazione dell'utente dovrà rispettare le indicazioni progettuali descritte in questo manuale.

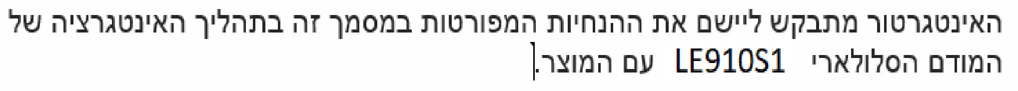
(DE) Die Integration des LE910R1 Mobilfunk-Moduls in ein Gerät muß gemäß der in diesem Dokument beschriebenen Kunstruktionsregeln erfolgen.

(SL) Integracija LE910R1 modula v uporabniški aplikaciji bo morala upoštevati projektna navodila, opisana v tem priročniku.

(SP) La utilización del modulo LE910R1 debe ser conforme a los usos para los cuales ha sido deseñado descritos en este manual del usuario.

(FR) L'intégration du module cellulaire LE910R1 dans l'application de l'utilisateur sera faite selon les règles de conception décrites dans ce manuel.

(HE)



האינטגרטור מתבקש ליישם את ההנחיות המפורטות במסמך זה בתהליך האינטגרציה של
המודם הסלולארי LE910S1 עם המוצר.

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2.2. Product Variants and Frequency Bands

Table 2 summarizes all region variants within the LE910R1 family, showing the band sets supported in each variant.

Different bands combinations are available:

Region Variant	2G	LTE FDD
LE910R1-EU	B3 (1800), B8 (900)	B1, B3, B7, B8, B20, B28
LE910R1-BR	B2 (1900), B3 (1800), B5 (850), B8 (900)	B1, B3, B5, B7, B8, B28

Table 2: RF Bands Variant

Refer to "RF Section" for details information about frequencies and bands.

Note: Cellular technologies and frequency bands that are enabled may vary based on firmware version and firmware configuration used.

2.3. Target Market

LE910R1 can be used for applications where tamper-resistance, confidentiality, integrity, and authenticity of end-user information are required, for example:

- Emergency call
- Road pricing
- Pay-as-you-drive insurance
- Internet connectivity

2.4. Main Features

The LE910R1 series of cellular modules features an LTE CAT1,GSM modem baseband and RF transceiver to cover 700MHz~2.7GHz bands for worldwide roaming.

Function	Features

Modem	• FDD LTE CAT1 Bis
	  ○ DL 10Mbps/ UL 5Mbps
	  ○ LTE+LTE dual-SIM dual-standby supported
	  ○ VoLTE supported
	• GSM/GRPS/EDGE Class 12
	• Support for SIM profile switching
	• Regional variants with optimal choice of RF bands for worldwide coverage of countries and MNOs

Audio
Audio
	• Integrated High quality audio codec and audio front-end
	  ○ ADC: 90dB SNR@20~20kHz
	  ○ DAC: 95dB SNR@20~20kHz
	• Single MICs input
	• Stereo audio output
	• Audio content sampling rates: 8kHz to 48kHz
	• Quad vocoders for adaptive multi-rate (AMR)
	• Noise suppression and echo cancellation
	• Digital side tone generator with programmable gain
	• Voice power amplifier with programmable gain

SIM	• Dual SIM/USIM card controller

Application processor	• Application processor to run customer application code
	  ○ ARM Cortex-R5 with 832MHz clock
	  ○ 32K I-Cache
	  ○ 32K D-Cache
	  ○ 64KB ATCM and 64KB BTCM
	  ○ 64KB ROM and 64KB on-chip SRAM for application usage

Interfaces	Rich set of interfaces, including:
	• USB2.0 – USB port is typically used for:
	  ○ Flashing of firmware and module configuration
	  ○ Production testing
	  ○ AT command access
	  ○ Diagnostic monitoring and debugging
	• Peripheral Ports –I2C, UART
	• GPIOs
	• Antenna ports

Form factor	Form factor (28x28mm), accommodating the multiple RF bands in each region variant
Environment and quality requirements	The entire module is designed and qualified by Telit for satisfying the environment and quality requirements.
Single supply module	The module generates all its internal supply voltages.
RTC	No dedicated RTC supply, RTC is supplied by VBATT
Operating temperature	Range -40 °C to +85 °C (conditions as defined in Section 2.8 Temperature Range

Table 3: Features Table

2.4.1 Block Diagram

Figure below shows an overview of the internal architecture of the LE910R1 module. It includes the following sub-functions:

- Application processor and Modem subsystem with their external interfaces. These two functions are contained in a single SOC.
- RF front end and antenna ports.
- Rich IO interfaces. Depending on which LE910R1 software features are enabled, some of its exported interfaces due to multiplexing may be used internally and therefore may not be usable by the application.
- PMIC with the RTC function inside

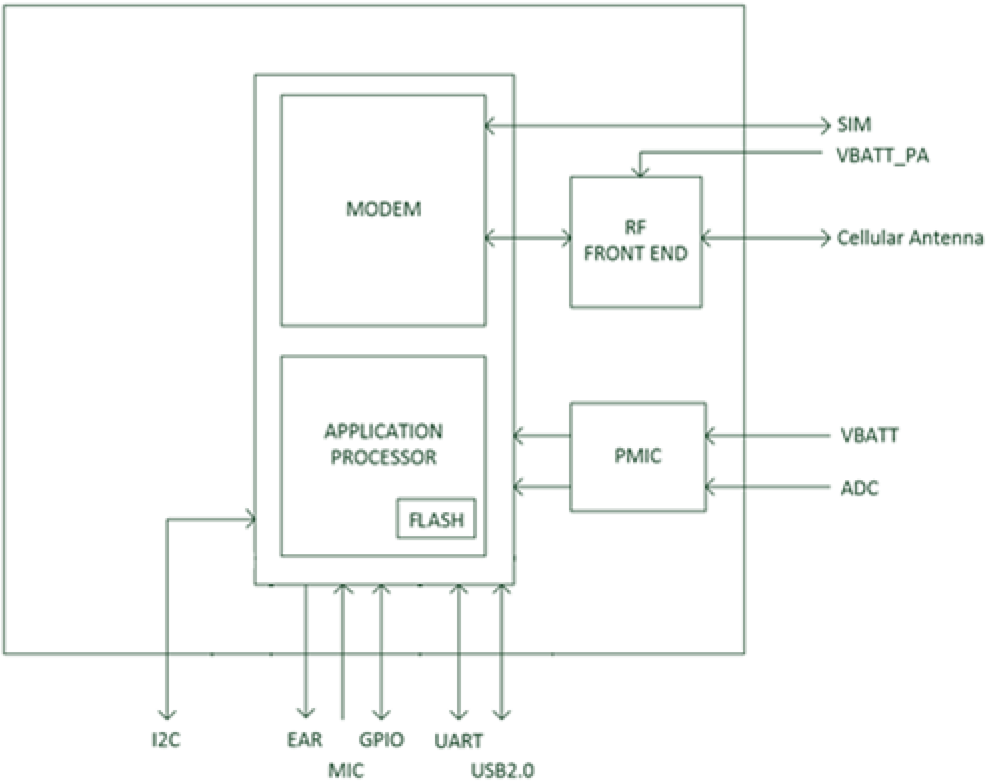


Figure 1: Block Diagram

2.5. TX Output Power

Typical values for Max output level are as follow:

Band	Power class
2G EGSM 900 - 2G EGSM 850	Class 4 (2W)
2G DCS 1800 - 2G PCS 1800	Class 1 (1W)
4G LTE (FDD) All Bands	Class 3 (0.2W)

Table 4: Transmission Output Power

Band	Mode	Class	RF power (dBm)
B8 900, B5 850	2G GSM/GPRS	4	33dBm +/- 1dB
	2G EGPRS	E2	27dBm +/- 1dB
B3 1800, B2 1900	2G GSM/GPRS	1	30dBm +/- 1dB
	2G EGPRS	E2	26dBm +/- 1dB
B1, B3, B5, B7, B8, B20, B28A, B28B	4G LTE FDD -CAT1	3	23dBm +/- 1dB

Table 5: Transmission Output Power - Band

2.6. RX Sensitivity

Below the 3GPP measurement conditions used to define the RX sensitity:

Technology	3GPP Compliance
2G GSM/GPRS	BER Class II <2.44%
4G LTE	Throughput >95% 10MHz

Table 6: Reception Sensitivity

Mode	Primary	3GPP
DCS 1800 - B3	-107.5	-102
EGSM 900 – B8	-109	-102
PCS 1900 – B2	-107.5	-102
EGSM 850 – B5	-109	-102
LTE 2100 – B1	-99.0	-96.3
LTE 1800 – B3	-97.5	-93.3
LTE 850 – B5	-99.5	-94.3
LTE 2600 – B7	-97.5	-94.3
LTE 900 – B8	-99	-93.3

Mode	Primary	3GPP
LTE 800 – B20	-99.5	-93.3
LTE 700 – B28A/B	-99	-94.8

Table 7: Typical sensitivity levels

Note: The sensitivity level may present a deviation of approximately +/- 2dB depending on model, device and channel; the level shown is the typical value.

2.7. Mechanical Specifications

2.7.1. Dimensions

The overall dimensions of LE910R1 are:

XYZ	mm
Length	28.2 mm, +/- 0.15 mm tolerance
Width	28.2 mm, +/- 0.15 mm tolerance
Thickness	2.5 mm, +/- 0.2 mm tolerance

Table 8: LE910R1 dimensions

Note: Consider a typical label thickness of 0.1 mm in addition to the module thickness.

2.7.2. Weight

The nominal weight of the LE910R1 module is 3.7 grams.

2.8. Temperature Range

Mode	Temperature	Note
Operating Temperature Range	–20°C ÷ +55°C	The module is fully functional(*) in all the temperature range and it fully meets the 3GPP specifications.
	–40°C ÷ +85°C	The module is fully functional (*) in all the temperature range, might slightly deviate from the 3GPP specifications.
Storage and non-operating Temperature Range	–40°C ÷ +85° C	The module is not powered and not connected to power supply

Table 9: Temperature Range

Note: (*) Functional: if applicable, the module is able to make and receive voice calls, data calls, send and receive SMS and data traffic.

3. PINS ALLOCATION

3.1. Pin-out

PAD	Signal	I/O	Function	Type	Comment
USB HS 2.0 Communication Port					
B15	USB_D+	I/O	USB differential Data (+)		
C15	USB_D-	I/O	USB differential Data (-)		
A13	USB_VBUS	AI	Power sense for the internal USB transceiver	Power	
F14	FORCED_USB_BOOT	I	FORCED_USB_BOOT	1.8V	Pull down to GND to enter emergency download mode
Asynchronous UART					
N15	C103/TXD	I	Serial data input (TXD) from DTE	1.8V	
M15	C104/RXD	O	Serial data output to DTE	1.8V	
M14	C108/DTR	I	Input for Data Terminal Ready (DTR) from DTE	1.8V	
L14	C105/RTS	I	Input for Request to send signal (RTS) from DTE	1.8V	
P15	C106/CTS	O	Output for Clear to send signal (CTS) to DTE	1.8V	
N14	C109/DCD	O	Output for Data Carrier Detect (DCD) to DTE	1.8V	
P14	C107/DSR	O	Output for Data Set Ready (DSR) to DTE	1.8V	
R14	C125/RING	O	Output for Ring Indication (RI) to DTE	1.8V	
K4	DEBUG_UART_TXD	O	Trace UART TX	1.8V	UART_DEBUG
M6	DEBUG_UART_RXD	I	Trace UART RX	1.8V	
AUX UART					
D15	TX_AUX	O	TX_AUX	1.8V	
E15	RX_AUX	I	RX_AUX	1.8V	
SIM Card Interface 1					
A6	SIMCLK1	O	External SIM 1 signal – Clock	1.8/3.3V	
A7	SIMRST1	O	External SIM 1 signal – Reset	1.8/3.3V	

PAD	Signal	I/O	Function	Type	Comment
A5	SIMIO1	I/O	External SIM 1 signal - Data I/O	1.8/3.3V	Internally PU 4.7 kΩ to SIMVCC1
A4	SIMIN1	I	External SIM 1 signal - Presence	1.8V	Active low
A3	SIMVCC1	-	External SIM 1 signal – Power supply for SIM 1	1.8/3.3V	
SIM Card Interface 2					
C1	SIMCLK2	O	External SIM 2 signal – Clock	1.8/3.3V	
D1	SIMRST2	O	External SIM 2 signal – Reset	1.8/3.3V	
C2	SIMIO2	I/O	External SIM 2 signal – Data I/O	1.8/3.3V	Internally PU 4.7kΩ to SIMVCC2
G4	SIMIN2	I	External SIM 2 signal – Presence	1.8V	Active low
D2	SIMVCC2	-	External SIM 2 signal – Power supply for SIM 2	1.8/3.3V	
General Purpose Digital I/O					
C8	GPIO_1	I/O	GPIO_1 / STAT_LED	1.8V	Alternate Fn STAT_LED
C9	GPIO_2	I/O	GPIO_2	1.8V	
C10	GPIO_3	I/O	GPIO_3/I2C2_SCL	1.8V	Alternate Fn I2C
C11	GPIO_4	I/O	GPIO_4/I2C2_SDA	1.8V	Alternate Fn I2C
B14	GPIO_5	I/O	GPIO_5/I2C3_SCL	1.8V	Alternate Fn I2C
C12	GPIO_6	I/O	GPIO_6/I2C3_SDA	1.8V	Alternate Fn I2C
C13	GPIO_7	I/O	GPIO_7	1.8V	
K15	GPIO_8	I/O	GPIO_8/ SW_RDY	1.8V	Alternate Fn SW_RDY
L15	GPIO_9	I/O	GPIO_9	1.8V	
G15	GPIO_10	I/O	GPIO_10	1.8V	
RF Section					
K1	Antenna	I/O	GSM/EDGE/LTE Main antenna (50 Ohm)	RF	
Miscellaneous Functions					
R12	ON_OFF_N	I	Power ON / Power OFF input		Active low
R13	HW_SHUTDOWN_N	I	Unconditional Shutdown input		Active low

PAD	Signal	I/O	Function	Type	Comment
R11	VAUX/PWRMON	O	Supply output for external accessories / Power ON monitor	1.8V	
E13	VIO_1V8	O	IO voltage for internal ICs This power rail is always on while LE910R1 is working.	1.8V	
B1	ADC_IN1	AI	Analog/Digital Converter Input 1	Analog	
H4	ADC_IN2	AI	Analog/Digital Converter Input 2	Analog	
K3	ATC1	I/O	Antenna Tuner Ctrl	1.8V	RF GPIO
L3	ATC2	I/O	Antenna Tuner Ctrl	1.8V	RF GPIO
I2C Interface					
B11	I2C_SCL	I/O	I2C clock	1.8V	Need external PU 4.7kΩ to 1.8V
B10	I2C_SDA	I/O	I2C Data	1.8V	Need external PU 4.7kΩ to 1.8V
Analog Audio					
B2	EAR+	O	Analog Audio (EAR+)	Analog	
B3	EAR-	O	Analog Audio (EAR-)	Analog	
B4	MIC+	I	Analog Audio (MIC+)	Analog	
B5	MIC-	I	Analog Audio (MIC-)	Analog	
Antenna Tuner					
L3	ATC1	O	Antenna Tuner Ctrl	1.8V	
K3	ATC2	O	Antenna Tuner Ctrl	1.8V	
Power Supply					
M1	VBATT	-	Main Power Supply (Digital Section)	Power	
M2	VBATT	-	Main Power Supply (Digital Section)	Power	
N1	VBATT_PA	-	Main Power Supply (RF Section)	Power	
N2	VBATT_PA	-	Main Power Supply (RF Section)	Power	
P1	VBATT_PA	-	Main Power Supply (RF Section)	Power	
P2	VBATT_PA	-	Main Power Supply (RF Section)	Power	
A2	GND	-	Ground		

PAD	Signal	I/O	Function	Type	Comment
B13	GND	-	Ground		
D4	GND	-	Ground		
E1	GND	-	Ground		
E2	GND	-	Ground		
E14	GND	-	Ground		
F2	GND	-	Ground		
G1	GND	-	Ground		
G2	GND	-	Ground		
G7	GND	-	Ground		
G8	GND	-	Ground		
G9	GND	-	Ground		
H1	GND	-	Ground		
H2	GND	-	Ground		
H7	GND	-	Ground		
H8	GND	-	Ground		
H9	GND	-	Ground		
J1	GND	-	Ground		
J2	GND	-	Ground		
J7	GND	-	Ground		
J8	GND	-	Ground		
J9	GND	-	Ground		
K2	GND	-	Ground		
L1	GND	-	Ground		
L2	GND	-	Ground		
M3	GND	-	Ground		
M4	GND	-	Ground		
M12	GND	-	Ground		
N3	GND	-	Ground		
N4	GND	-	Ground		
N5	GND	-	Ground		
N6	GND	-	Ground		
P3	GND	-	Ground		

PAD	Signal	I/O	Function	Type	Comment
P4	GND	-	Ground		
P5	GND	-	Ground		
P6	GND	-	Ground		
P8	GND	-	Ground		
P9	GND	-	Ground		
P10	GND	-	Ground		
P13	GND	-	Ground		
R2	GND	-	Ground		
R3	GND	-	Ground		
R5	GND	-	Ground		
R6	GND	-	Ground		
R8	GND	-	Ground		
R10	GND	-	Ground		
Reserved for Internal Use					
D12	Reserved	-	Reserved		
F15	Reserved	-	Reserved		
H14	Reserved	-	Reserved		
J12	Reserved	-	Reserved		
F12	Reserved	-	Reserved		
E12	Reserved	-	Reserved		
G12	Reserved	-	Reserved		
K12	Reserved	-	Reserved		
H12	Reserved	-	Reserved		
G13	Reserved	-	Reserved		
F13	Reserved	-	Reserved		
N13	Reserved	-	Reserved		
L13	Reserved	-	Reserved		
J13	Reserved	-	Reserved		
M13	Reserved	-	Reserved		
K13	Reserved	-	Reserved		
H13	Reserved	-	Reserved		
L12	Reserved	-	Reserved		

PAD	Signal	I/O	Function	Type	Comment
M11	Reserved	-	Reserved		
M10	Reserved	-	Reserved		
L4	Reserved	-	Reserved		
B9	Reserved	-	Reserved		
B6	Reserved	-	Reserved		
B7	Reserved	-	Reserved		
B8	Reserved	-	Reserved		
B12	Reserved	-	Reserved		
Reserved					
A8	Reserved	-	Reserved		
A9	Reserved	-	Reserved		
A10	Reserved	-	Reserved		
A11	Reserved	-	Reserved		
A12	Reserved	-	Reserved		
A14	Reserved	-	Reserved		
C7	Reserved	-	Reserved		
D5	Reserved	-	Reserved		
D6	Reserved	-	Reserved		
D7	Reserved	-	Reserved		
D8	Reserved	-	Reserved		
D9	Reserved	-	Reserved		
D10	Reserved	-	Reserved		
D11	Reserved	-	Reserved		
D13	Reserved	-	Reserved		
D14	Reserved	-	Reserved		
E4	Reserved	-	Reserved		
F1	Reserved	-	Reserved		
F4	Reserved	-	Reserved		
G3	Reserved	-	Reserved		
H3	Reserved	-	Reserved		
H15	Reserved	-	Reserved		
J3	Reserved	-	Reserved		

PAD	Signal	I/O	Function	Type	Comment
J4	Reserved	-	Reserved		
J15	Reserved	-	Reserved		
M5	Reserved	-	Reserved		
M7	Reserved	-	Reserved		
M8	Reserved	-	Reserved		
M9	Reserved	-	Reserved		
N7	Reserved	-	Reserved		
N8	Reserved	-	Reserved		
N10	Reserved	-	Reserved		
N11	Reserved	-	Reserved		
N12	Reserved	-	Reserved		
P11	Reserved	-	Reserved		
P12	Reserved	-	Reserved		
C14	Reserved	-	Reserved		
C4	Reserved	-	Reserved		
C3	Reserved	-	Reserved		
C5	Reserved	-	Reserved		
C6	Reserved	-	Reserved		
D3	Reserved	-	Reserved		
E3	Reserved	-	Reserved		
F3	Reserved	-	Reserved		
R4	Reserved	-	Reserved		
R9	Reserved	-	Reserved		
R7	Reserved	-	Reserved		
N9	Reserved	-	Reserved		
G14	Reserved	-	Reserved		
J14	Reserved	-	Reserved		
K14	Reserved	-	Reserved		
P7	Reserved	-	Reserved		

Table 10: Pin-out Information

Note: When the UART signals are used as the communication port between the host and the modem, the RTS must be connected to GND (on the module side) if flow control is not used.

If the UART port is not used, all UART signals can be left disconnected

Note: The following pins are unique for the LE910R1 and may not be supported on other (former or future) xE910 family modules. Special care must be taken when designing the application board if future compatibility is required.
REF_CLK • I2C_SCL • I2C_SDA • ADC_IN1 • ADC_IN2

Warning: Reserved pins must not be connected.

3.2. Signals that Must Be Connected

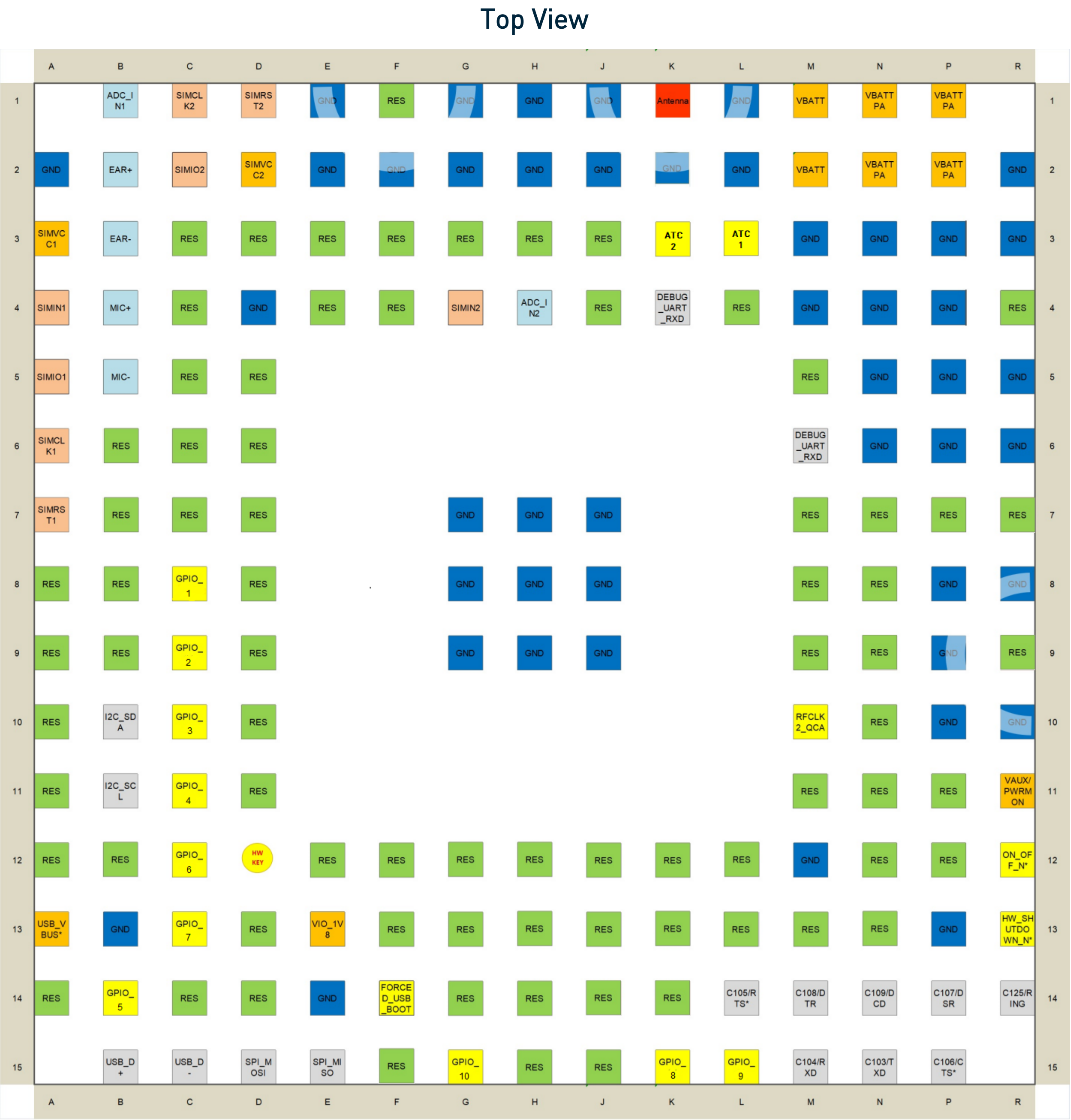
Table 11 lists the LE910R1 signals that must be connected even if not used by the end application:

PAD	Signal	Notes
M1, M2, N1, N2, P1, P2	VBATT & VBATT_PA	
A2, B13, D4, E1, E2, E14, F2, G1, G2, G7, G8, G9, H1, H2, H7, H8, H9, J1, J2, J7, J8, J9, K2, L1, L2, M3, M4, M12, N3, N4, N5, N6, P3, P4, P5, P6, P8, P9, P10, P13, R2, R3, R5, R6, R8, R10	GND	
R12	ON/OFF	Main power on off signal
R13	HW_SHUTDOWN_N	Emergency power off
B15	USB_D+	If not used, connect to a Test Point or an USB connector
C15	USB_D-	If not used, connect to a Test Point or an USB connector
A13	USB_VBUS	If not used, connect to a Test Point or an USB connector
F14	FORCED_USB_BOOT	If not used, connect to a Test Point

PAD	Signal	Notes
N15	C103/TXD	If not used, connect to a Test Point
M15	C104/RXD	If not used, connect to a Test Point
L14	C105/RTS	If flow control is not used, connect to GND
P15	C106/CTS	If not used, connect to a Test Point
K4	DEBUG_UART_TXD	If not used, connect to a Test Point
M6	DEBUG_UART_RXD	If not used, connect to a Test Point
C8	GPIO_1/STAT_LED	If not used, connect to a Test Point
K1	Antenna	MAIN antenna

Table 11: LE910R1 signals that must be connected

3.3. LGA Pads Layout



Top View

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
1		ADC_IN1	SIMCLK2	SIMRST2	GND	RES	GND	GND	GND	Antenna	GND	VBATT	VBATT PA	VBATT PA		1
2	GND	EAR+	SIMIO2	SIMVCC2	GND	GND	GND	GND	GND	GND	GND	VBATT	VBATT PA	VBATT PA	GND	2
3	SIMVCC1	EAR-	RES	RES	RES	RES	RES	RES	RES	ATC2	ATC1	GND	GND	GND	GND	3
4	SIMIN1	MIC+	RES	GND	RES	RES	SIMIN2	ADC_IN2	RES	DEBUG_UART_RXD	RES	GND	GND	GND	RES	4
5	SIMIO1	MIC-	RES	RES								RES	GND	GND	GND	5
6	SIMCLK1	RES	RES	RES								DEBUG_UART_RXD	GND	GND	GND	6
7	SIMRST1	RES	RES	RES			GND	GND	GND			RES	RES	RES	RES	7
8	RES	RES	GPIO_1	RES			GND	GND	GND			RES	RES	GND	GND	8
9	RES	RES	GPIO_2	RES			GND	GND	GND			RES	RES	GND	RES	9
10	RES	I2C_SDA	GPIO_3	RES								RFCLK2_QCA	RES	GND	GND	10
11	RES	I2C_SCL	GPIO_4	RES								RES	RES	RES	VAUX/PWRMON	11
12	RES	RES	GPIO_6	HW KEY	RES	RES	RES	RES	RES	RES	RES	GND	RES	RES	ON_OFF_N*	12
13	USB_VBUS*	GND	GPIO_7	RES	VIO_1V8	RES	RES	RES	RES	RES	RES	RES	RES	GND	HW_SHUTDOWN_N*	13
14	RES	GPIO_5	RES	RES	GND	FORCED_USB_BOOT	RES	RES	RES	RES	C105/RTS*	C108/DTR	C109/DCD	C107/DSR	C125/RING	14
15		USB_D+	USB_D-	SPI_MOSI	SPI_MISO	RES	GPIO_10	RES	RES	GPIO_8	GPIO_9	C104/RXD	C103/TXD	C106/CTS*		15
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

Figure 2: LGA Pads Layout

■ SUPPLY AND CONTROL
■ SIM CARD
■ ANALOG FUNCTIONALITY
■ GROUND
■ DIGITAL FUNCTIONALITY

■ DIGITAL COMMUNICATION
■ RF SIGNALS
■ RESERVED/NOT ASSIGNED/ RESERVED FOR FUTURE USE

4. POWER SUPPLY

The power supply circuitry and board layout are very important parts of the complete product design, with a critical impact on the overall product performance. Please read the following requirements and guidelines carefully to ensure a good and proper design..

4.1. Power Supply Requirements

The LE910R1 power requirements are as follows:

Power Supply	Value
Nominal Supply Voltage	3.8V
Operating Voltage Range	normal: 3.4 - 4.2 V extended 3.1 - 4.5 V
Max ripple on module input supply	30 mV

Table 12: Power Supply Requirements

Note: The Operating Voltage Range MUST never be exceeded; the application's power supply section must be designed with care to avoid an excessive voltage drop.

If the voltage drop exceeds the limits it may cause an unintentional module power off.

Note: For approval on the final products the power supply is required to be within the "Normal Operating Voltage Range". In the extended voltage operating range below the 3.4V the RF power could have some reduction.

4.2. Power Consumption

Table 13 provides typical current consumption values of LE910R1 for the various available modes.

Mode	Average (Typ.)	Mode Description
Switched Off		
Switched off	130uA	Module supplied but switched Off (RTC On)
Idle Mode (Standby Mode; No Call in Progress)		
AT+CFUN = 1	24mA	Module full functionality with power saving disabled

Mode		Average (Typ.)	Mode Description
DRX AT+CFUN=5	GSM	2mA	
	LTE		
Operative Mode (LTE)			
LTE (max power)		550mA	
LTE (0dBm)		260mA	
Operative Mode (GSM)			
GSM Tx and Rx mode			
GSM900/GSM850 PL5		GSM900: 230mA DCS1800: 160mA PCS1900: 160mA GSM850: 230mA	
DCS1800/PCS1900 PL0			
GPRS 2 Tx + 1 Rx			
GSM900/GSM850 PL5		GSM900: 380mA DCS1800: 255mA PCS1900: 255mA GSM850: 390mA	
DCS1800/PCS1900 PL0			

Table 13: Current Consumption

**Worst/best case current values depend on network configuration, not under module control.*

Note: The electrical design for the power supply must ensure a peak current output of at least 2.0A.

The support of specific network wireless technology depends on the product variant configuration.

Note: In GSM/GPRS mode, the RF transmission is not continuous, but is split into bursts at a base frequency of about 216 Hz with relative current peaks up to approximately 2.0A. Therefore, the power supply must be designed to withstand these current peaks without large voltage drops. This means that both the electrical design and the board layout must be designed for this current flow.

If the PCB layout is not well designed, a loud background noise is generated. This will be reflected on all audio paths producing an annoying audible noise at 216 Hz.

If the voltage drops during the peaks, the current absorption is too high. The device may even shut down due to a drop in the supply voltage.

4.3. General Design Rule

The principal guidelines for the Power Supply Design comprise three different design steps:

- the electrical design of the power supply
- the thermal design
- the PCB layout

4.3.1. Electrical Design Guidelines

The electrical design of the power supply strongly depends on the power source where this power is drained. We will distinguish them into three categories:

- +5V input (typically PC internal regulator output)
- +12V input (typically automotive)
- Battery

4.3.1.1. +5V Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V. So, the difference between the input source and the desired output is not big, and therefore a linear regulator can be used. A switching power supply is preferred to reduce power consumption.
- When using a linear regulator, a proper heat sink must be provided to dissipate the generated power.
- A low bypass ESR capacitor of adequate capacity must be provided to cut the current absorption peaks near the LE910R1 module. A 100 µF tantalum capacitor is usually suitable on both VBATT and VBATT_PA power lines.
- Make sure the low ESR capacitor on the output of the power supply (usually a tantalum one) is rated at least 10V.
- A protection diode must be placed near the power input to protect the LE910R1 module from power polarity inversion.

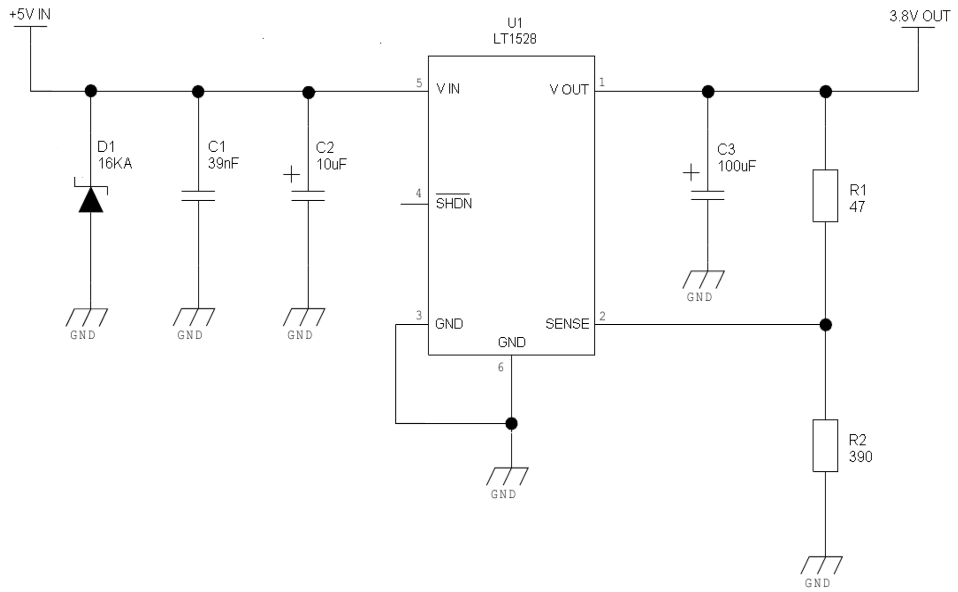


Figure 3: An Example of Linear Regulator with 5V Input

4.3.1.2. +12V Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, so due to the big difference between the input source and the desired output, a linear regulator is not suitable and shall not be used. A switching power supply will be preferable because of its better efficiency.
- When using a switching regulator, a 500kHz or more switching frequency regulator is preferable because of its smaller inductor size and its faster transient response. This allows the regulator to respond quickly to the current peaks absorption.
- In any case the frequency and Switching design selection is related to the application to be developed since the switching frequency could also generate EMC interferences.
- For the car PB battery the input voltage can rise up to 15,8V and this should be kept in mind when choosing components: all components in the power supply must withstand this voltage.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100µF capacitor is usually suitable.
- Make sure the low ESR capacitor on the power supply output is rated at least 10V.
- For Automotive applications a spike protection diode should be inserted close to the power input, in order to clean the supply from the spikes.

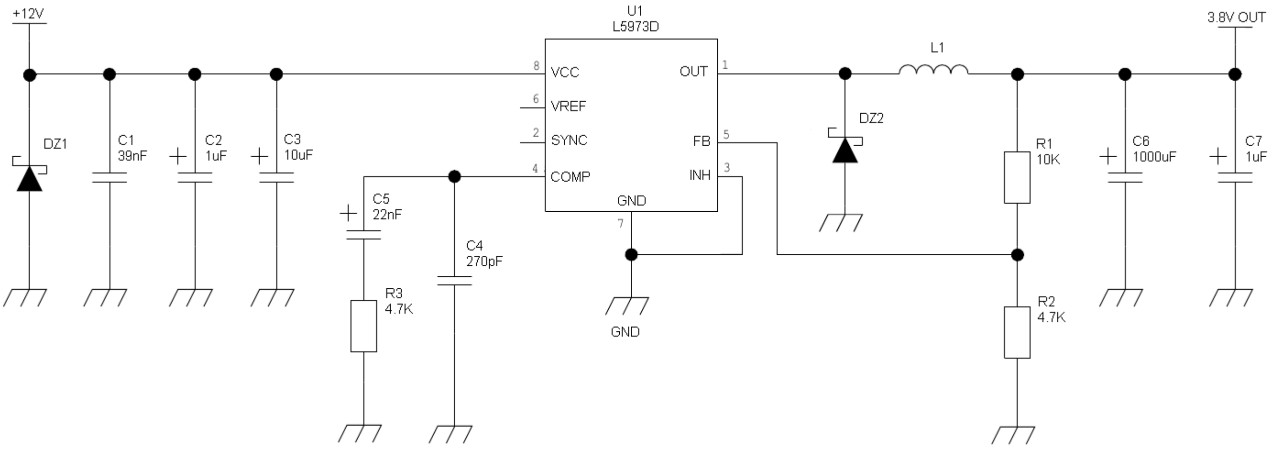


Figure 4: An Example of Switching Regulator with 12V Input

4.3.1.3. Battery Source Power Supply Design Guidelines

The desired nominal output for the power supply is 3.8V and the maximum voltage allowed is 4.2V. Hence a single 3.7V Li-Ion cell battery type is suitable for supplying the power to the LE910R1 module.

- A low ESR bypass capacitor of adequate capacity must be provided to cut the current absorption peaks; usually a 100µF tantalum capacitor is suitable.
- Make sure that the low ESR capacitor (usually a tantalum one) is rated at least 10V.
- A protection diode must be placed near the power input to protect the LE910R1 module from power polarity inversion. Otherwise, the battery connector must be done in such a way to avoid polarity inversions when connecting the battery.
- The battery capacity must be at least 500 mAh to withstand the current peaks of 2A.

Note: DON'T USE any Ni-Cd, Ni-MH, and Pb battery types directly connected with LE910R1. Their use can lead to overvoltage on the LE910R1 and damage it. USE ONLY Li-Ion battery types.

4.3.2. Thermal Design Guidelines

The thermal design for the power supply heat sink should be done with the following specifications:

- Considering the very low current during Idle, especially if the Power Saving function is enabled, it is possible to consider from the thermal point of view that the device absorbs significant current only during an Active Call or Data session.

- For the heat generated by the LE910R1 module, consider it to be 2W max during the GPRS Class12 upload transmission.
- In LTE mode, the LE910R1 emits RF signals continuously during transmission. Therefore, special attention must be paid on how to dissipate the heat generated.
- The LE910R1 is designed to conduct the heat flow from the module IC's towards the bottom of the PCB across GND metal layers
- The generated heat is mostly conducted to the grounding plane under the LE910R1 module. The application board should be properly designed to dissipate this heat.
- The design of the application board must ensure that the area under the LE910R1 module is as large as possible. Make sure the LE910R1 is mounted on the large ground area of application board and provides plenty of ground vias to dissipate heat.

Note: Make PCB design in order to have the best connection of GND pads to large surfaces of copper.

Note: The average consumption during transmission depends on the power level at which the device is requested to transmit over the network. Therefore, the average current consumption varies significantly.

Note: The thermal design for the power supply should be made keeping an average consumption at maximum transmission level during calls of LTE/GPRS.

4.3.3. Power Supply PCB Layout Guidelines

As seen in the electrical design guidelines, the power supply must have a low ESR capacitor on the output to cut the current peaks and a protection diode on the input to protect the supply from spikes and polarity inversion. The placement of these components is crucial for the correct operation of the circuitry. A misplaced component can be useless or can even decrease the performance of the power supply

- The Bypass low ESR capacitor must be placed close to the Telit LE910R1 power input pads or, in the case the power supply is a switching type it can be placed close to the inductor to cut the ripple provided the PCB trace from the capacitor to the LE910R1 is wide enough to ensure a voltage dropless connection even during 2A (GSM) current peak.

- The protection diode must be placed close to the input connector where the power source is drained.
- The PCB traces from the input connector to the power regulator IC must be wide enough to ensure that no voltage drops occur during the 2A current peaks.

  Note that this is not done in order to avoid RF power loss but to avoid voltage drops on the power line at the current peaks frequency of 216 Hz which will be reflected on all the components connected to that supply (also introducing the background noise at the burst base frequency).

  The PCB traces to LE910R1 and the bypass capacitor must be wide enough to ensure that no significant voltage drops occur when the 2A current peaks are absorbed. This is necessary for the same above-mentioned reasons. Try to keep these traces as short as possible.
- To reduce the EMI due to switching, it is important to keep the mesh involved very small; therefore the input capacitor, the output diode (if not embodied in the IC) and the regulator shall form a very small loop.This is done in order to reduce the radiated field (noise) at the switching frequency (100-500 kHz usually).
- The placement of the power supply on the board should be done in such a way to guarantee that the high current return paths in the ground plane are not overlapped to any noise sensitive circuitry as the microphone amplifier/buffer or earphone amplifier.
- The power supply input cables should be kept separate from noise sensitive lines such as microphone/earphone cables.
- The insertion of EMI filter on VBATT pins is suggested in those designs where antenna is placed close to battery or supply lines. A ferrite bead like Murata BLM18EG101TN1 or Taiyo Yuden P/N FBMH1608HM101 can be used for this purpose.

The below figure shows the recommended circuit:

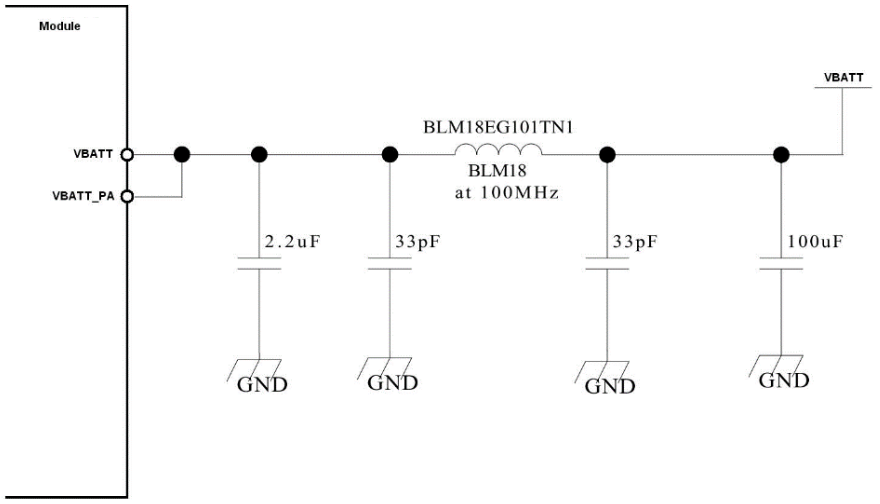


Figure 5: Recommended Circuit

4.3.4. Bypass Capacitor on Power Supplies

When a sudden voltage step to or cut from the power supplies is asserted, the steep transition causes some reactions such as overshoot and undershoot. This abrupt voltage transition can affect the device causing it to fail or to malfunction.

Bypass capacitors are needed to alleviate this behaviour. The behaviour may appear for different applications. Customers must pay special attention to this issue when they design their application board.

The length and width of the power lines must be considered carefully, and the capacitance of the capacitors must be selected accordingly.

The capacitor will also avoid power supplies ripple and the switching noise caused in TDMA systems, such as GSM.

In particular, a suitable bypass capacitor must be mounted on the following lines on the application board:

- VBATT & VBATT_PA (M1, M2, N1, N2, P1, P2)
- USB_VBUS (Pad A13)

Recommended values are:

- 100uF for both VBATT and VBATT_PA together
- 4.7uF for USB_VBUS (including the 1uF capacitor inside the module)

However, customers should consider that the capacitance mainly depends on the conditions of their application board.

Generally, more capacitance is required when the power line is longer.

4.4. VAUX Power Output

A regulated power supply output is provided to supply small devices from the module. This output is active when the module is ON and goes OFF when the module is shut down. The operating range characteristics of the supply are as follows:

Item	Min	Typical	Max
Output voltage	-	1.8V	-
Output current	-	-	50mA
Output bypass capacitor (inside the module)		2.2uF	

Table 14: Operating range characteristics of the supply

4.5. RTC Supply

The RTC within the LE910R1 module does not have a dedicated RTC supply pin. The RTC block is supplied by the VBATT supply.

When the VBATT is removed, RTC time is lost and RTC stopped; if you need to maintain the time and RTC running, VBATT must be supplied continuously.

In Power OFF mode, the average current consumption is ~130uA.

5. DIGITAL SECTION

5.1. Logic Levels

Unless otherwise specified, all the interface circuits of the LE910R1 are 1.8V CMOS logic. Only few specific interfaces (such as USIM) are capable of dual voltage I/O.

The following tables show the logic level specifications used in the LE910R1 interface circuits.

1.8V Pads - Absolute Maximum Ratings

Parameter	Min	Max
Input level on any digital pin when on	-0.3V	+2.2V
Input voltage on analog pins when on	-0.3V	+2.2 V

Table 15: Absolute Maximum Ratings - Not Functional

5.1.1. 1.8V Standard GPIOs

Pad	Parameter	Min	TYP	Max	Unit	Comment
V_{IH}	Input high level	VCC*0.7	1.8V	VCC+0.2	[V]	
V_{IL}	Input low level	-0.3	0V	0.3*VCC	[V]	
V_{OH}	Output high level	VCC-0.2V			[V]	
V_{OL}	Output low level			0.2V	[V]	
I_{IL}	Low-level input leakage current			10	[uA]	No pull-up
I_{IH}	High-level input leakage current	--		10	[uA]	No pull-down
R_{PU}	Pull-up resistance	55	79	121	[kΩ]	
R_{PD}	Pull-down resistance	51	87	169	[kΩ]	
C_i	Input capacitance	--		5	[pF]	

Table 16: Operating Range – Interface Levels (1.8V CMOS)

5.1.2. 1.8V SIM Card Pads

Pad	Parameter	Min	TYP	Max	Unit	Comment
V_{IH}	Input high level	VCC*0.7	1.8V	VCC+0.2	[V]	
V_{IL}	Input low level	-0.3V	0V	0.43V	[V]	

Pad	Parameter	Min	TYP	Max	Unit	Comment
V_{OH}	Output high level	1.35V	1.8V	1.875V	[V]	
V_{OL}	Output low level	0V	0V	0.2V	[V]	
I_{IL}	Low-level input leakage current	-		10	[uA]	No pull-up
I_{IH}	High-level input leakage current	-		10	[uA]	No pull-down
R_{PU}	Pull-up resistance		45		[kΩ]	
R_{PD}	Pull-down resistance		45		[kΩ]	
C_i	Input capacitance			5	[pF]	

Table 17: Operating Range – SIM Pads Working at 1.8V

5.1.3. Dual Voltage Pads - Absolute Maximum Ratings

Parameter	Min	Max
Input level on any digital pin when on	-0.3V	+3.6V
Input voltage on analog pins when on	-0.3V	+3.6 V

Table 18: Absolute Maximum Ratings - Not Functional

5.1.4. SIM Card Pads @3.3V

Pad	Parameter	Min	TYP	Max	Unit	Comment
V_{IH}	Input high level	2	3.3 (VCC)	VCC+0.3	[V]	
V_{IL}	Input low level	-0.3	0V	0.8	[V]	
V_{OH}	Output high level	2.4			[V]	
V_{OL}	Output low level			0.4V	[V]	
I_{IL}	Low-level input leakage current			10	[uA]	No pull-up
I_{IH}	High-level input leakage current			10	[uA]	No pull-down
R_{PU}	Pull-up resistance	26	47	72	[kΩ]	
R_{PD}	Pull-down resistance	27	54	27	[kΩ]	
C_i	Input capacitance			5	[pF]	

Table 19: Operating Range – For SIM Pads Operating at 3.3V

5.2. Power On

To turn on the LE910R1 module, the ON_OFF_N pad must be asserted low for more than 3.2 seconds and less than 6.8 seconds, and then released.

The maximum current that can be drained from the ON/OFF # pad is 0.12 mA. This pin is pulled up internally; customers should expect to see VBATT at the output.

Figure 6 illustrates a simple circuit to power on the module using an inverted buffer output.

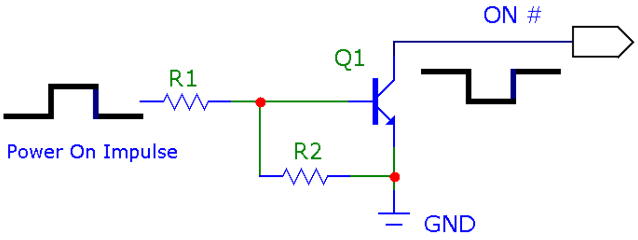


Figure 6: Power-on Circuit; illustrates a simple circuit to power on the module using an inverted buffer output.

Note: Do not use any pull up resistor on the ON_OFF_N line, it is internally pulled up. Using pull up resistor may bring to latch up problems on the LE910R1 power regulator and improper power on/off of the module. The line ON_OFF_N must be connected only in open collector or open drain configuration.

Note: To avoid back powering it is recommended to prevent any HIGH logic level signal from being applied to the digital pins of LE910R1 when the module is powered off or during an ON-OFF transition.

Note:: To check if the device has just powered on, the hardware line PWRMON should be monitored.

After turning on the LE910R1 module, a predefined internal boot sequence performs the HW and SW initialization of the module, which takes some time to complete. During this process, the LE910R1 is not accessible.

As shown in Figure 7, the LE910R1 becomes operational at least 15 seconds after ON_OFF is asserted.

Note: During the Initialization state, AT commands are not available. The DTE host must wait for the Activation state prior to communicating with the LE910R1.

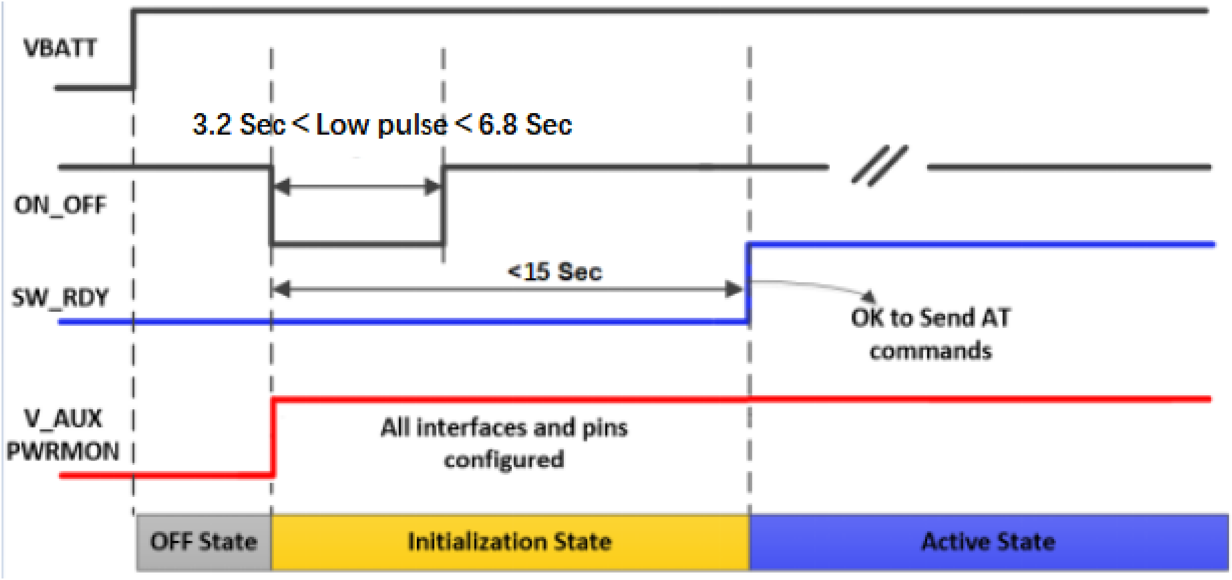


Figure 7: Power ON Sequence

Note: SW_RDY signal is available on GPIO_8 (by default GPIO_8 functions as SW_RDY)

Note: To check whether the LE910R1 is fully operational, monitor the SW_RDY hardware line. When SW_RDY goes high, the module is fully operational and is ready to accept AT commands.

Note: During the SW initialization of the LE910R1, the SW configures all pads and interfaces in the desired status. When PWRMON goes high, this indicates that the initialization of all I/O pads is completed.

Note: Do not use any pull-up resistor on the ON_OFF_N line as it is pulled up internally. Using a pull-up resistor may cause latch-up problems on the LE910R1 power regulator and improper power on/off of the module. The ON_OFF_N line must be connected only in an open-collector configuration

Note: For systems not requiring controlled power ON/OFF, automatic power on can be supported by shorting the ON_OFF signal directly to GND. In this case, the module will start the power on sequence immediately after applying VBATT supply.

Note: Active low signals are labeled with a name that ends with "#" or with "_N"

Note: To avoid back powering it is recommended to prevent any HIGH logic level signal from being applied to the digital pins of LE910R1 when the module is powered off or during an ON-OFF transition.

5.3. Power Off

Turning off the device can be done in the following different ways:

- Shutdown by software using AT#SHDN software command
- Hardware shutdown using ON_OFF_N pad
- Unconditional shutdown using HW_SHUTDOWN_N

When the device is shut down by a software command or a hardware shutdown, it sends a detach disconnection request to the network, informing the network that the device will no longer be reachable.

Note: To check if the device has turned off, monitor the PWRMON hardware line. When PWRMON goes low, this indicates that the device is turned off.

Note: To avoid back powering it is recommended to prevent any HIGH logic level signal from being applied to the digital pins of LE910R1 when the module is powered off or during an ON-OFF transition.

Warning: Not following the recommended shut-down procedures might damage the device and consequently void the warranty.

5.3.1. Shutdown by Software Command

The LE910R1 module can be shut down via a software command.

When a shutdown command is sent, the LE910R1 enters the Finalization state and at the end of the finalization process shuts down PWRMON.

The duration of the Finalization state may vary depending on the current situation of the module, so it is not possible to define a value.

Usually, it will take more than 2 seconds from sending a shutdown command until a complete shutdown is achieved. The DTE host should monitor the PWRMON status to observe the actual power-off.

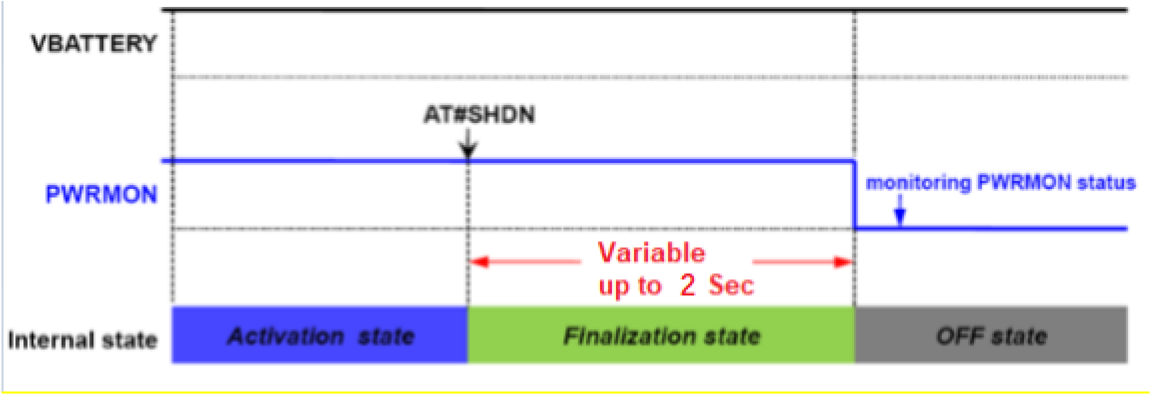


Figure 8: Shutdown by Software Command

Note: To check if the device is turned off, monitor the PWRMON hardware line. When PWRMON goes down, the device has powered off.

5.3.2. Hardware Shutdown

To turn off the LE910R1 module, the ON_OFF_N pad must be asserted low for more than 1.7 seconds and less than 6.8 seconds, and then released. Use the same circuitry and timing for power-on. When the hold time of ON/OFF# is more than 1.7 seconds, the LE910R1 enters the Finalization state and finally shuts down PWRMON .

The duration of the Finalization may vary depending on the current situation of the module, so it is not possible to define a value. Usually, it will take more than 3 seconds issuing a shutdown command until a complete shutdown is achieved. The DTE host should monitor the PWRMON status to observe the actual power-off.

To turn off the LE910R1 module, the ON_OFF_N pad must be asserted low for more than 1.7 seconds and less than 6.8 seconds, and then released.

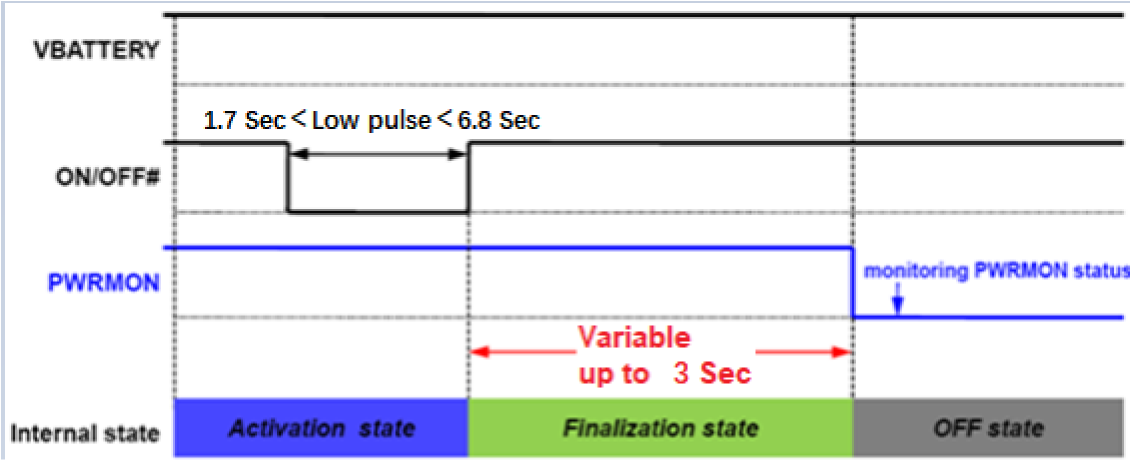


Figure 9: Hardware Shutdown

Note: To check whether the device is turned off, monitor the PWRMON hardware line. When PWRMON goes down, the device has powered off.

5.3.3. Unconditional Shutdown

- To unconditionally shut down the LE910R1 module, the HW_SHUTDOWN_N pad must be tied low for at least 0.6 milliseconds and then released.
- Figure 10 shows a simple circuit for applying an unconditional shutdown.

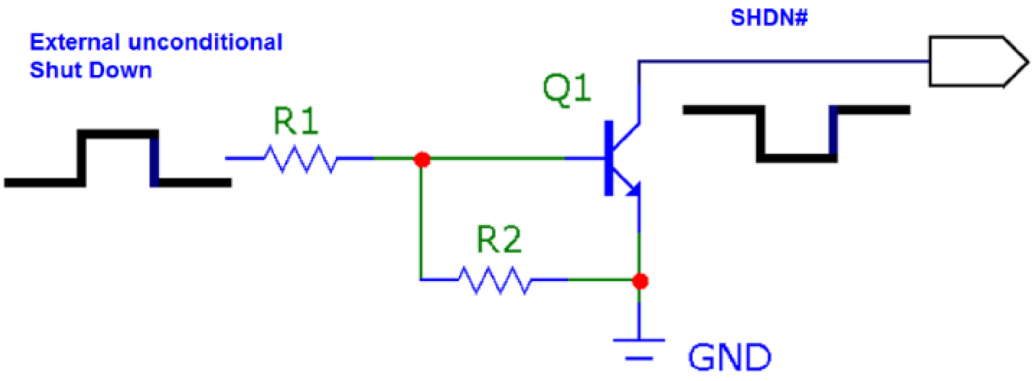


Figure 10: Circuit for Unconditional Hardware Shutdown

Figure 11 shows the system power-down timing when using HW_SHUTDOWN_N.

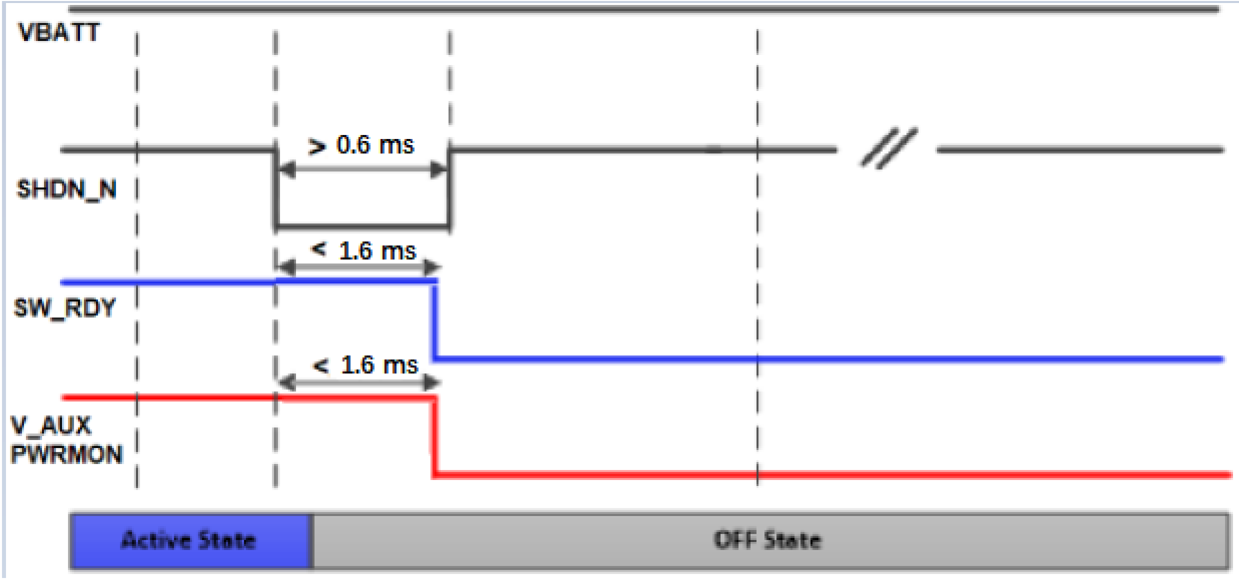


Figure 11: Power down timing using HW_SHUTDOWN_N

Note: Recommended values are as follows: R2 = 47kΩ, R1 = 10kΩ for a 3V signal level.

Note: Do not use any pull-up resistor on the HW_SHUTDOWN_N line or any digital output of the totem pole. Using a pull-up resistor may cause latch-up problems on the LE910R1 power regulator and improper module functioning. The HW_SHUTDOWN_N line must be connected only in an open-collector configuration.

Note: The Unconditional Hardware Shutdown must always be implemented on the boards, but the software must use it only as an emergency exit procedure, and not as a normal power-off operation.

5.4. Communication Ports

5.4.1. USB Port

The LE910R1 module includes a Universal Serial Bus (USB) transceiver, which operates at USB high-speed (480Mbits/sec). It can also operate with USB full-speed hosts (12Mbits/sec).

It is compliant with the USB 2.0 specification and can be used for control and data transfers, as well as for diagnostic monitoring and firmware update.

The USB port is typically the main interface between the LE910R1 module and OEM hardware.

Note: The USB_D+ and USB_D- signals have a clock rate of 480 MHz. The signal traces must be routed carefully. Minimize trace lengths, number of vias, and capacitive loading. The impedance value should be as close as possible to 90 Ohms differential.

Table below lists the USB interface signals.

Signal	Pad No.	Usage
USB_VBUS	A13	Power and cable detection for the internal USB transceiver. Acceptable input voltage range 2.5V – 5.5V @ max 5 mA consumption
USB_D-	C15	Minus (-) line of the differential, bi-directional USB signal to/from the peripheral device
USB_D+	B15	Plus (+) line of the differential, bi-directional USB signal to/from the peripheral device
USB_ID	A14	Not supported, NC internal.
FORCED_USB_BOOT	F14	FORCED_USB_BOOT

Table 20: USB Interface Signals

Note: USB_VBUS input power is used internally to detect the USB port and start the enumeration process.
It is a power supply pin with a maximum consumption of 5 mA.
Do not use pull up or a voltage divider for sourcing this supply

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Note: Even if USB communication is not used, it is still highly recommended to place an optional USB connector on the application board.
At least USB signals test points are required as the USB physical communication is needed in the case of SW update.

5.4.2. Serial Ports

The serial port is typically a secondary interface between the LE910R1 module and OEM hardware. The following serial ports are available on the module:

- Modem Serial Port 1 (Main)
- Modem Serial Port 2 (Auxiliary)
- Modem Serial Port 3(DEBUG_LOG)

Several serial port configurations can be designed for the OEM hardware. The most common are:

- RS232 PC com port
- Microcontroller UART @ 1.8V (Universal Asynchronous Receive Transmit)
- Microcontroller UART @ 3.3V/5V or other voltages different from 1.8V

Depending on the type of serial port on the OEM hardware, level translator circuits may be required to make the system operate. The only configuration that does not require level translation is the 1.8V UART. The LE910R1 UART has CMOS levels as described in Section 5.1, Logic Level Specification.

5.4.2.1. Modem Serial Port 1 Signals

On the LE910R1, Serial Port 1 is a +1.8V UART with 7 RS232 signals. It differs from the PC-RS232 in signal polarity (RS232 is reversed) and levels. Table 23 lists the signals of LE910R1 Serial Port 1.

RS232 Pin#	Signal	Pad No.	Name	Usage
1	DCD - DCD_UART	N14	Data Carrier Detect	Output from LE910R1 that indicates carrier presence
2	RXD - TX_UART	M15	Transmit line *see Note	Output transmit line of LE910R1 UART
3	TXD -RX_UART	N15	Receive line *see Note	Input receive line of LE910R1 UART

RS232 Pin#	Signal	Pad No.	Name	Usage
4	DTR - DTR_UART	M14	Data Terminal Ready	Input to LE910R1 that controls the DTE READY condition
5	GND	A2, B13, D4…	Ground	Ground
6	DSR - DSR_UART	P14	Data Set Ready	Output from LE910R1 that indicates that the module is ready
7	RTS - RTS_UART	L14	Request to Send	Input to LE910R1 controlling the Hardware flow control
8	CTS - CTS_UART	P15	Clear to Send	Output from LE910R1 controlling the Hardware flow control
9	RI - RI_UART	R14	Ring Indicator	Output from LE910R1 indicating the Incoming call condition

Table 21: Modem Serial Port 1 Signals

Note: To avoid back powering it is recommended to prevent any HIGH logic level signal from being applied to the digital pins of LE910R1 when the module is powered off or during an ON-OFF transition.

Note: For minimum implementations, only the TXD, RXD lines need to be connected to the host, but RTS must be either grounded or connected directly to CTS. The other lines can be left open provided a software flow control is implemented.

Note: According to V.24, Rx/Tx signal names refer to the application side; therefore, on the LE910R1 side, these signal are in the opposite direction: TXD from the application side will be connected to the reception line (here named TXD/ RX_UART) of the LE910R1 serial port and vice versa for Rx.

Note: The DTR pin is used to control the UART and system sleep Pulling the DTR pin down prevents the UART and the entire module from entering low power mode. DTR can be left floating if not used (DTR is internally pulled high).

5.4.2.2. Modem Serial Port 2

On the LE910R1, Serial Port 2 is a +1.8V UART with Rx and Tx signals only.

PAD	Signal	I/O	Function	Type	Comment
D15	TXD_AUX	O	Auxiliary UART (Tx Data to DTE)	1.8V	
E15	RXD_AUX	I	Auxiliary UART (Rx Data to DTE)	1.8V	

Table 22: Modem Serial Port 2 Signals

Note: To avoid back powering it is recommended to prevent any HIGH logic level signal applied to the digital pins of the module when it is powered OFF or during an ON/OFF transition.

5.4.2.3. Modem Serial Port 3

PAD	Signal	I/O	Function	Type	Comment
K4	DEBUG_UART_TXD	O	LOG_UART_TXD	1.8V	
M6	DEBUG_UART_RXD	I	LOG_UART_RXD	1.8V	

Table 23: Modem Serial Port 3

Note: The DEBUG_UART is used as the SW main debug console. Test points must be placed on this interface even if not used.

5.4.2.4. RS232 Level Translation

To interface the LE910R1 with a PC COM port or an RS232 (EIA/TIA-232) application, a level translator is required. This level translator must perform the following actions:

- Invert the electrical signal in both directions
- Change the level from 0/1.8V to +15/-15V

The RS232 UART 16450, 16550, 16650 & 16750 chipsets accept signals with lower levels on the RS232 side (EIA/TIA-562), allowing for a lower voltage-multiplying ratio on the level translator. Note that the negative signal voltage must be less than 0V and therefore some sort of level translation is always required.

The easiest way to translate the levels and invert the signal is by using a single chip-level translator. There are a multitude of them, which differ in the number of drivers and receivers and in the levels (be sure to get a real RS232 level translator, not a RS485 or other standards).

By convention, the driver is the level translator from the 0-1.8V UART to the RS232 level. The receiver is the translator from the RS232 level to 0-1.8V UART. To translate the whole set of control lines of the UART, the following is required:

- 2 drivers
- 2 receivers

Warning: The digital input lines, operating at 1.8V CMOS levels, have absolute maximum input voltage of 2.2V. The level translator IC outputs on the module side (i.e. LE910R1 inputs) will cause damage to the module inputs if the level translator is powered with +3.8V power. Therefore, the level translator IC must be powered from a dedicated +1.8V power supply.

As an example, RS232 level adaption circuitry could use a MAXIM transceiver (MAX218). In this case, the chipset is able to translate directly from 1.8V to the RS232 levels (example on 4 signals only).

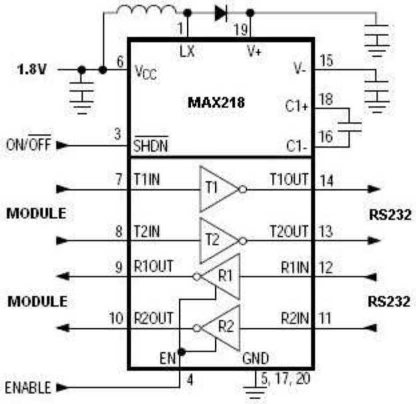

Figure 12: RS232 Level Adaption Circuitry Example

Note: In this case, it is necessary to take into account the length of the lines on the application to avoid problems in the case of high-speed rates on RS232.

The RS232 serial port lines are usually connected to a DB9 connector as shown in the figure below. Signal names and directions are named and defined from the DTE perspective.

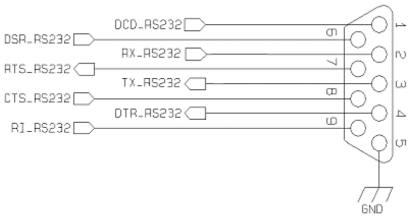

Figure 13: RS232 Serial Port Lines Connection Layout

5.4.3. I2C - Inter-integrated Circuit

The LE910R1 supports I2C interface on the following pins:

- B14 - I2C 3_SCL
- C12 - I2C 3_SDA

The I2C can also be used externally by the end customer application. LE910R1 supports I2C Master Mode only.

5.4.4. General Purpose I/O

The general-purpose I/O pads can be configured to act in three different ways:

- Input
- Output
- Alternative function (internally controlled)

Input pads can only be read, reporting digital values (high / low) present on the pad at the time of reading. Output pads can only be written or queried and set values on the pad output. Alternative function pads can be controlled internally by LE910R1 firmware and act according to the implementation.

The following GPIOs are always available as a primary function on the LE910R1.

PAD	Signal	I/O	Function	Type	Note
C8	GPIO_1	I/O	Configurable GPIO	CMOS 1.8V	
C9	GPIO_2	I/O	Configurable GPIO	CMOS 1.8V	
C10	GPIO_3	I/O	Configurable GPIO	CMOS 1.8V	Can be used to I2C2_SCL
C11	GPIO_4	I/O	Configurable GPIO	CMOS 1.8V	Can be used to I2C2_SDA
B14	GPIO_5	I/O	Configurable GPIO	CMOS 1.8V	Can be used to I2C3_SCL

PAD	Signal	I/O	Function	Type	Note
C12	GPIO_6	I/O	Configurable GPIO	CMOS 1.8V	Can be used to I2C3_SDA
C13	GPIO_7	I/O	Configurable GPIO	CMOS 1.8V	
K15	GPIO_8	I/O	Configurable GPIO	CMOS 1.8V	
L15	GPIO_9	I/O	Configurable GPIO	CMOS 1.8V	
G15	GPIO_10	I/O	Configurable GPIO	CMOS 1.8V	

Table 24: Primary GPIOs

5.4.5. Using a GPIO Pad as Input

GPIO pads, when used as inputs, can be connected to a digital output of another device and report its status, provided this device has interface levels compatible with the 1.8V CMOS levels of the GPIO. If the digital output of the device is connected to the GPIO input, the pad has interface levels other than 1.8V CMOS. It can be buffered with an open collector transistor with a 10 kΩ pull-up resistor to 1.8V.

5.4.6. Using a GPIO Pad as an Interrupt / Wakeup Source

GPIO pads that are used as input can also be used as an interrupt source for the software. In general, all GPIO pads can also be used as interrupts. However, not all GPIO's can be used as a wakeup source of the module (wakeup from sleep).

Only the following GPIO's can be used to wake up the system from sleep:

- GPIO_2
- GPIO_7
- GPIO_9
- GPIO_10

5.4.7. Using a GPIO Pad as Output

GPIO pads, when used as outputs, can drive 1.8V CMOS digital devices or compatible hardware. When set as outputs, the pads have a push-pull output, and therefore the pull-up resistor can be omitted.

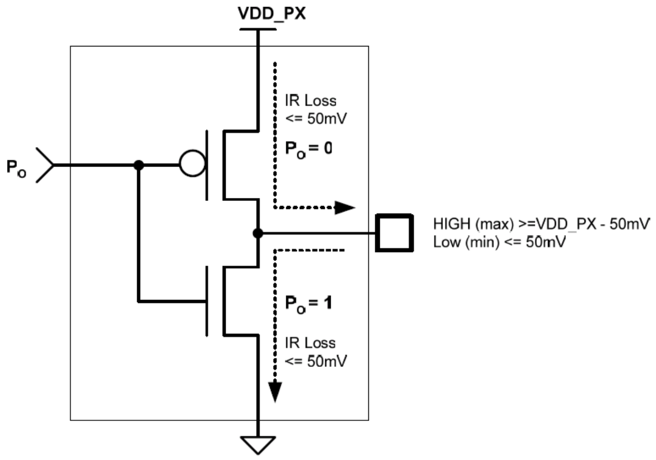

Figure 14: GPIO Output Pad Equivalent Circuit

5.5. Indication of Network Service Availability

The STAT_LED pin status shows information on the network service availability and call status. In the LE910R1 module, the STAT_LED usually needs an external transistor to drive an external LED. The STAT_LED does not have a dedicated pin. The STAT_LED functionality is available on GPIO_1 pin (by default GPIO_1 functions as STAT_LED)

See the AT Command User Guide for details on the AT#SLED section.

LED Status		Device Status
Permanently off		Device off
Blinking	Blinking 1s on and 2s off	Registered in idle
	Blinking time depends on network condition in order to minimize power consumption	Registered in idle with power saving
Permanently on		Not registered

Table 25: Network Service Availability Indication

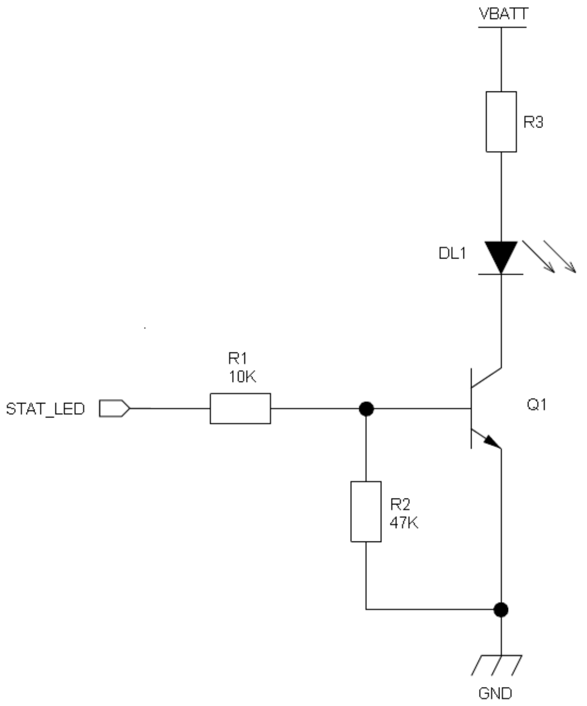

Figure 15: Status LED Circuit Example

5.6. Indication of Software Ready

The SW_RDY signal provides indication about the module' ability to receive commands. As long as the SW_RDY is asserted low, it indicates that the LE910R1 has not finished booting yet. Once the SW_RDY is asserted high, it indicates that the LE910R1 is ready to receive commands.

The SW_RDY does not have a dedicated pin. The SW_RDY functionality is available on GPIO_8 pin (by default GPIO_8 functions as SW_RDY).

5.7. External SIM Holder

This section presents the recommended schematics for the design of SIM interfaces on the application boards. The LE910R1 supports two external SIM interfaces.

5.7.1. SIM Schematic Example

Figure 16 shows in particular how to design the application side and what values to assign to the components.

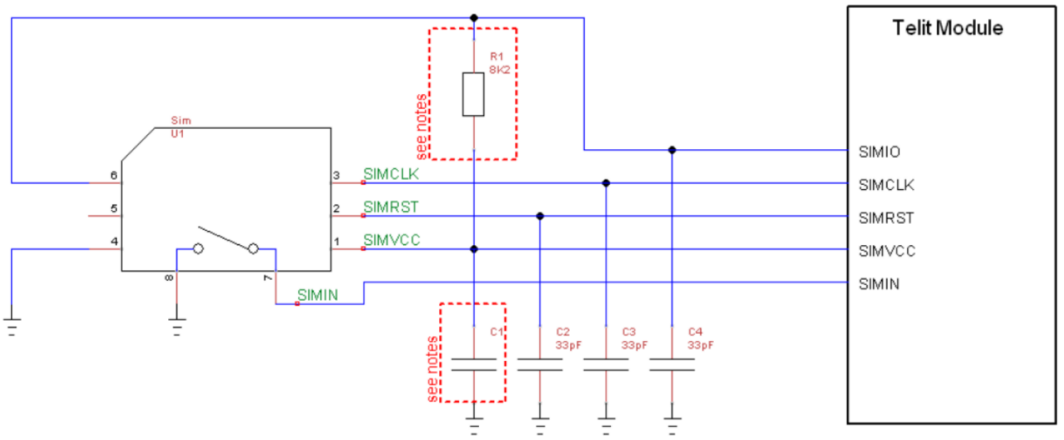

Figure 16: SIM Schematics

Note: The resistor value on SIMIO pulled up to SIMVCC must be defined to comply with the 3GPP specification for USIM electrical testing. The LE910R1 module contains an internal pull-up resistor of 4.7K Ω on SIMIO.

However, the un-mounted R1 option in the application can be used to tune SIMIO timing if required.

Table 26 lists the values of C1 to be adopted with the LE910R1 product:

Product P/N	C1 Range (nF)
LE910R1	1µF+0.1µF

Table 26: SIM Interface – C1 Range

5.8. ADC Converter

5.8.1. Description

The LE910R1 module provides two on-board Analog to Digital converters. Each ADC reads the voltage level applied to the relevant pin, the accuracy is about 20mv@1.8v.

Item	Min	Max	Units
Input voltage range	-0.3	1.8V	Volt
Accuracy	-	20mV	mV

Table 27: ADC Parameters

5.8.2. Using the ADC Converter

An AT command is available to use the ADC function.

The command is AT#ADC=1,2. The read value is expressed in mV.

Refer to Ref.1: LE910R1 AT Command User Guide for the full description of this function.

5.9. Debug of the LE910R1 Module in Production

To test and debug the mounting of the LE910R1 module, it is highly recommended to add several test pads on the application board design for the following purposes:

- Check the connection between the LE910R1 itself and the application
- Test the performance of the module by connecting it with an external computer

Depending on the customer's application, these test pads include, but are not limited to the following signals:

- TXD
- RXD
- ON/OFF
- HW_SHUTDOWN_N
- GND
- VBATT
- DEBUG_UART_TXD
- DEBUG_UART_RXD
- USB_VBUS
- USB_D+
- USB_D-
- FORCED_USB_BOOT

In addition, the following signals are also recommended (but not mandatory:

- SW_RDY
- PWRMON
- GPIO_1 (STAT_LED)
- GPIO_8 (SW_RDY)

6. RF SECTION

6.1. Bands Variants

Table below summarizes all region variants within the LE910R1 family, showing the band sets supported in each variant.

Different bands combinations are available:

Region Variant	2G	LTE FDD
LE910R1-EU	B3 (1800), B8 (900)	B1, B3, B7, B8, B20, B28
LE910R1-BR	B2 (1900), B3 (1800), B5 (850), B8 (900)	B1, B3, B5, B7, B8, B28

Table 28: RF Bands Variant

Mode	Freq. Tx (MHz)	Freq. Rx (MHz)	Channels	Tx-Rx Offset
PCS 1900	1850.2 ~ 1909.8	1930.2 ~ 1989.8	512 ~ 810	80 MHz
DCS 1800	1710 ~ 1785	1805 ~ 1880	512 ~ 885	95 MHz
GSM 850	824.2 ~ 848.8	869.2 ~ 893.8	128 ~ 251	45 MHz
EGSM 900	890 ~ 915	935 ~ 960	0 ~ 124	45 MHz
	880 ~ 890	925 ~ 935	975 ~ 1023	45 MHz
LTE 2100 – B1	1920 ~ 1980	2110 ~ 2170	Tx: 18000 ~ 18599 Rx: 0 ~ 599	190 MHz
LTE 1800 – B3	1710 ~ 1785	1805 ~ 1880	Tx: 19200 ~ 19949 Rx: 1200 ~ 1949	95 MHz
LTE 850 – B5	824 ~ 849	869 ~ 894	Tx: 20400 ~ 20649 Rx: 2400 ~ 2649	45 MHz
LTE 2600 – B7	2500 – 2570	2620 – 2690	Tx: 20750 ~ 21449 Rx: 2750~ 3449	120 MHz
LTE 900 – B8	880 ~ 915	925 ~ 960	Tx: 21450 ~ 21799 Rx: 3450 ~ 3799	45 MHz
LTE 800 – B20	832 ~ 862	791 ~ 821	Tx: 24150 ~ 24449 Rx: 6150 ~ 6449	-41 MHz
LTE 700 – B28A	703 ~ 733	758 ~ 788	Tx: 27210 ~ 27510 Rx: 9210 ~ 9510	55 MHz
LTE 700 – B28B	703 ~ 748	758 ~ 803	Tx: 27210 ~ 27659 Rx: 9210 ~ 9659	55 MHz

Table 29: Bandwidth

6.2. TX Output Power

Typical values for Max output level are as follow:

Band	Power class
2G EGSM 900 , 2G EGSM 850	Class 4 (2W)
2G DCS 1800, PCS 1900	Class 1 (1W)
4G LTE (FDD TDD) All Bands	Class 3 (0.2W)

Table 30: Transmission Output Power

Band	Mode	Class	RF power (dBm)
B8 900, B5 850	2G GSM/GPRS	4	33dBm +/- 1dB
	2G EGPRS	E2	27dBm +/- 1dB
B3 1800, B2 1900	2G GSM/GPRS	1	30dBm +/- 1dB
	2G EGPRS	E2	26dBm +/- 1dB
B1, B3, B5, B7, B8, B20, B28A, B28B	4G LTE FDD -CAT1	3	23dBm +/- 1dB

Table 31: Transmission Output Power

6.3. RX Sensitivity

Below the 3GPP measurement conditions used to define the RX sensitity:

Technology	3GPP Compliance
2G GSM/GPRS	BER Class II <2.44%
4G LTE	Throughput >95% 10MHz

Table 32: Reception Sensitivity

Mode	Sensitivity	3GPP
DCS 1800 - B3	-107.5	-102
EGSM 900 – B8	-109	-102
PCS 1900 – B2	-107.5	-102
EGSM 850 – B5	-109	-102
LTE 2100 – B1	-99.0	-96.3
LTE 1800 – B3	-97.5	-93.3
LTE 850 – B5	-99.5	-94.3
LTE 2600 – B7	-97.5	-94.3
LTE 900 – B8	-99	-93.3

Mode	Sensitivity	3GPP
LTE 800 – B20	-99.5	-93.3
LTE 700 – B28A/B	-99	-94.8

Table 33: Typical Sensitivity Levels

Note: The sensitivity level may present a deviation of approximately +/- 2dB depending on model, device and channel; the level shown is the typical value.

6.4. Antenna Requirements

The antenna connection and board layout design are the most important aspect in the full product design as they strongly affect the general performance of the product, so read carefully and follow the requirements and the guidelines for a proper design.

The antenna and antenna transmission line on PCB for a Telit LE910R1 device shall fulfil the following requirements:

Item	Value
Frequency range	Depending by frequency band(s) provided by the network operator, the customer shall use the most suitable antenna for that/those band(s)
Bandwidth	See table 33: Bandwidth
Impedance	50 ohm
Input power	GSM: > 33dBm Average power LTE: > 24dBm Average power
VSWR absolute max	≤ 10:1 (limit to avoid permanent damage)
VSWR recommended	≤ 2:1 (limit to fulfill all regulatory requirements)

Table 34: Antenna and Antenna transmission line on PCB

6.5. Antenna Tuner

The ME910G1 includes a feature to enable an external antenna tuning solution. This enables to dynamically tune the antenna on multiple frequencies.

Refer to AT command AT#ATUNERSEL (AT Commands Reference Guide-Telit code 80617ST10991A) to select GPIO or MIPI interfaces on ATC1 (pin K3) and ATC2 (pin L3) pins.

6.5.1. GPIO

ATC1 Pin	ATC2 Pin	Band (Uplink)	Freq. Range [MHz]
0	0	B1, B3, B7 GSM1800, GSM1900	1710-2690
0	1	B8, EGSM900	880-960
1	0	B5, B20, GSM850	791-894
1	1	B28A, B28	698-803

Table 35 Antenna Tuner GPIO table

6.6. PCB Design Guidelines

When using the LE910R1, since there's no antenna connector on the module, the antenna must be connected to the LE910R1 antenna pad (K1) by means of a transmission line implemented on the PCB.

This transmission line shall fulfil the following requirements:

Item	Value
Characteristic Impedance	50 ohm (+-10%)
Max Attenuation	0.3 dB
Coupling	Coupling with other signals shall be avoided
Ground Plane	Cold End (Ground Plane) of antenna shall be equipotential to the LE910R1 ground pins

Table 36: Antenna Pad Requirements

The transmission line should be designed according to the following guidelines:

- make sure that the transmission line’s characteristic impedance is 50 ohm;
- keep the antenna waveguide on the PCB as short as possible, since the antenna line loss shall be less than about 0,3 dB;
- the geometry of the line must have uniform characteristics, constant cross section, avoid meanders and abrupt curves;
- any kind of suitable geometry / structure (Microstrip, Stripline, Coplanar, Grounded Coplanar Waveguide...) can be used to implement the printed transmission line relating to the antenna;

- if a Ground plane is required in the geometry of the line, this plane must be continuous and sufficiently extended, so that the geometry can be as similar as possible to the related canonical model;
- keep, if possible, at least one layer of the PCB used only for the Ground plane; If possible, use this layer as reference Ground plane for the transmission line;
- it is advisable to surround (on both sides) the PCB transmission line with Ground, avoiding that other signal tracks face directly the antenna line track;
- avoid crossing any un-shielded transmission line footprint with other signal tracks on different layers;
- the ground surrounding the antenna line on the PCB must be tightly connected to the main Ground Plane through holes (at east once every 2mm), placed near the edges of the ground facing the line track;
- place EM noisy devices as far as possible from LE910R1 antenna line;
- keep the antenna line far away from the LE910R1 power supply lines;
- if EM noisy devices (such as fast switching ICs, LCD and so on) are present on the PCB hosting the LE910R1, take care of the shielding of the antenna line by burying it in an inner layer of PCB and surrounding it with the Ground planes, or shield it with a metal frame cover;
- if EM noisy devices are not present around the line, the use of geometries such as Microstrip or Grounded Coplanar Waveguide is preferable, since they typically ensure less attenuation if compared to a Stripline of the same length.

The following image shows the suggested layout for the Antenna pad connection:

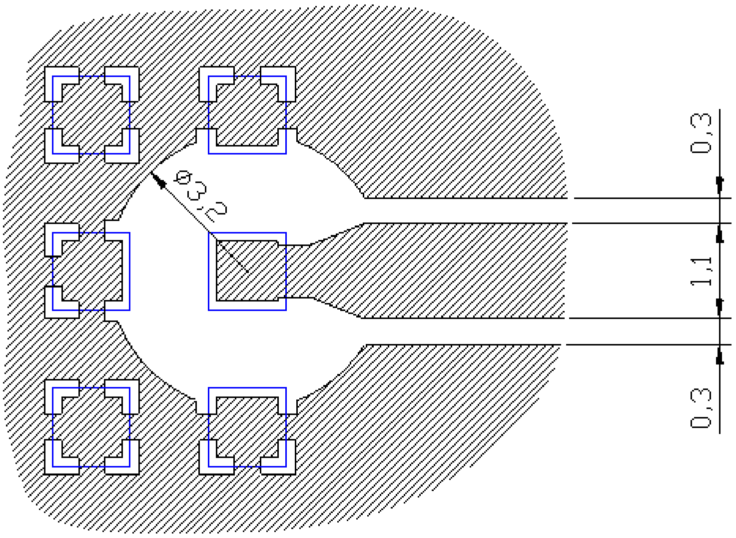

Figure 17: Layout for the Antenna pad connection

6.6.1.1. Transmission Line Design

When designing the LE910R1 interface board, the placement of components was chosen properly, in order to keep the length of the line as short as possible, thus leading to the lowest possible power losses. A Grounded Coplanar Waveguide (G-CPW) line has been chosen, since this kind of transmission line ensures good impedance control and can be implemented in an outer PCB layer as needed in this case. A SMA female connector has been used to feed the line.

The interface board is made on a FR4, 4-layers PCB. The substrate material is characterized by relative permittivity εr = 4.6 ± 0.4 @ 1 GHz, TanD= 0.019 ÷ 0.026 @ 1 GHz.

A characteristic impedance of nearly 50 Ω is achieved using a track width = 1.1 mm, clearance from a coplanar ground plane = 0.3 mm each side.

The line uses the reference ground plane on layer 3, while copper is removed from layer 2 below the line. The height of the trace above ground plane is 1.335 mm. The calculated characteristic impedance is 51.6 Ω, the estimated line loss is less than 0.1 dB.

The line geometry is shown below:

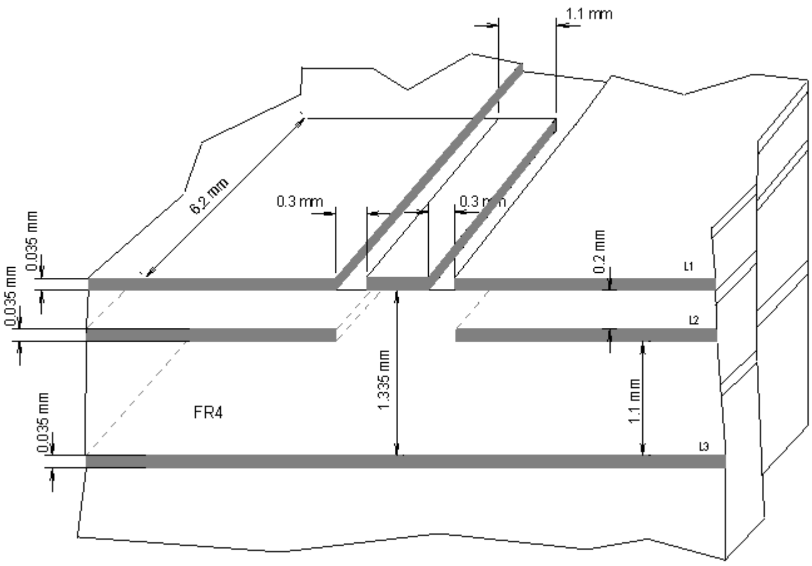

Figure 18: Line Geometry

6.6.1.2. Transmission Line Measurements

An HP8753E VNA (Full-2-port calibration) was used in this measurement session.

A calibrated coaxial cable was soldered to the pad corresponding to RF output; a SMA connector was soldered to the board in order to characterize the losses of the transmission line including the connector itself. During Return Loss / impedance measurements, the transmission line has been terminated to 50 Ω load.

Return Loss plot of line under test is shown below:

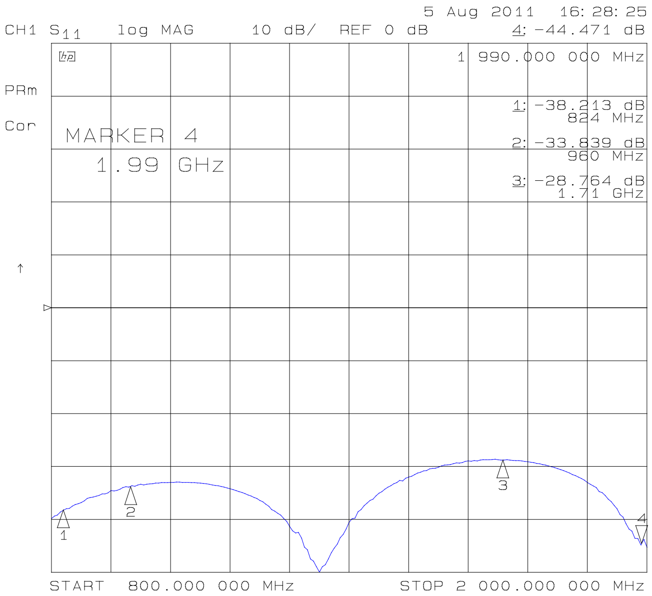

Figure 19: Return Loss plot of line under test

The input impedance of the line (in Smith Chart format, once the line has been terminated to 50 Ω load) is shown in the following figure:

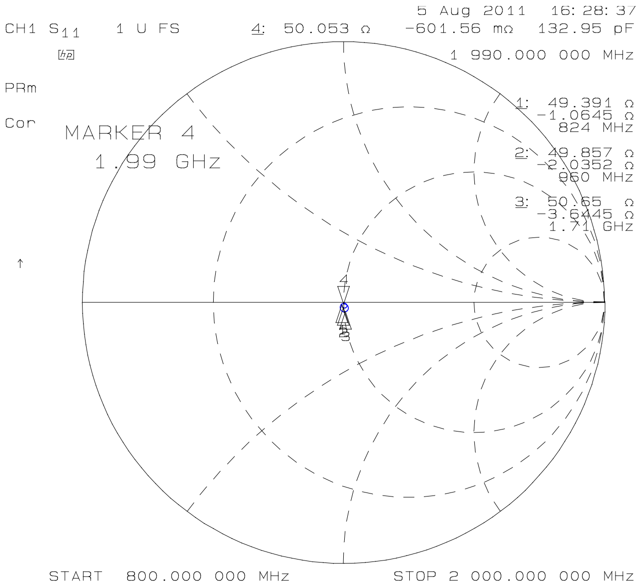

Figure 20: Line input impedance

Insertion Loss of G-CPW line plus SMA connector is shown below:

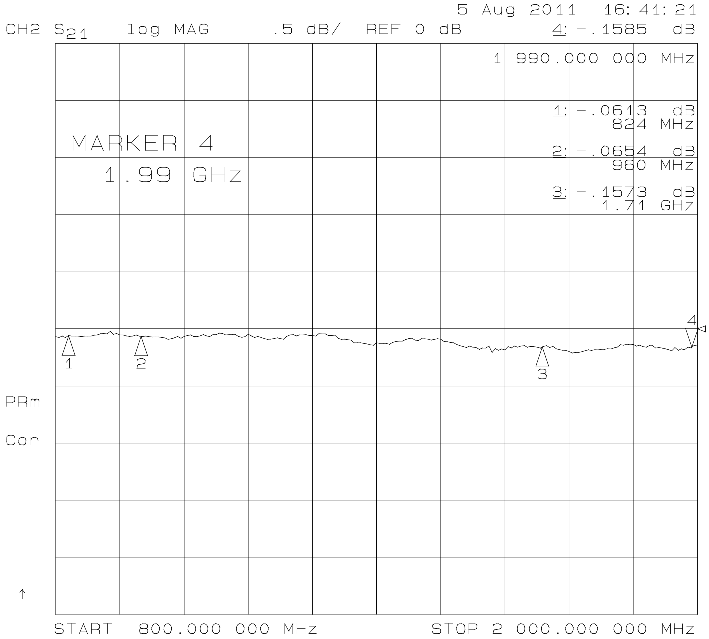

Figure 21: Insertion Loss of G-CPW line plus SMA connector

6.6.1.3. Antenna Installation Guidelines

- Install the antenna in a place covered by the LTE signal.
- The Antenna must not be installed inside metal cases.
- The Antenna must be installed according Antenna manufacturer instructions.
- The Antenna integration should optimize the Radiation Efficiency. Efficiency values > 50% are recommended on all frequency bands.
- The Antenna integration should not perturb the radiation pattern described in the documentation of the Antenna manufacturer.
- It is preferable to get an omnidirectional radiation pattern.
- The Antenna Gain must not exceed the values indicated in regulatory requirements, where applicable, in order to meet the related EIRP limitations. The Typical antenna Gain in most M2M applications does not exceed 2.1dBi.

7. AUDIO SECTION

7.1. Analog Front-End

7.1.1. MIC Connection

The bias for the microphone should be as clean as possible; the first connection (single ended) is preferable since the Vmic noise and the background noise are input as common mode and therefore rejected. This sounds strange; usually the connection to be used to reject the common mode is the balanced one. In this situation we must remember that the microphone is a sound to current transducer, therefore the resistor is the current to tension transducer, so finally the resistor feeds the input in a balanced way even if the configuration, from the microphone point of view, seems to be un-balanced.

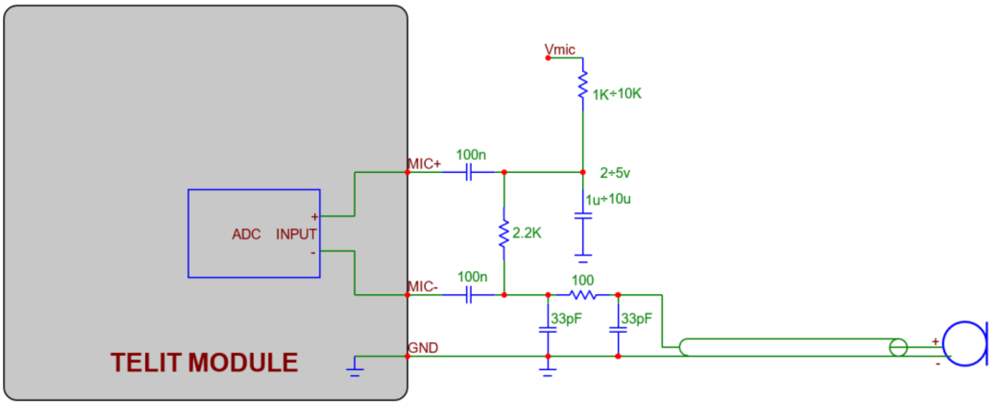

Figure 22: MIC Connection single ended

However, if a "balanced way" is desired, much more care must be paid to Vmic noise and background noise; also the 33pF-100Ohm-33pF Π-RF filter must be doubled (one each wire).

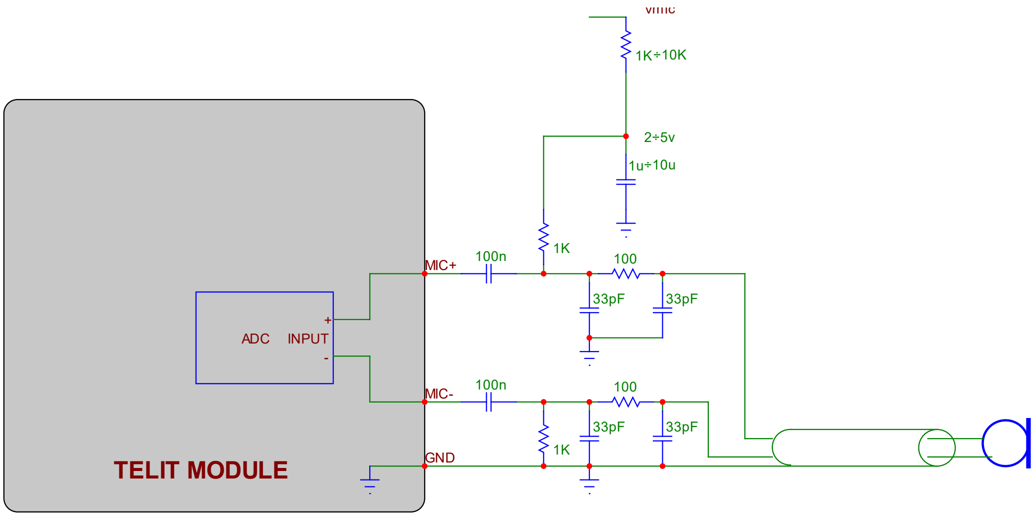

Figure 23: MIC Connection balanced

Tip: Since the J-FET transistor inside the microphone acts as RF detector amplifier, ask your supplier for a microphone with anti-EMI capacitor (usually a 33pF or a 10pF capacitor placed across the output terminals inside the case).

7.1.2. EAR Connection

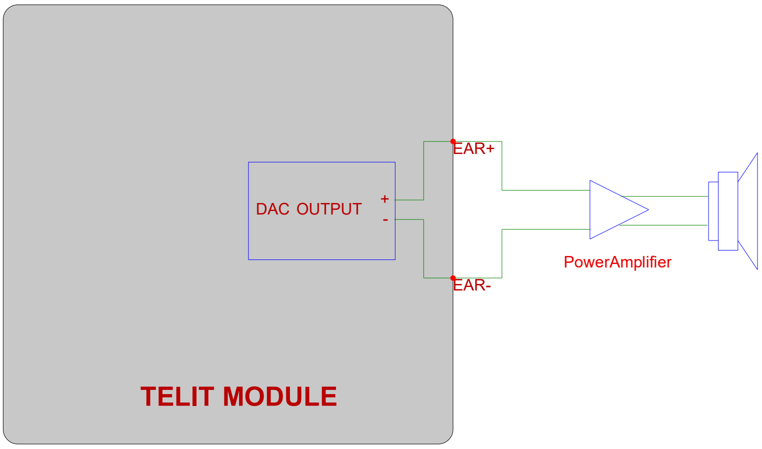

Figure 24: EAR Connection

The audio output of the LE910R1 is balanced, this is helpful to double the level and to reject common mode (click and pop are common modes and therefore rejected); The power of the analog output is 37mW, it's too low to directly manage a loudspeaker with electrical impedance of at least 8Ohm ,so an external amplifier is needed. The circuit of the an external amplifier need to be designed according the datasheet of the external amplifier.

Tip: to obtain the maximum audio level at a given output voltage level (dBspl/Vrms), the following breaking through procedure can be used. Have the loudspeaker as close as you can to the listener (this also simplify the echo cancelling); choose the loudspeaker with the highest sensitivity (dBspl per W); choose loudspeakers with the impedance close to the limit (ex: 16 or 8 Ohm).

8. MECHANICAL DESIGN

8.1. General

The LE910R1 module is designed comply with a standard lead-free soldering process.

8.2. Finishing & Dimensions

The below figure shows the mechanical dimensions of the LE910R1 module.

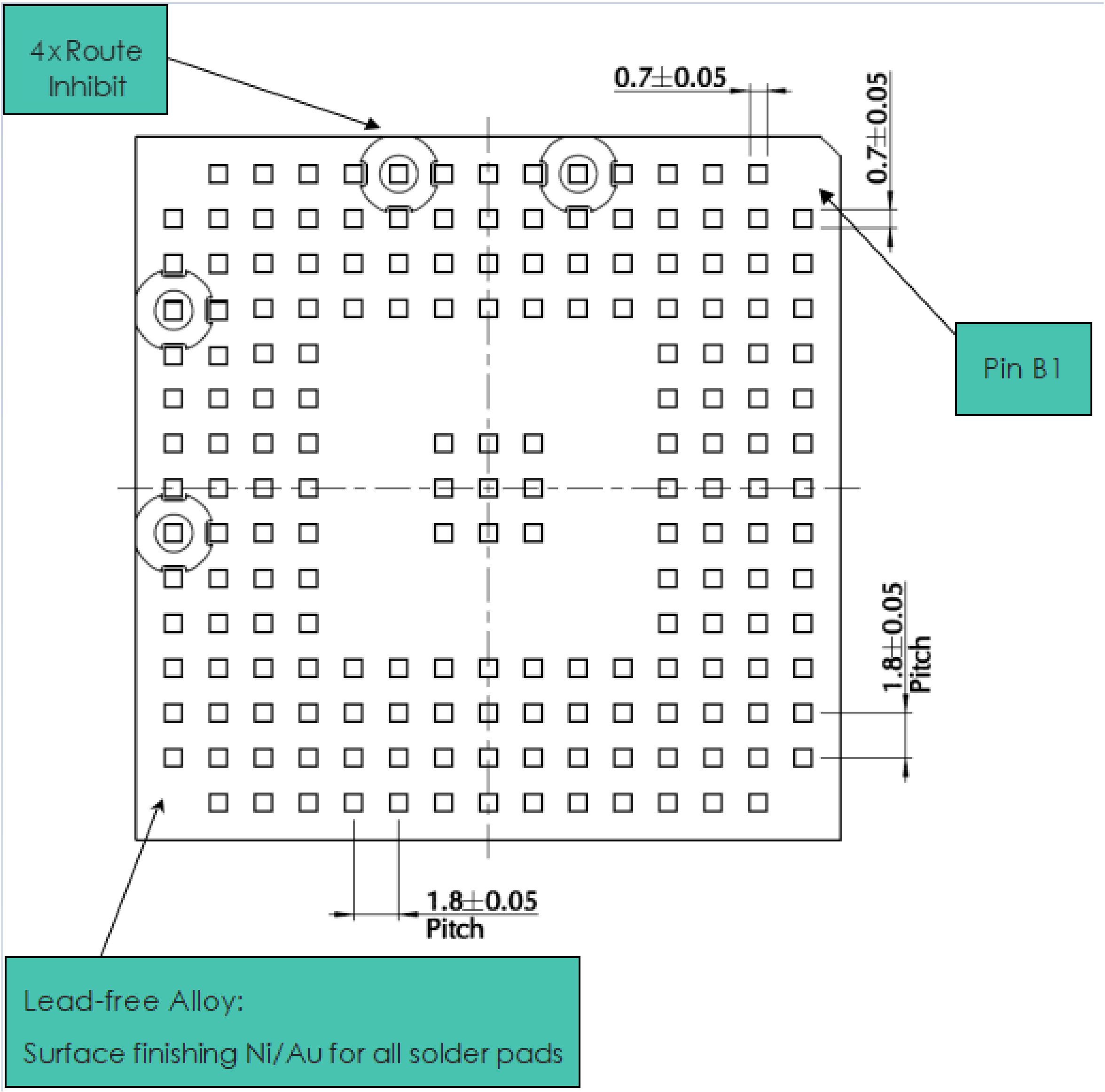

Figure 25: LE910R1 Mechanical Dimensions (Bottom View)

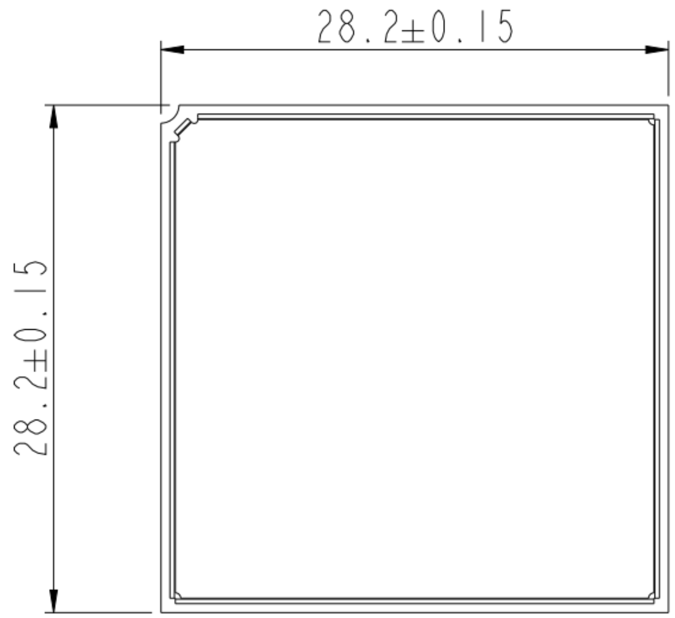

Figure 26: LE910R1 Mechanical Dimensions (Top view)

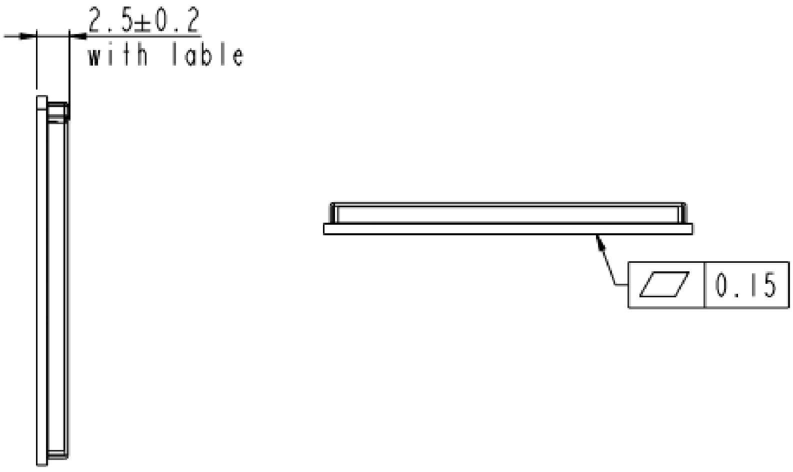

Figure 27: LE910R1 Mechanical Dimensions (Side view)

9. APPLICATION PCB DESIGN

The LE910S modules have been designed in order to be compliant with a standard lead-free SMT process

9.1. Recommended Footprint for the Application

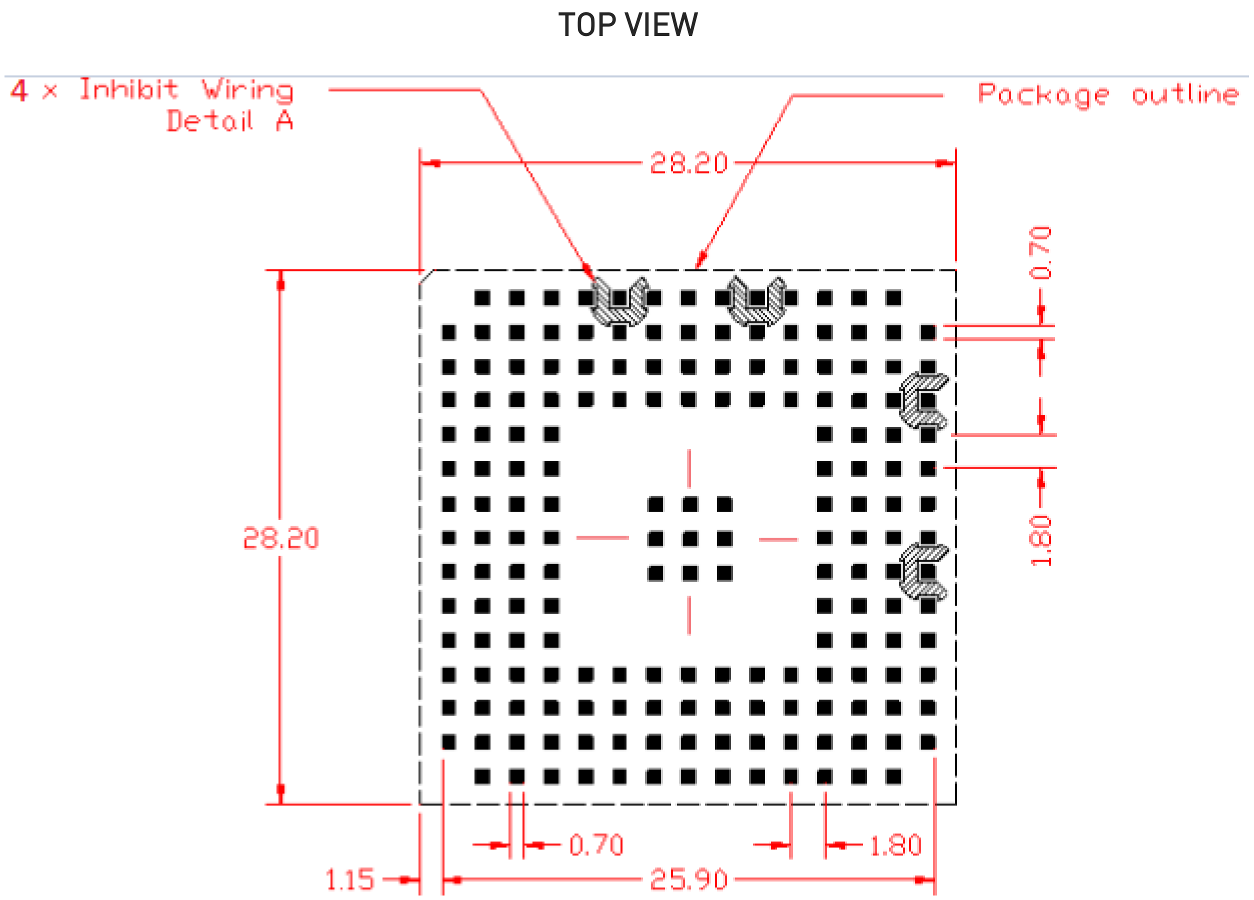

Figure 28: Footprint

SOLDER RESIST PATTERN (dimensions in mm)

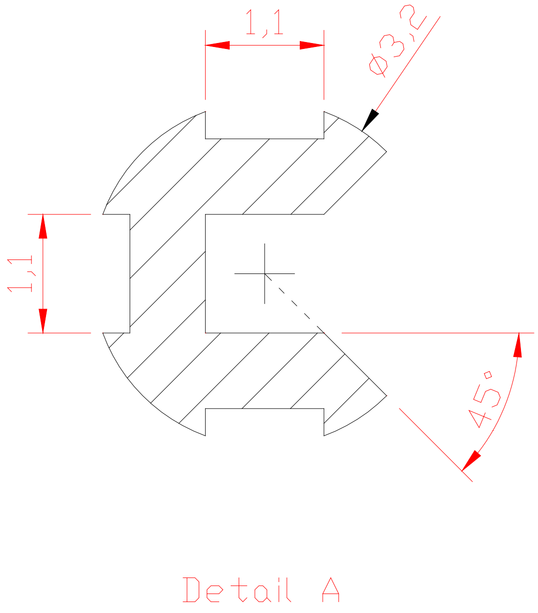

Figure 29:: Solder resist pattern

TOP TRANSPARENT VIEW

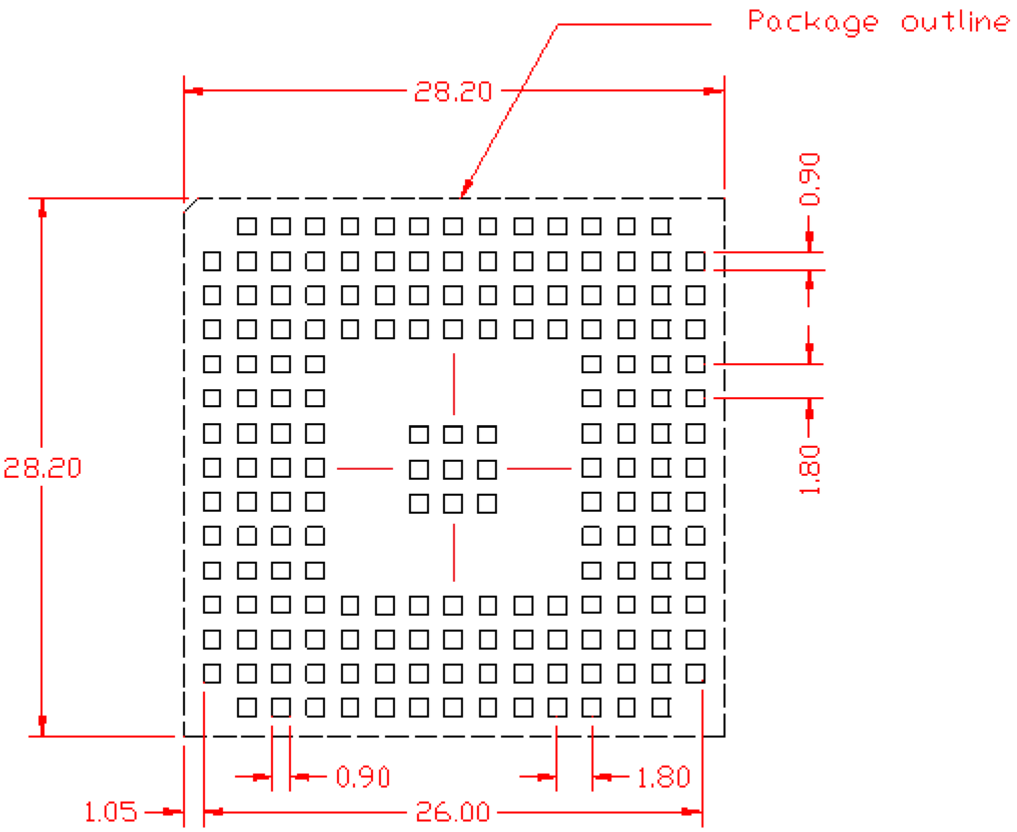

Figure 30: Top transparent view

In order to easily rework the LE910R1 it is recommended to consider on the application a 1.5 mm placement inhibit area around the module.

It is also suggested, as common rule for an SMT component, to avoid having a mechanical part of the application in direct contact with the module.

Note: In the customer application, the region under WIRING INHIBIT (see figure above) must be clear from signal or ground paths.

9.2. PCB Pad Design

In PCB design, the solder pads can be defined as either Solder Mask Defined (SMD) or Non-Solder Mask Defined (NSMD). The difference between these two solder mask pad definitions, is in the closeness of the solder mask to the metal pad. In SMD pads, the solder mask opening is smaller than the metal pad and overlaps the metal on all sides. The solder mask opening defines the solderable area of the pad. In NSMD pads, the solder mask opening is larger than the metal pad and does not overlap the metal. The metal edge defines the solderable area of the pad (see Figure below).

Since the metal etching process in PCB manufacture, has significantly tighter alignment and etching tolerances than the alignment registration of the solder masking process, which, a more accurate solder pad land pattern can be obtained with NSMD pads. In addition, with SMD pads, the solder mask that overlaps the metal pad introduces additional height above the metal surface that may affect solder joint adhesion and reliability. Non solder mask defined (NSMD) type is recommended for the solder pads on the PCB.

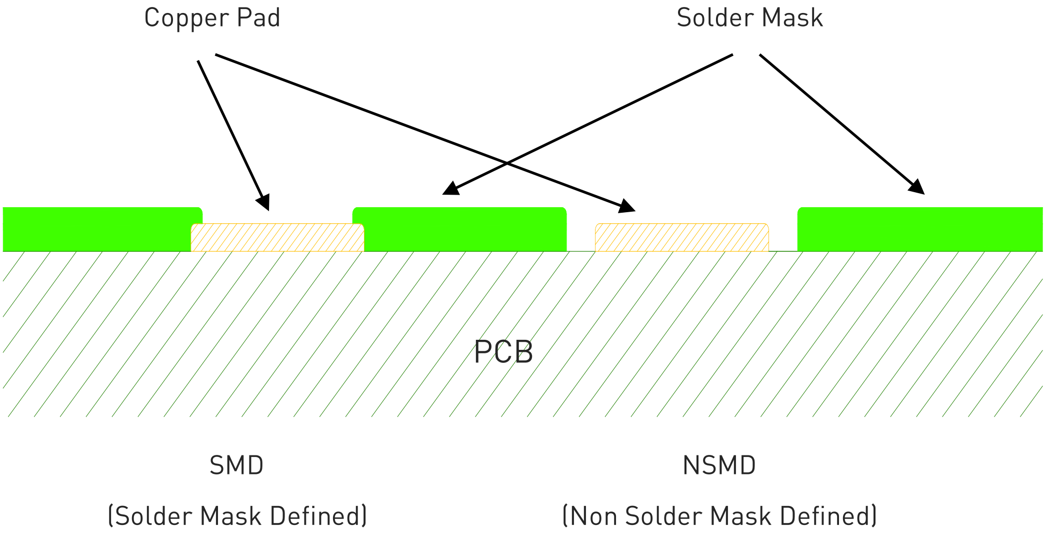

Figure 31: PCB solder pad recommendations

9.3. Reccomendations for PCB Pad Dimensions

It is not recommended to place via or micro-via not covered by solder resist in an area of 0,3 mm around the pads unless it carries the same signal of the pad itself

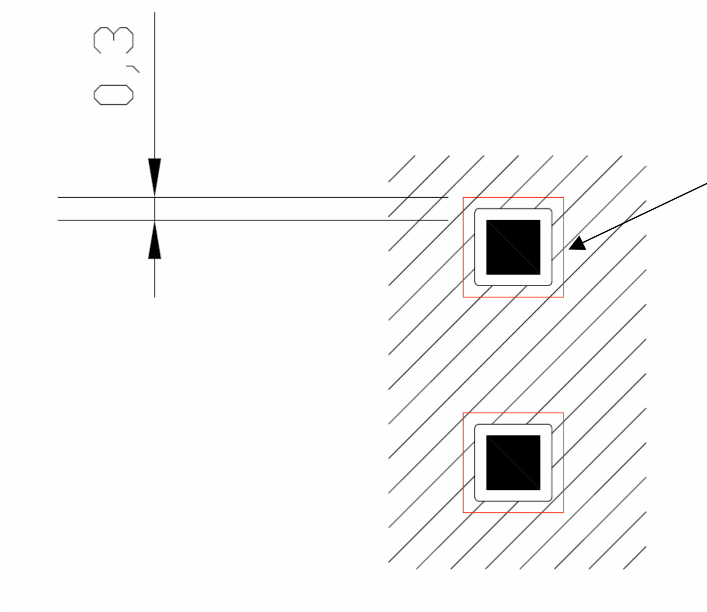

Figure 32: Pad dimensions recommendations

Holes in pad are allowed only for blind holes and not for through holes.

Recommendations for PCB pad surfaces:

Finish	Layer Thickness (um)	Properties
Electro-less Ni / Immersion Au	3 –7 / 0.05 – 0.15	good solder ability protection, high shear force values

Table 37: Recommendations for PCB pad surfaces

The PCB must be able to resist the higher temperatures which are occurring during the lead-free process. This issue should be discussed with the PCB-supplier. Generally, the wettability of tin-lead solder paste on the described surface plating is better than compared to the lead-free solder paste.

It is not necessary to panel the application's PCB, however in that case it is recommended to use milled contours and predrilled board breakouts; scoring or v-cut solutions are not recommended.

9.4. Thermal Performance

FR4 is one of the most commonly used PCB materials, it is a flame retardant composite material, composed by fiberglass-reinforced and epoxy laminate. One of the features of the FR4, is to have a very low thermal conductivity. An inexpensive way to improve thermal transfer for FR-4 PCBs is to add thermal vias - plated through-holes (PTH) between the conductive layers. Vias are created by drilling holes and copper plating them, in the same way that a PTH or via is used for electrical interconnections between layers. A series of plated through-hole thermal vias, should be located in the GND area underneath Telit module of the PCB to provide a thermal connection from the PCB GND to additional metal layers of the PCB.

The application PCB layout should include plated through-hole thermal vias for efficient heat dissipation from the Telit module into the PCB. One of the following thermal via types should be used:

- Open plated through-hole vias that will provide lower PCB fabrication costs but may fill with solder.
- Plugged and capped plated through-hole vias that will provide higher PCB fabrication costs but will not fill with solder.

Telit recommends creating areas of 10 mil (0.254-mm) vias arranged on a 25 mil (0.635-mm) rectilinear matrix. The reason for this choice is the combination of cost, performance and manufacturability. According to several PCB manufacturers, 10-mil holes and 25-mil spacing are reasonable and repeatable production choice.

A uniform metal plating thickness on the PCB will ensure reliable, high Telit module solder assembly yield.

9.5. Stencil

A silk-screen process will be required for the deposition of solder paste to the PCB, for reflow of the Telit module to the PCB. The silk-screen process requires the use of a metal stencil based on an opening where the solder paste is transferred through the openings on the solder pads of the application PCB. To minimize solder voids and ensure maximum electrical and thermal connectivity of the module to the PCB, large pads, solder volume, and solder straining must be considered in the stencil design. The design and fabrication of the stencil determines the quality of the solder paste deposition onto the PCB and the resulting solder joint after reflow. The primary stencil parameters are aperture size, thickness, and fabrication method. The stencil should be made from stainless steel and the apertures layout can be the same of the recommended footprint (1:1). The recommended thickness shall be 127 um (5 mil). A stencil thickness of 152 µm (6 mil) can be used as well.

9.6. Solder Paste

Various types and grades of solder paste can be used for surface mounting Telit modules. For leadfree applications, a Sn-Ag (SA) or Sn-Ag-Cu (SAC) solder paste can be used. Any Type 3 solder paste that is either water-soluble or no clean is acceptable.

We recommend using only “no clean” solder paste in order to avoid the cleaning of the modules after assembly.

9.7. Solder Reflow

Recommended solder reflow profile:

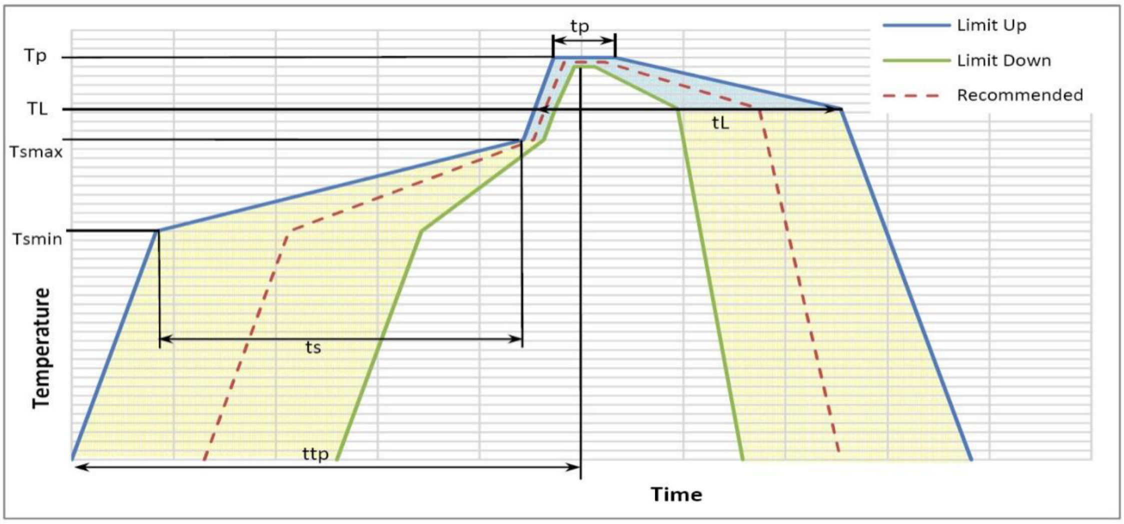

Figure 33: Recommended solder reflow profile

Profile Feature	Pb-Free Assembly Free
Average ramp-up rate (T_L to T_P)	3°C/second max
Preheat – Temperature Min (Tsmin) – Temperature Max (Tsmax) – Time (min to max) (ts)	150°C 200°C 60-180 seconds
Tsmax to TL – Ramp-up Rate	3°C/second max
Time maintained above: – Temperature (TL) – Time (tL)	217°C 60-150 seconds
Peak Temperature (Tp)	245 +0/-5°C
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds
Ramp-down Rate	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

Table 38: Profile feature recommendations

Note: All temperatures refer to topside of the package, measured on the package body surface

Warning: THE LE910R1 MODULE WITHSTANDS ONE REFLOW PROCESS ONLY.

Warning: The above solder reflow profile represents the typical SAC reflow limits and does not guarantee adequate adherence of the module to the customer application throughout the temperature range. Customer must optimize the reflow profile depending on the overall system taking into account such factors as thermal mass and warpage.

9.8. Inspection

An inspection of the solder joint between the solder pads of the Telit module and the application PCB should be performed. The best visual inspection tool for inspection of the Telit module solder joints on the PCB is a transmission X-ray, which can identify defects such as solder bridging, shorts, opens, and large voids (Note: small voids in large solder joints are not detrimental to the reliability of the solder joint).

10. PACKAGING

10.1. Tray

The LE910R1 modules are packaged on trays that can be used in SMT processes for pick & place handling.The first Marketing and Engineering samples of the LE910R1 series will be shipped with the current packaging of the LE910R1 modules (on trays of 20 pieces each). The mass production units of LE910R1 will be shipped according to the following drawings:

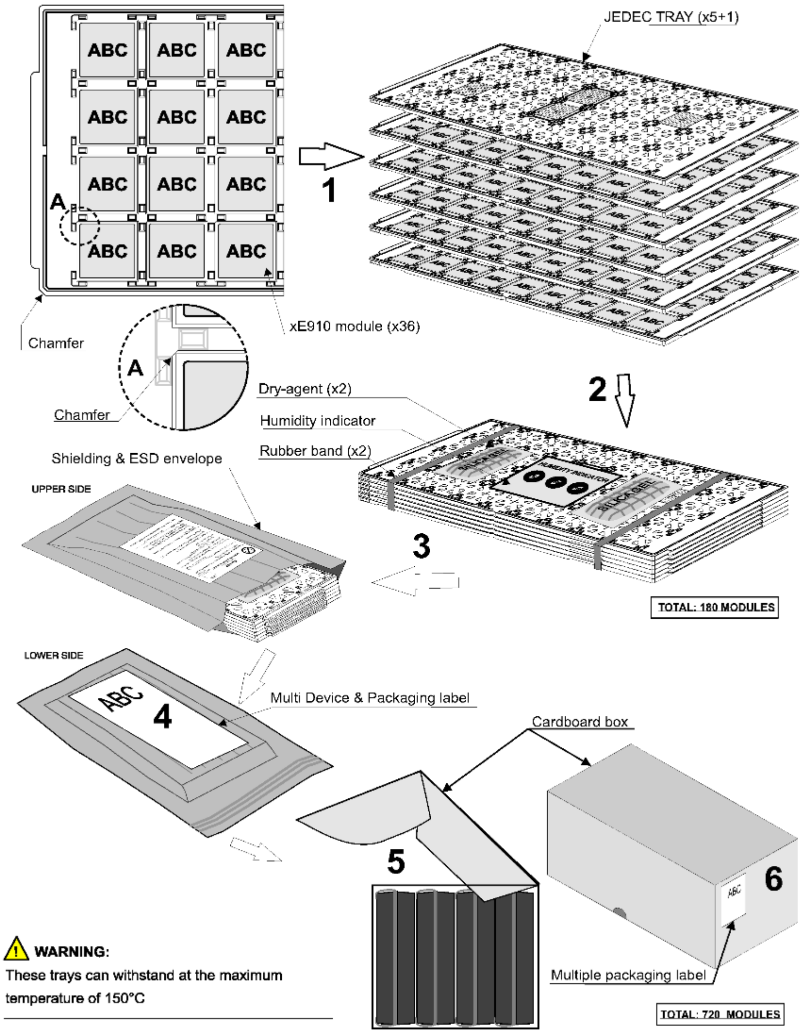

Figure 34: Tray packaging

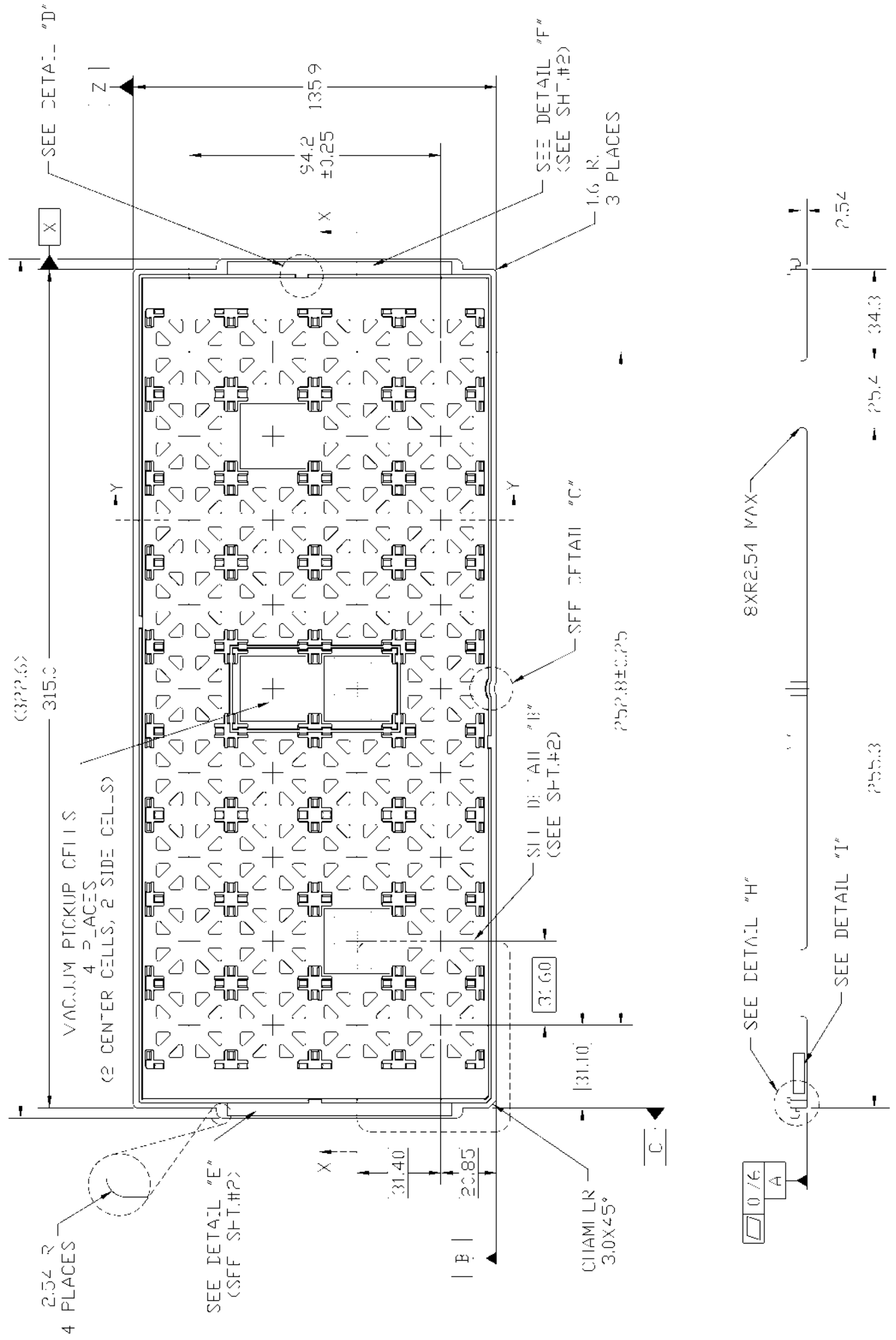

Figure 35: Tray dimensions

10.2. Reel

The LE910R1 can be packaged on reels of 200 pieces each. See figure for module positioning into the carrier.

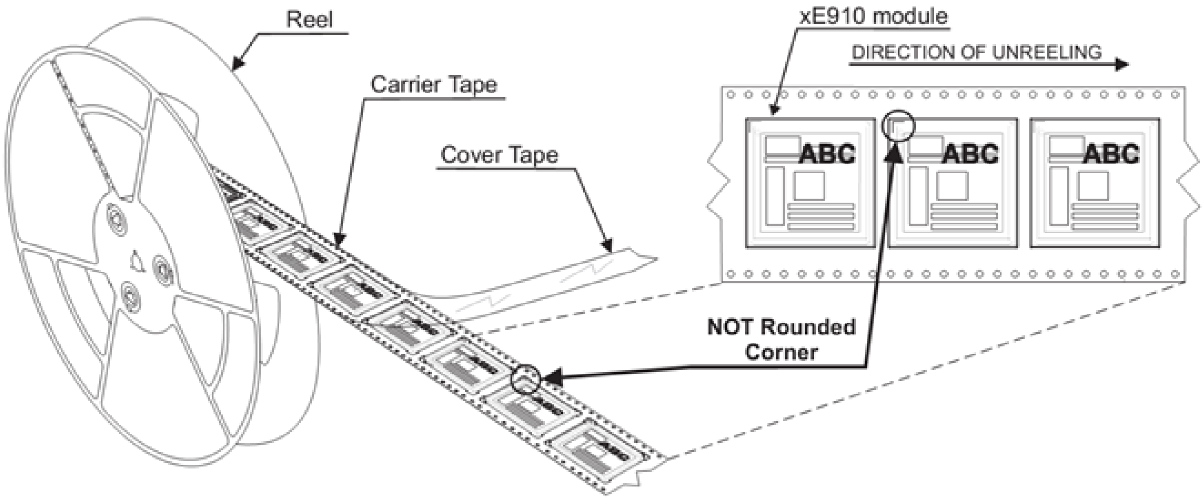

Figure 36: Module positioning into the carrier

10.3. Carrier Tape Detail

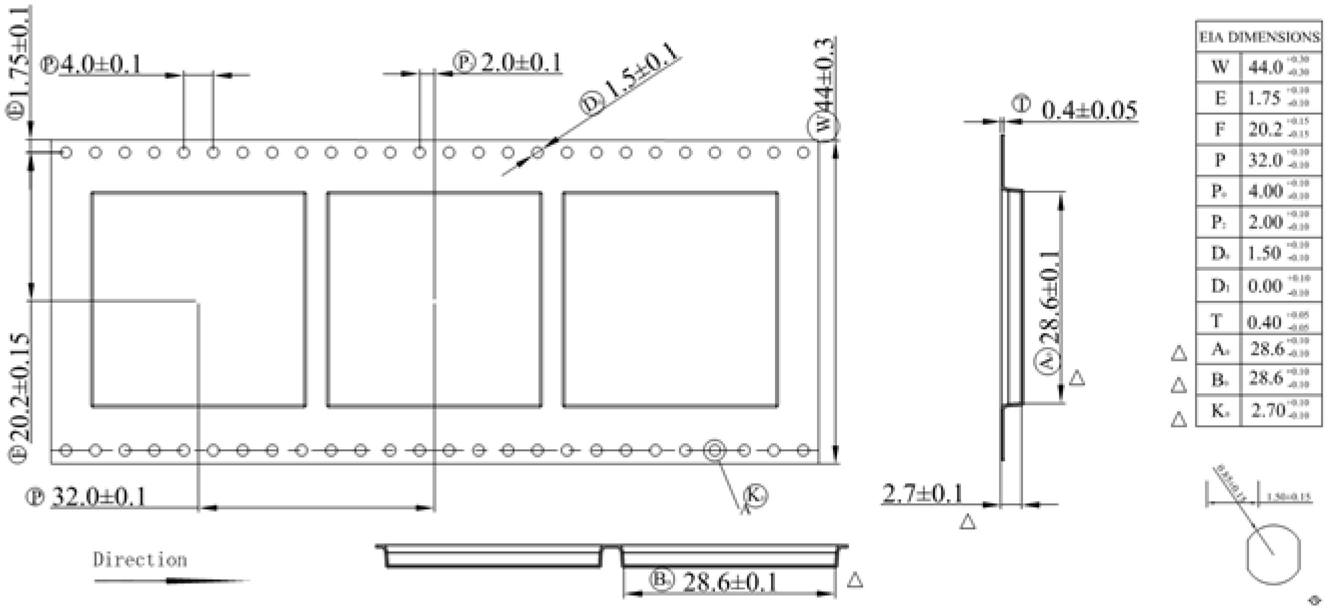

Figure 37: Carrier Tape Detail

10.4. Reel Detail

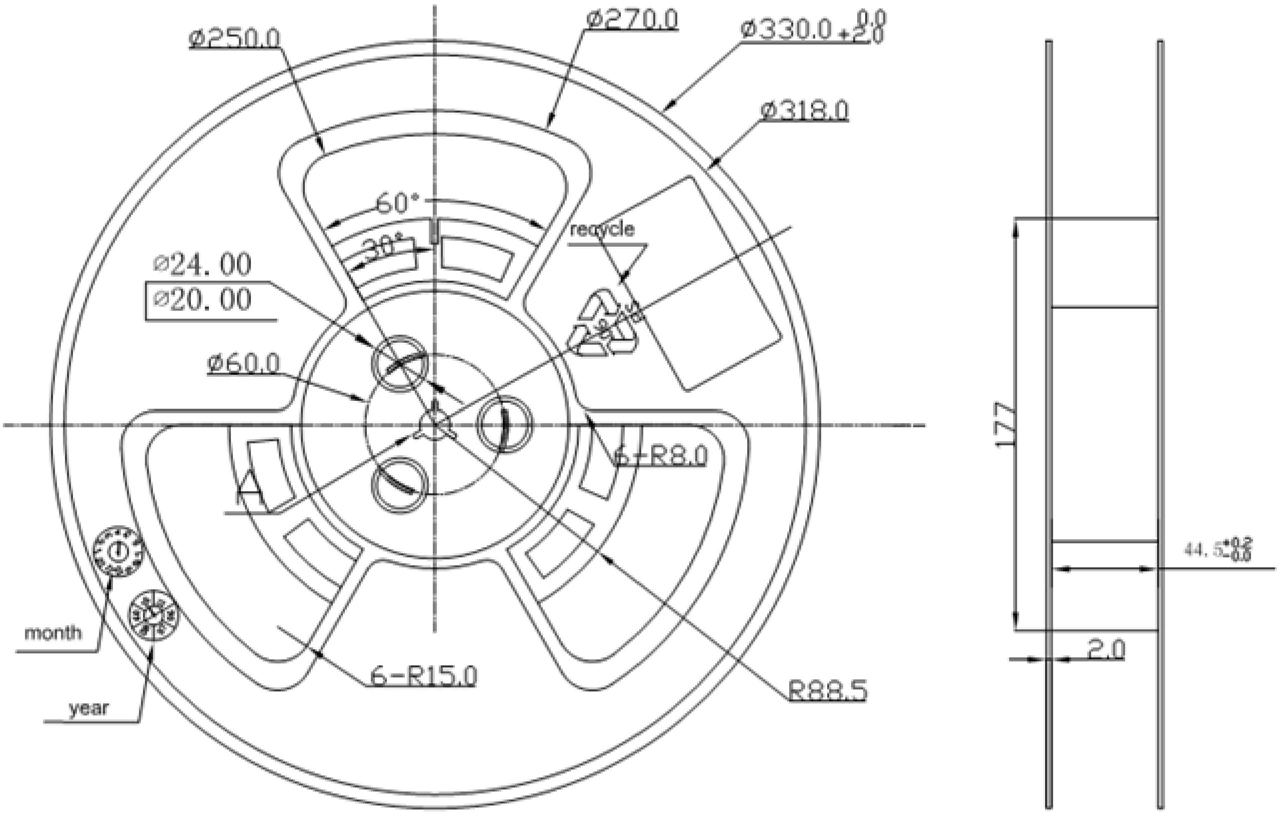

Figure 38: Reel detail

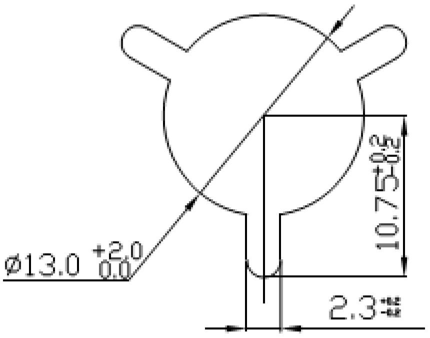

Figure 39: Detail

10.5. Packaging Detail

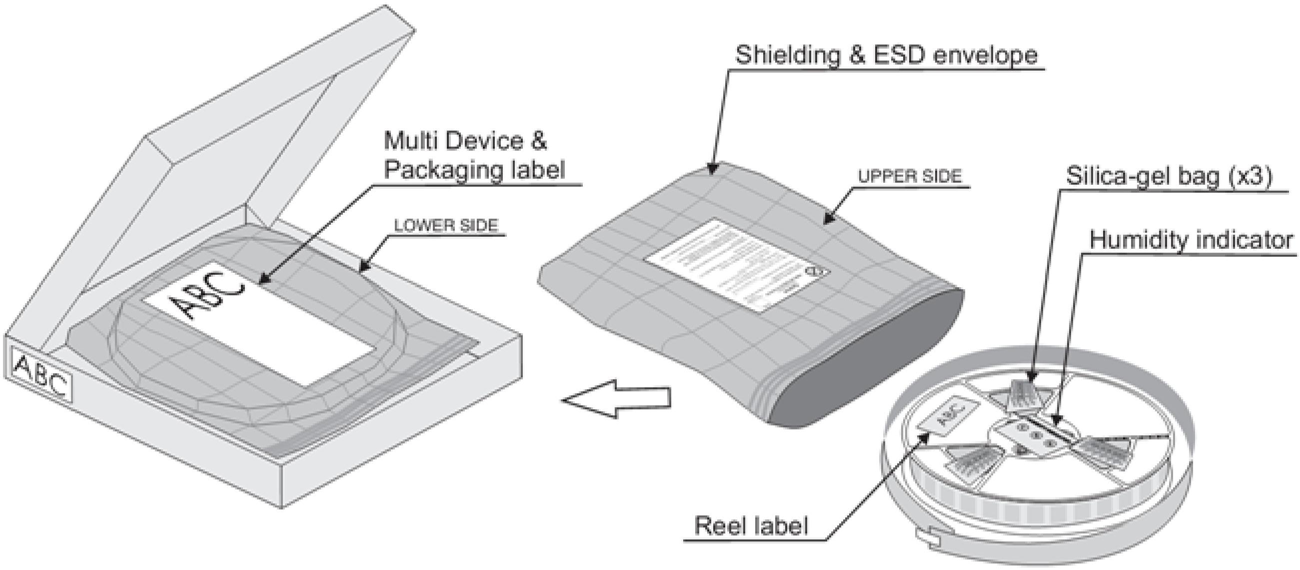

Figure 40: Packaging detail

10.6. Moisture Sensitivity

The LE910R1 is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care all the relatives requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH).

b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5.

c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition b) "IPC/JEDEC J-STD-033D paragraph 5.2" is respected

d) Baking is required if conditions b) or c) are not respected

e) Baking is required if the humidity indicator inside the bag indicates 10% RH

or more.

11. CONFORMITY ASSESTMENT ISSUES

11.1. Approvals Summary

	Europe		Brasil
PRODUCTS	RED	UKCA	ANATEL
LE910R1-EU	Compliant	In progress	In progress
LE910R1-BR	-	-	In progress

Table 39: Approvals summary

11.2. Europe Approvals

11.2.1. RED Declaration of Conformity

Hereby, Telit Communications S.p.A declares compliance with the Directive 2014/53/EU for the modules listed in the table above.

The full text of the EU declaration of conformity is available at the following internet address: *https://www.telit.com/red*

Text of 2014/53/EU Directive (RED) requirements can be found here:

https://eur-lex.europa.eu/legal-content/EN/TXT/?uri=CELEX:32014L0053

11.2.2. UKCA Declaration of Conformity

Hereby, Telit Communications S.p.A declares the compliance with the Radio Equipment Regulations 2017 for UKCA for the modules listed in the table above.

The full text of the UKCA declaration of conformity is available at the following internet address: *https://www.telit.com/ukca*

The UKCA requirements can be found here:

https://www.gov.uk/guidance/using-the-ukca-marking

11.2.3. RED / UKCA Antennas

This radio transmitter has been approved under RED / UKCA to operate with the antenna types listed below with the maximum permissible gain indicated. The usage of a different antenna in the final hosting device may need a new assessment of host conformity to RED / UKCA.

11.3. RoHS and REACH Info

11.3.1. RoHS Info

Any requests on information related to RoHS certifications can be addressed to *Chemical.Certifications@telit.com*.

11.3.2. REACH Info

Any requests on information related to REACH certifications can be addressed to *Chemical.Certifications@telit.com*.

12. REFERENCE TABLE OF RF BANDS CHARACTERISTICS

Mode	Freq. Tx (MHz)	Freq. Rx (MHz)	Channels	Tx-Rx Offset
PCS 1900	1850.2 ~ 1909.8	1930.2 ~ 1989.8	512 ~ 810	80 MHz
DCS 1800	1710 ~ 1785	1805 ~ 1880	512 ~ 885	95 MHz
GSM 850	824.2 ~ 848.8	869.2 ~ 893.8	128 ~ 251	45 MHz
EGSM 900	890 ~ 915	935 ~ 960	0 ~ 124	45 MHz
	880 ~ 890	925 ~ 935	975 ~ 1023	45 MHz
LTE 2100 – B1	1920 ~ 1980	2110 ~ 2170	Tx: 18000 ~ 18599 Rx: 0 ~ 599	190 MHz
LTE 1900 – B2	1850 ~ 1910	1930 ~ 1990	Tx: 18600 ~ 19199 Rx: 600 ~ 1199	80 MHz
LTE 1800 – B3	1710 ~ 1785	1805 ~ 1880	Tx: 19200 ~ 19949 Rx: 1200 ~ 1949	95 MHz
LTE AWS – B4	1710 ~ 1755	2110 ~ 2155	Tx: 19950 ~ 20399 Rx: 1950 ~ 2399	400 MHz
LTE 850 – B5	824 ~ 849	869 ~ 894	Tx: 20400 ~ 20649 Rx: 2400 ~ 2649	45 MHz
LTE 900 – B8	880 ~ 915	925 ~ 960	Tx: 21450 ~ 21799 Rx: 3450 ~ 3799	45 MHz
LTE 800 – B20	832 ~ 862	791 ~ 821	Tx: 24150 ~ 24449 Rx: 6150 ~ 6449	-41 MHz
LTE 700 – B28A	703 ~ 733	758 ~ 788	Tx: 27210 ~ 27510 Rx: 9210 ~ 9510	55 MHz
LTE 700 – B28B	703 ~ 748	758 ~ 803	Tx: 27210 ~ 27659 Rx: 9210 ~ 9659	55 MHz

Table 40: RF Bands Characteristics

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13.3. Safety Recommendations

Make sure the use of this product is allowed in your country and in the environment required. The use of this product may be dangerous and has to be avoided in areas where:

- it can interfere with other electronic devices, particularly in environments such as hospitals, airports, aircrafts, etc.
- there is a risk of explosion such as gasoline stations, oil refineries, etc. It is the responsibility of the user to enforce the country regulation and the specific environment regulation.

Do not disassemble the product; any mark of tampering will compromise the warranty validity. We recommend following the instructions of the hardware user guides for correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to be conformed to the security and fire prevention regulations. The product has to be handled with care, avoiding any contact with the pins because electrostatic discharges may damage the product itself. Same cautions have to be taken for the SIM, checking carefully the instruction for its use. Do not insert or remove the SIM when the product is in power saving mode.

The system integrator is responsible for the functioning of the final product. Therefore, the external components of the module, as well as any project or installation issue, have to be handled with care. Any interference may cause the risk of disturbing the GSM network or external devices or having an impact on the security system. Should there be any doubt, please refer to the technical documentation and the regulations in force. Every module has to be equipped with a proper antenna with specific characteristics. The antenna has to be installed carefully in order to avoid any interference with other electronic devices and has to guarantee a minimum distance from the body (20 cm). In case this requirement cannot be satisfied, the system integrator has to assess the final product against the SAR regulation.

The equipment is intended to be installed in a restricted area location.

The equipment must be supplied by an external specific limited power source in compliance with the standard EN 62368-1:2014.

The European Community provides some Directives for the electronic equipment introduced on the market. All of the relevant information is available on the European Community website:

https://ec.europa.eu/growth/sectors/electrical-engineering_en

14. GLOSSARY

ADC	Analog – Digital Converter
CLK	Clock
CMOS	Complementary Metal – Oxide Semiconductor
CS	Chip Select
DAC	Digital – Analog Converter
DTE	Data Terminal Equipment
ESR	Equivalent Series Resistance
GPIO	General Purpose Input Output
HS	High Speed
HSDPA	High Speed Downlink Packet Access
HSIC	High Speed Inter Chip
HSUPA	High Speed Uplink Packet Access
I/O	Input Output
MISO	Master Input – Slave Output
MOSI	Master Output – Slave Input
MRDY	Master Ready
PCB	Printed Circuit Board
RTC	Real Time Clock
SIM	Subscriber Identification Module
SRDY	Slave Ready
TTSC	Telit Technical Support Centre
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
VNA	Vector Network Analyzer
VSWR	Voltage Standing Wave Radio

15. DOCUMENT HISTORY

Revision	Date	Changes
1	2022-01-31	
0	2021-12-27	First issue

From Mod.0818 rev.4

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www.telit.com