# UE/HE910V2_DE/CE910_HE920
# Digital Voice Interface Application Note

80000NT10101A Rev.0 2013-06-25


Making machines talk.

# APPLICABILITY TABLE

| PRODUCT |
| --- |
| DE910 Family |
| HE910- V2 Family |
| CE910 Family |
| UE910- V2 Family |
| HE920 Family |

 

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Contents



 

# 1 Introduction

## 1.1 Scope

The aim of this document is the description of some hardware specification useful to develop a product using Telit modules supporting DVI, as specified in the aforementioned applicability table.

## 1.2 Audience

This document is intended for Telit customers, who are integrators, about to implement their applications using our UE/HE910V2, DE/CE910 and HE920 modules.

## 1.3 Contact Information, Support

For general contact, technical support, to report documentation errors and to order manuals, contact Telit's Technical Support Center (TTSC) at:

TS-EMEA@telit.com
TS-NORTHAMERICA@telit.com
TS-LATINAMERICA@telit.com
TS-APAC@telit.com

Alternatively, use:

http://www.telit.com/en/products/technical-support-center/contact.php

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

http://www.telit.com

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Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

 

## 1.4 Document Organization

This document contains the following chapters:

Chapter 1: "Introduction" provides a scope for this document, target audience, contact and support information, and text conventions.

Chapter 2: "Overview" provides an overview of the document.

Chapter 3: "UE/HE910V2_DE/CE910_HE920 DVI (PCM)" describes the DVI port as far as the UE/HE910V2_DE/CE910_HE920 modules are concerned

Chapter 4: "Protocol description"

Chapter 5: "Parameters and timing characteristics"

Chapter 6: "Custom AT commands"

Chapter 7: "External codec" provides an example of interfacing with an external audio codec.

## 1.5 Text Conventions


***Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.***

***Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.***

**Tip or Information – Provides advice and suggestions that may be useful when integrating the module.**

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

 

## 1.6 Related Documents

- Software User guide
- Hardware User Guide
- Product description
- AT Commands Reference Guide

## 1.7 Document History

| Revision | Date | Changes |
|---|---|---|
| 0 | 2013-06-25 | First release |

 

# 2 Overview

The Telit Modules support the ***Digital Voice Interface*** (from here onwards ***DVI***), which can be used to transfer digital audio data *to* and *from* the module itself.

The ***DVI*** uses the *PCM interface* as part of the audio front end; it easily allows for an external codec to be used instead of the internal codec.

As an example, through the ***DVI*** you could connect a Telit Module to a Bluetooth device.

## 2.1 Hint on PCM

Although analog communication is ideal for human communication, analog transmission is neither robust nor efficient at recovering from line noise.
As example in the early telephony network, when analog transmission was passed through amplifiers to boost the signal, not only was the voice boosted but the line noise was amplified, as well. This line noise resulted in an often-unusable connection.
It is much easier for digital samples, which are comprised of 1 and 0 bits, in order to be separated from line noise. Therefore, when analog signals are regenerated as digital samples, a clean sound is maintained.
PCM converts analog sounds into digital form by sampling the analog sounds 8000 times per second and converting each sample into a numeric code. If you sample an analog signal at twice the rate of the highest frequency of interest, you can accurately reconstruct that signal back into its analog form (Nyquist theorem). Because most speech content is below 4000Hz, a sampling rate of 8000 times per second (8 KHz that means 125 µSec between samples) is required.

## 2.2 General information

The Telit Modules can have one ***DVI*** port.

Please refer to the User Guide of the module that you are using to know the number of the available ***DVI*** port.

 

# 3 UE/HE910V2, DE/CE910 and HE920 DVI (PCM)

The UE/HE910V2, DE/CE910 and HE920 have only one ***DVI*** port (or *Auxiliary Codec Port*), the hardware supports for continual transmission and reception of PCM Data. It has two different modes:

- Standard Operating Mode, actually used
- Standalone Operating Mode, actually not allowed

The activation of the ***DVI function*** does the internal codec automatically disabled, and the user has to interface an external codec (the "*AUXILIARY PCM device*") in order to use it.

Even if the ***Auxiliary Codec Port*** is physically one, you can set it via software in two configuration modes, each one with its own clock frequency, clock format, frame synchronism and clock mode.

The gains (*volumes*) for DOWNLIK and UPLINK paths can be set:

- by the dedicated AT commands
- tuning the gain of the external codec amplifiers (refer to external codec manual)

## 3.1 Configuration mode

The configuration modes are ***Auxiliary (Normal mode)*** and ***Primary (Highspeed mode).*** The choice depends from the needs of the customer, but always keeping in mind that only *one mode at time* is allowed.

- **Auxiliary** *Configuration Mode* is the *default mode* running at 128 KHz with standard *Long Frame Sync* timing. It supports: *16-bit linear or 8-bit A-Law* or *µ-Law with padding*.

- ***Primary*** *Configuration Mode* is the *other mode* running at 2.048 MHz with *Short Frame Sync* timing. It supports: *16-bit linear* or *8-bit A-Law* or *µ-Law with padding*.

They both use the same hardware path at 8 KHz sample-rate, in burst mode and mono voice data.

*A-Law* is the PCM variant in Europe, while *µ-Law* is the PCM variant in America.

 

## 3.2 Clock Mode

Being a bidirectional interface, you can choose the "direction" of clock for receive and transmit codec PCM data.

The *clock Mode (or in other words the module)* can be:
:

- ***Master*** if UE/HE910V2_DE/CE910_HE920 are the clock signal source; the ***PCM_CLK*** pin becomes an output and its direction is from UE/HE910V2_DE/CE910_HE920 to external codec.

- ***Slave*** if the external "*AUXILIARY PCM device*" is the signal clock source; the ***PCM_CLK*** pin becomes an input and its direction is from external codec to UE/HE910V2_DE/CE910_HE920.

**WARNING:**

***Slave mode* is not allowed in the *"AUXILIARY Configuration Mode (128K with standard Long sync frame).***

## 3.3 Summary

- the *Digital Voice Interface* allows the use of an external codec .It is Software , and can be the "*AUXILIARY PCM Interface*" (*the default interface* ) working at 128KHz clock , or the "*PRIMARY PCM Interface*" (*the other interface*) working at 2.048MHz ;
- the "*AUXILIARY CODEC PORT*" operates at 128KHz when the "*AUXILIARY PCM Interface*" is active
- the "*AUXILIARY CODEC PORT*" operates at 2.048MHz when the "*PRIMARY PCM Interface*" is active
- the "*AUXILIARY CONFIGURATION Mode*" sets the clock frequency/sync type to 128KHz/ long sync
- the "*PRIMARY CONFIGURATION Mode*" sets the clock frequency/sync type to 2.048MHz/ short sync
- the "*MASTER Clock Mode*" sets UE/HE910V2_DE/CE910_HE920 as clock source
- the "*SLAVE Clock Mode*" sets the external "*AUXILIARY PCM device*" as clock source

 

| Standard Operating Mode | | | Standalone Operating Mode |
|---|---|---|---|
| UE/HE910V2_ DE/CE910_ HE920 | YES | | Not allowed |
| DVI MASTER Clock Mode | clock freq. = 128KHz long-frame sync | AUXILIARY Configuration Mode | |
| | clock freq. =2.048KHz short-frame sync | PRIMARY Configuration Mode | |
| DVI SLAVE Clock Mode | clock source= external | | |

**Table 1. Settings Map of the Digital Voice Interface**

## 3.4 DVI port pinout

The ***DVI port*** is accessible on four pins on UE/HE910V2_DE/CE910_HE920. The port itself is mapped on two logical ports, *Auxiliary port* and *Primary port*, depending on the functionality set via AT command. For the timing diagram of the two different refer to Protocol Description in chapter 3.

According to the applied *Configuration Mode*, you will have on the pins of the UE/HE910V2_DE/CE910_HE920 LGA PAD signals with different logical names.

The table 2 summarizes the signal and correspondent pin, while the figure 2 is the block diagram of the routing of the same signals.

| LGA PAD or Connector PINOUT | Function | Primary PCM Interface | Auxiliary PCM Interface |
|---|---|---|---|
| name | | Logical name | |
| DVI_CLK | Clock in/out | PCM_CLK | AUX_PCM_CLK |
| DVI_RX | Data in | PCM_DIN | AUX_PCM_DIN |
| DVI_TX | Data out | PCM_DOUT | AUX_PCM_DOUT |
| DVI_WA0 | Synchronism | PCM_SYNC | AUX_PCM_SYNC |

**Table 2. Signal name Map**

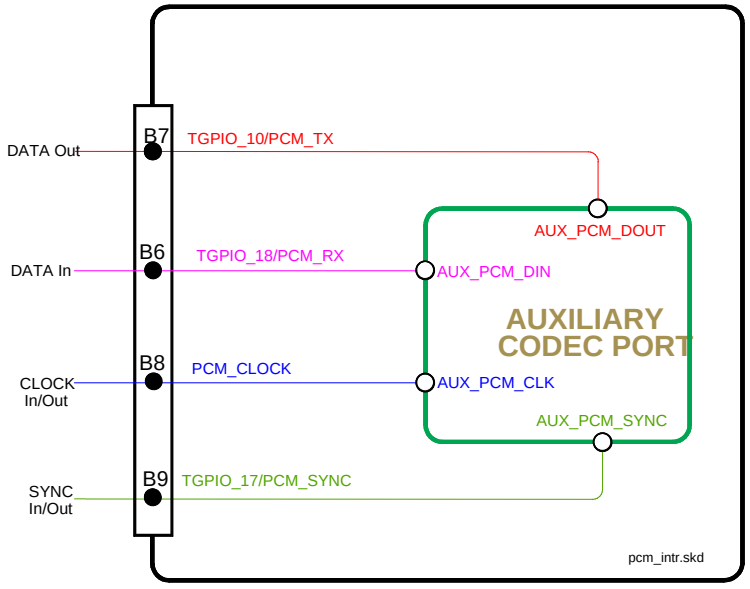


**Figure 1. Auxiliary Codec Port signals routing**

### 3.4.1 Pin position on UE/HE910V2_DE/CE910_HE920 Interface

Telit offers the dedicated Interface Board ***CS1467x*** and ***KS0145x*** where the **UE/HE910V2_DE/CE910_HE920** could be fitted on during the development phase of the customer application.

In such a way the useful signals are easily available on two connectors named PL203, PL101 and PL102.

| DVI Function | PL203 |
|---|---|
| DVI_CLK | **4** |
| DVI_WA0 | **2** |
| DVI_RX | **1** |
| DVI_TX | **3** |

**Table 3.1 DVI signals Pin assignment on CS1467x for xE910-xxx**

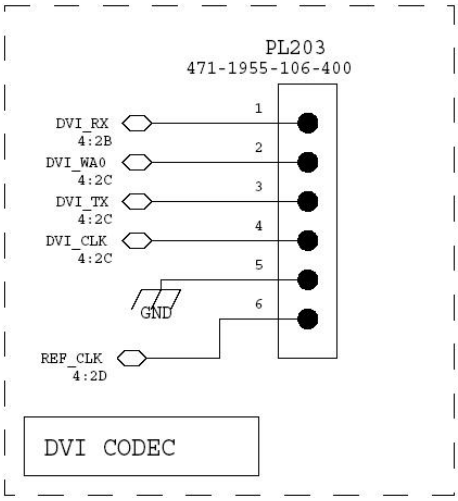


**Figure2.1 DVI Pin displacement on CS1467x for xE910-xxx**

| DVI Function | PL102 |
|---|---|
| **PCM_CLOCK** | **4** |
| **PCM_SYNC** | **3** |
| **PCM_RX** | **1** |
| **PCM_TX** | **2** |

**Table 3.3 DVI signals Pin assignment on KS0145x for xE920-xxx**

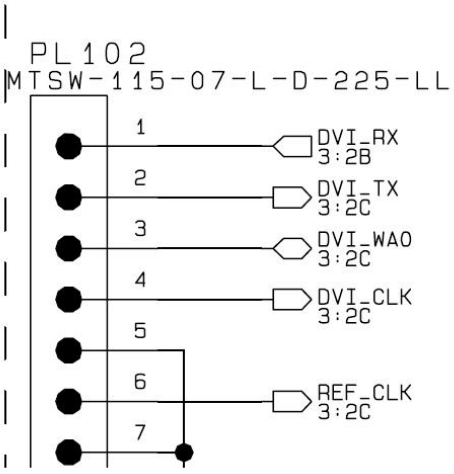


**Figure2.3 DVI Pin displacement on KS0145x for xE920-xxx**

 

## 3.5 Electrical Characteristics

| | Minimum | Maximum | Unit |
|---|---|---|---|
| **$V_{IL}$** | -0.3 | 0.36 | V |
| **$V_{IH}$** | 1.44 | 2.1 | V |
| $V_{OL}$ | -0.3 | 0.18 | V |
| $V_{OH}$ | 1.62 | 2.1 | V |

**Table 3.4 DVI signals Electrical characteristics for xE910-xxx and xE920-xxx**

## 3.6 Clock and Sync direction

The table below summarizes how change the *Data Clock* and *Frame Synchronism* direction according to *Configuration Mode*.

| | | | | | Master | Slave |
|---|---|---|---|---|---|---|
| LGA Pad | Function | Name | Function | | Direction | |
| **4** | **PCM_CLOCK** | ***DVI_CLK*** | **Data Clock** | → | **OUT** | **IN** |
| **2** | **PCM_SYNC** | ***DVI_WA0*** | **Frame Synchronism** | → | **OUT** | **IN** |
| **1** | **PCM_RX** | ***DVI_RX*** | **Received Data** | → | **IN** | **IN** |
| 3 | PCM_TX | *DVI_TX* | Transmitted Data | → | OUT | OUT |

# 4 Protocol Description

The ***DVI*** operates in 16-bit data burst mode, starting with the most significant bit.

GSM voice is 13-bit *2's* complement but the output of the speech decoder is saved on 16-bit *2's* complement (Q15 format). The last 3 LSBs are equal to 0.

The frame lasts for 17 clock pulses, as one more clock pulse is needed for the frame synchronization of the signal ***PCM_SYNC***.

Following the falling edge of the ***PCM_SYNC*** signal, the data bits are sampled at the module data input (RX) and module output data (TX) at the next falling clock (CLK) pulse edge.

All data is 8KHz and 16 bits with DVI (PCM interface).

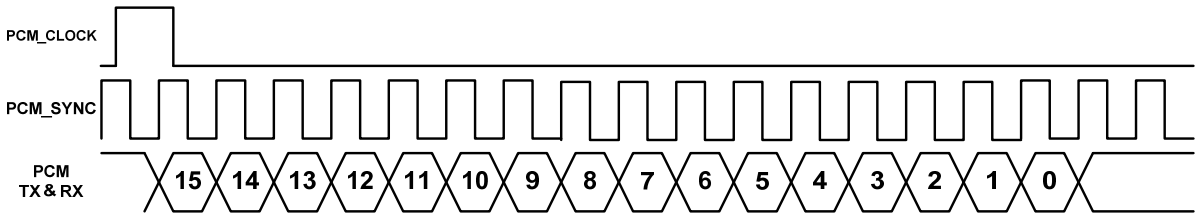


**Figure 3. Digital Voice Interface (PCM) signal timing**

## 4.1 Primary Mode

On ***Primary*** mode UE/HE910V2_DE/CE910_HE920 provide a 16-bit linear or 8-bit A-law or µ-law with padding, with short-sync and 2.048MHz clock (on the ***PCM_CLOCK*** pin).

Both ***Master*** and ***Slave*** mode are allowed.

## 4.2 Auxiliary Mode

On ***Auxiliary mode*** UE/HE910V2_DE/CE910_HE920 provide 16-bit linear or 8-bit A-law or µ-law with padding, with ***long-sync*** and 128KHz clock (on the **PCM_CLOCK** pin).

Only ***Master*** mode is allowed.

**NOTE:**

**UE910-xxx DOES NOT support Auxiliary Mode (128K / Long-sync).**

 

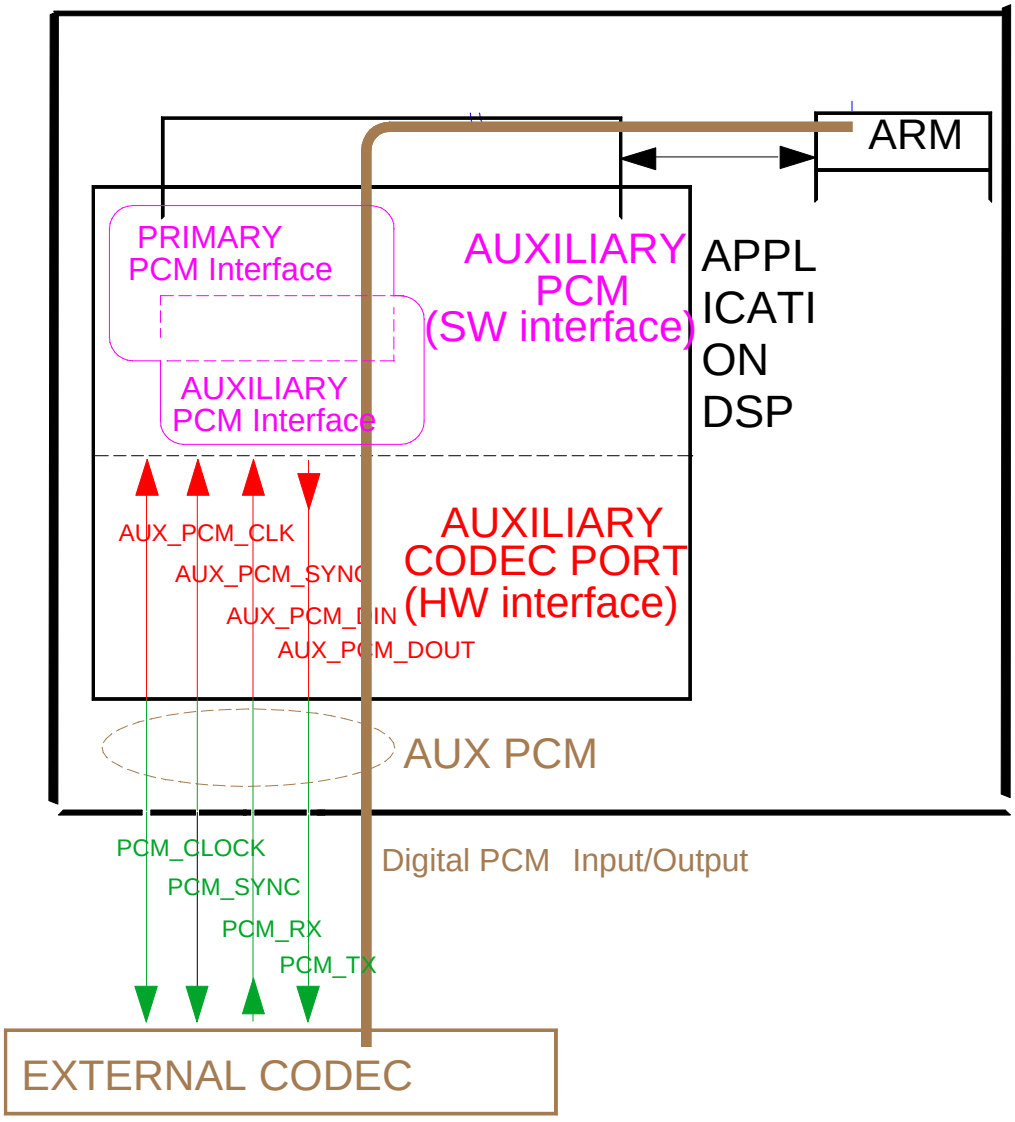


Figure 4. Simplified DVI block diagram

# 5 Parameters and Timing Characteristics

## 5.1 Primary PCM Interface

| Parameter | Description | Min | Typical | Max | Units |
|---|---|---|---|---|---|
| t(sync) | PCM_SYNC cycle time | | 125 | | us |
| t(synch) | PCM_SYNC high time | 400 | 500 | | ns |
| t(syncl) | PCM_SYNC low time | | 124.5 | | us |
| t(clk) | PCM_CLOCK cycle time | | 488 | | ns |
| t(clkh) | PCM_CLOCK high time | | 244 | | ns |
| t(clkl) | PCM_CLOCK low time | | 244 | | ns |
| t(susync) | PCM_SYNC setup time high before falling edge of PCM_CLOCK | 60 | | | ns |
| t(hsync) | PCM_SYNC hold time after falling edge of PCM_CLOCK | 60 | | | ns |
| t(sudin) | PCM_RX setup time before falling edge of PCM_CLOCK | 50 | | | ns |
| t(hdin) | PCM_RX hold time after falling edge of PCM_CLOCK | 10 | | | ns |
| t(pdout) | Delay from PCM_CLOCK rising to PCM_TX valid | | | 350 | ns |
| t(zdout) | Delay from PCM_CLOCK falling to PCM_TX HIGH-Z | | 160 | | ns |

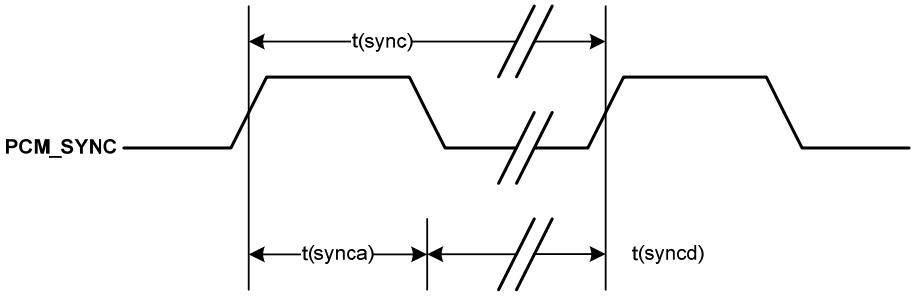


**Figure 5. Primary PCM_SYNC timing (only Short sync)**

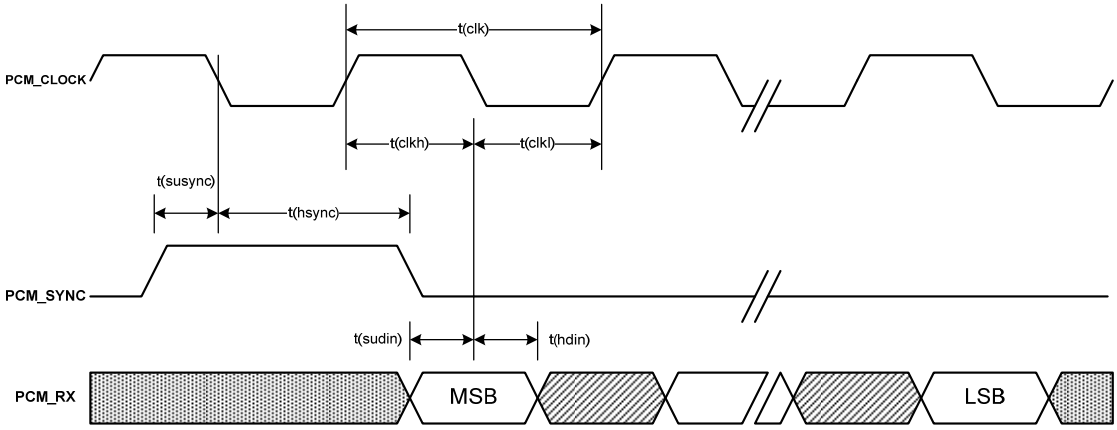


**Figure 6. External codec to UE/HE910V2_DE/CE910_HE920 timing**

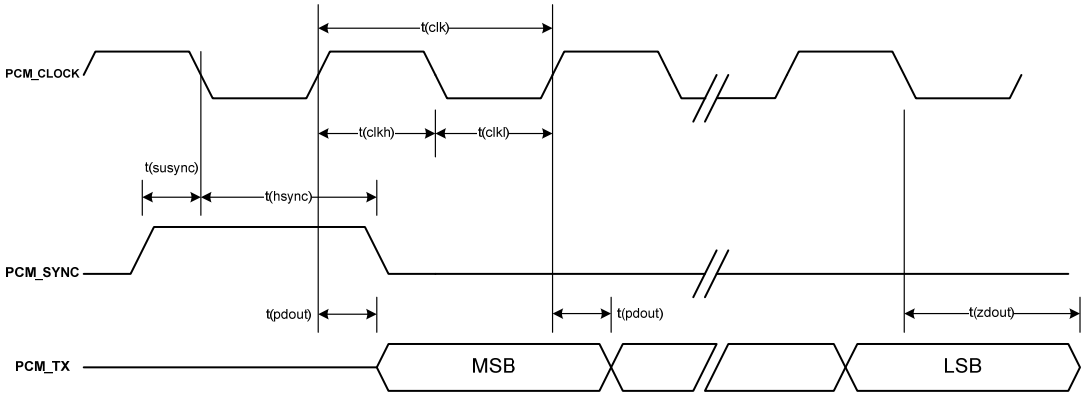


**Figure 7. UE/HE910V2_DE/CE910_HE920 to External codec timing**

## 5.2 Auxiliary PCM Interface

| Parameter | Description | Min | Typical | Max | Units |
|---|---|---|---|---|---|
| t(auxsync) | PCM_SYNC cycle time | | 125 | | us |
| t(auxsynch) | PCM_SYNC high time | 62.4 | 62.5 | | us |
| t(auxsyncl) | PCM_SYNC low time | 62.4 | 62.5 | | us |
| t(auxclk) | PCM_CLOCK cycle time | | 7.8 | | us |
| t(auxclkh) | PCM_CLOCK high time | 3.8 | 3.9 | | us |
| t(auxclkl) | PCM_CLOCK low time | 3.8 | 3.9 | | us |
| t(suauxsync) | PCM_SYNC setup time high before falling edge of PCM_CLOCK | 1.95 | | | us |
| t(hauxsync) | PCM_SYNC hold time after falling edge of PCM_CLOCK | 1.95 | | | us |
| t(suauxdin) | PCM_RX setup time before falling edge of AUX_PCM_CLK | 70 | | | ns |
| t(hauxdin) | PCM_RX hold time after falling edge of AUX_PCM_CLK | 20 | | | ns |
| t(pauxdout) | Delay from AUX_PCM_CLK rising to AUX_PCM_TX valid | | | 50 | ns |

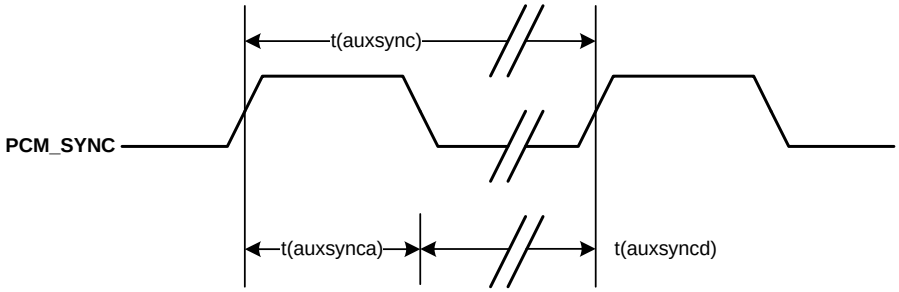


**Figure 8. AUX PCM_SYNC timing (only Long sync)**

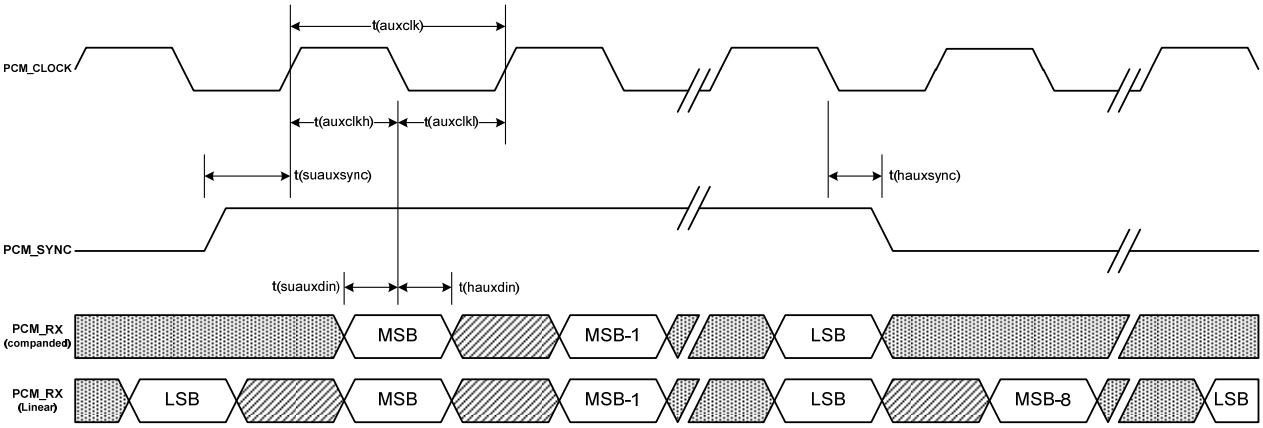


**Figure 9. AUX External codec to UE/HE910V2_DE/CE910_HE920 timing**

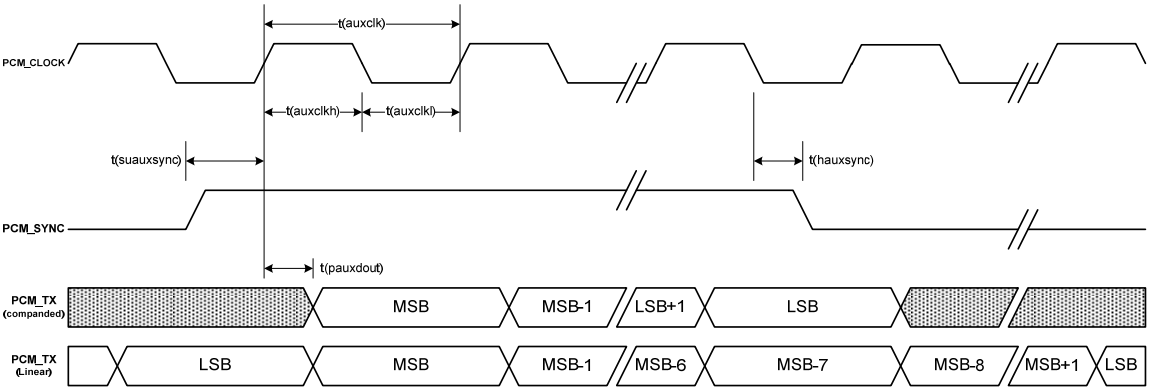


**Figure 10. AUX UE/HE910V2_DE/CE910_HE920 to External codec timing**

 

# 6 Custom AT Commands

The ***DVI can*** be set by the following custom ***AT commands***.
Needing more details, please refer to ***AT_Commands_Reference_Guide_<Model name>*** Telit specification document.

## 6.1 DVI port Enabling

| **#DVI - Digital Voiceband Interface** | |
|---|---|
| **AT#DVI=<mode> [,<dviport>, <clockmode>]** | Set command enables/disables the Digital Voiceband Interface.<br><br>Parameters:<br>**<mode>** - enables/disables the DVI.<br>1 - enable DVI; audio is forwarded to the DVI block (factory default)<br>**<dviport>**<br>2 - DVI port 2 will be used<br>**<clockmode>**<br>0 - DVI slave<br>1 - DVI master (factory default)<br><br>Note: **#DVI** parameters are saved in the extended profile |
| **AT#DVI?** | Read command reports last setting, in the format:<br><br>**#DVI: <mode>,<dviport>,<clockmode>** |
| **AT#DVI=?** | Test command reports the range of supported values for parameters **<mode>,<dviport>** and **<clockmode>** |
| Example | AT#DVI=1,2,1<br>OK<br><br>*DVI activated for audio. DVI is configured as master providing on DVI Port #2* |

 

## 6.2 DVI port Configuration

| **#DVICFG – DVI CONFIGURATION** | |
|---|---|
| **AT#DVICFG=[ <clock>[,<decoder pad>[,<decoder format>[, <encoder pad>[,<encoder format>]]]]]** | Set command sets the DVI configuration<br><br>Parameter:<br>**<clock>**: Clock speed for master mode<br>0 : normal mode<br>1 : high speed mode<br>**<decoder pad>**: PCM padding enable in decoder path<br>0 : disable<br>1 : enable<br>**<decoder format>**: PCM format in decoder path<br>0 : u-Law<br>1 : A-Law<br>2 : linear<br>**<encoder pad>**: PCM padding enable in encoder path<br>0 : disable<br>1 : enable<br>**<encoder format>**: PCM format in encoder path<br>0 : u-Law<br>1 : A-Law<br>2 : linear<br><br>Note: #DVICFG parameters are saved in the extended profile |
| **AT#DVICFG?** | Read command reports the value of parameter in the format:<br><br>**#DVICFG: <clock>,<decoder pad>,<decoder format>, <encoder pad>,<encoder format>** |
| **AT#DVICFG=?** | Test command returns the supported range of values of parameter **<clock>,<decoder pad>,<decoder format>, <encoder pad>,<encoder format>**. |

 

## 6.3 DVI gain

| **#PCMTXG – DVI Microphone Gain** | |
|---|---|
| **AT#PCMTXG=<TX_VOL>** | Set command sets the DVI (PCM) Audio TX gain<br><br>Parameter:<br>**<TX_VOL>** : PCM TX volume in TX path (factory default : 0)<br>TX VOL RANGE : -5000(-50 dB) ~ 1200(+12 dB)<br><br>Note: meaning of a TX_VOL is 1/100 dB step.<br>Note: meaning of -50 dB is mute |
| **AT#PCMTXG?** | Read command returns the current PCM Audio TX value:<br>**#PCMTXG: <TX_VOL>** |
| **AT#PCMTXG=?** | Test command returns the supported range of values of parameter<br>**<TX_VOL>** |

| **#PCMRXG – DVI Speaker Volume Level** | |
|---|---|
| **AT#PCMRXG=<RX_VOL>** | Set command sets the PCM Audio RX value<br><br>Parameter:<br>**<RX_VOL>** : PCM RX volume in RX path (factory default : 0)<br>RX_VOL RANGE : -5000(-50 dB) ~ 1200(+12 dB)<br><br>Note: meaning of a RX_VOL is 1/100 dB step.<br>Note: meaning of -50 dB is mute |
| **AT#PCMRXG?** | Read command returns the current PCM Audio RX value:<br>**#PCMRXG: <RX VOL>** |
| **AT#PCMRXG=?** | Test command returns the supported range of values of parameter **<RX VOL>** |

# 7 External Codec

The market offers great variety of audio codecs and, obviously, the customers will choose by itself the device that better fits their application.
Just as an example, in the following we go describing a possible interfacing with an external audio codec.

## 7.1 The choice

MAXIM ® offers in the same package the ***MAX9851/9853***, two stereo audio CODECs designed to provide a complete audio solution, differing only in the stereo output amplifiers:

- ***MAX9853*** has Stereo Differential Line Output Amplifiers
- ***MAX9851*** has Stereo 1.25W/ 8Ω Class-D Amplifiers

We describe the implementation of ***MAX9853***.

### 7.1.1 Hint on Class-D amplifier

As said before, the stereo output amplifiers of ***MAX9851*** are *Class-D* stages.

This type of amplifier uses switching technique to achieve power efficiency more than 90% . Not only, by this configuration do we not need large transformers and heavy heatsinks, because they are smaller and lighter in weight than an equivalent Class AB amplifier.

The ***Class-D audio Amplifiers*** operate in on/off mode: their output stages reproduce signals with a bandwidth well below the switching frequency, and the losses are minimized allowing each output device to be either fully on or off.

The input signal is converted to a sequence of pulses whose averaged value is directly proportional to the instantaneous amplitude of the signal. The frequency of the pulses is typically ten times or more the highest significant frequency in the input signal. The output of such an amplifier contains unwanted spectral components (*the pulse frequency and its harmonics*) which must be removed by an external passive filter. The resulting filtered signal is then an amplified replica of the input.

 

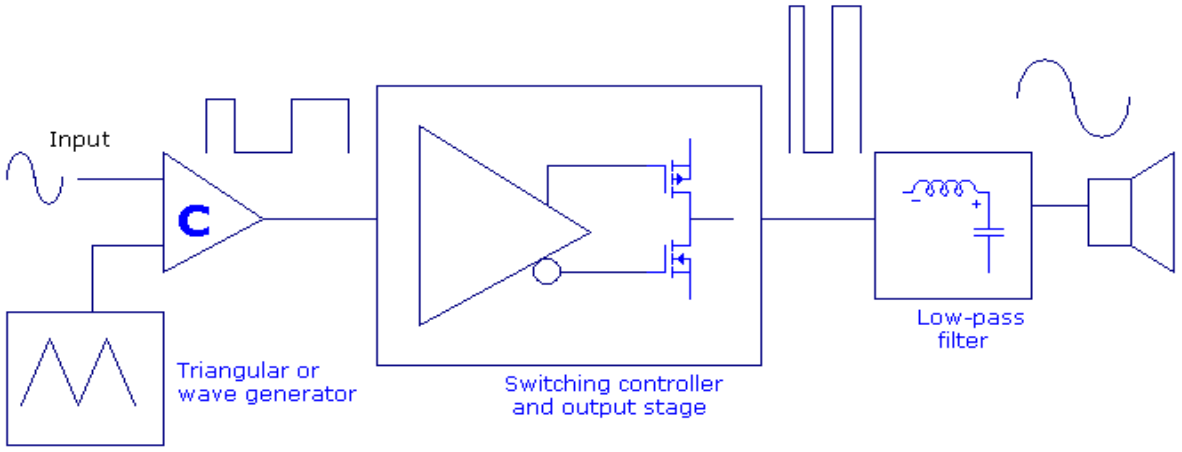


**Figure 11 . Block diagram of the Class-D audio Amplifier**

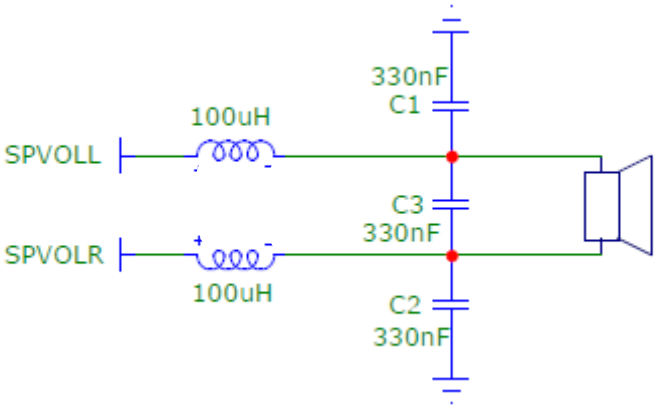


**Figure 12. Class-D Low-Pass output filter**

## 7.2 MAX9853 features

MAX9853 audio codec provides:

- stereo amplifiers to directly drive an headset
- a mono (receiver) speaker amplifier
- microphone input amplifiers
- flexible input selection and gain control

Control for volume levels, signal mixing, and operating modes could be applied.

Two "*serial digital audio interfaces"* are at your disposal, one intended to accept *Voiceband Data* and the other to accept $I^2S$ *Data* , supporting a variety of serial audio formats.
The *Voiceband interface* can be reconfigured as needed to act as a secondary $I^2S$ feed input, allowing multiple audio sources mixing at different sample rates (*ringer tones and/or other audio inputs*).

The "*secondary serial audio interface"* has independent supply voltages allowing integration into multiple supply systems.

The stereo digital-to-analog converter *(DAC)* path includes:

- filtering and mixing
- programmable-gain amplifiers *(PGA)* on the front end, allowing dynamic range optimization with a wide range of input sources
- soft muting
- optional Voiceband digital filtering

The stereo analog-to-digital converter *(ADC)* converts audio signals from either internal or external microphones or stereo line inputs.
The input amplifiers have a programmable gain ***G=(0 ÷ +40)dB*** , handling both amplified microphones and electret modules.
In addition to a digital highpass filter to remove DC offset voltages, the ADC also features Voiceband digital filtering.

 

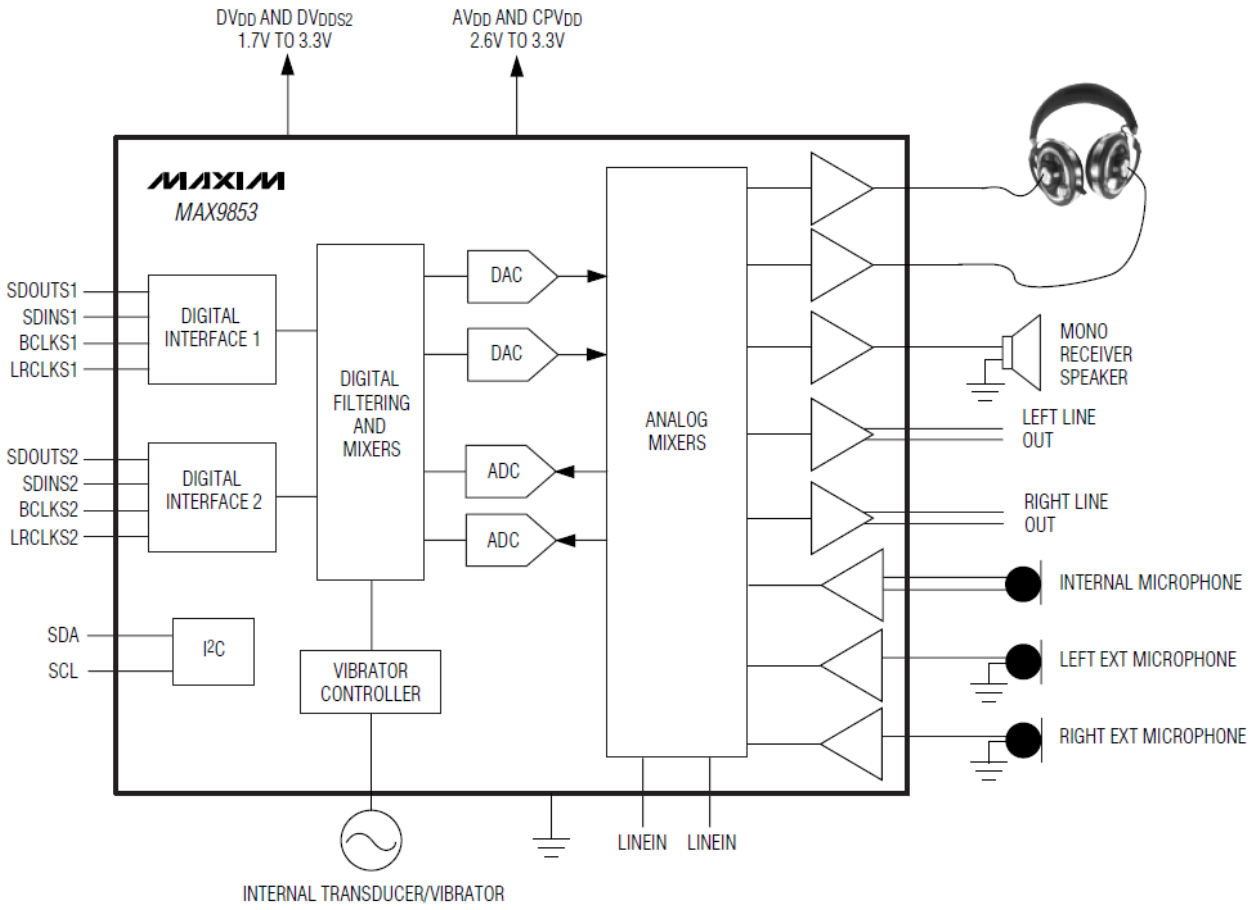


**Figure 13. Block diagram of *MAX9853* audio codec**

 

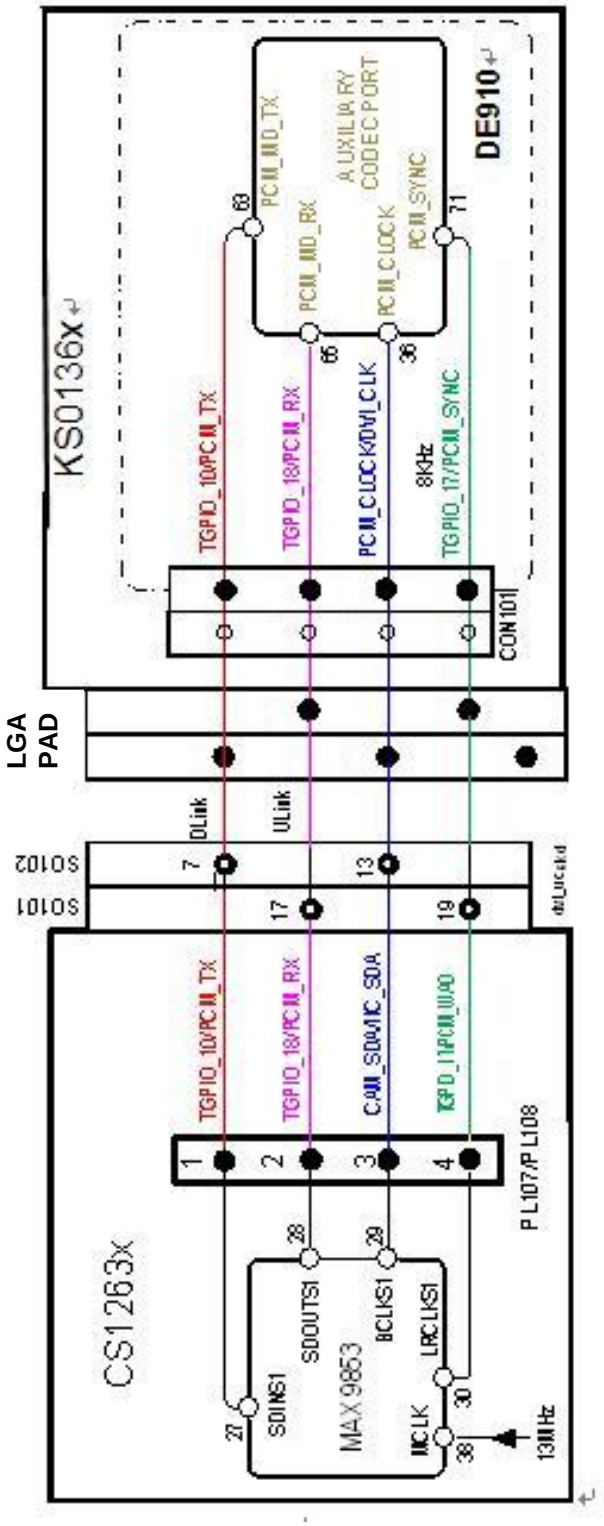


**Figure 14. Block diagram of DVI signal routing to/from MAX9853**

## 7.3 Codec and DVI settings

Speaker and microphone are connected to the external output input lines of the codec.
MAX9853 is configured by a script file, sent by a modem like Procomm® or Hyperlink®.
Every block defines some parameters to load:

- amplifiers gain
- signal mixing
- operating mode
- any other information needed

### 7.3.1 First step DVI signals routing

The DVI useful signals are routed to the assigned pin of the module.
Refer to the Telit module's HW User Guide for all information on the used DVI signals.

- DVI_TX, DVI_RX, DVI_WA0 and DVI_CLK

### 7.3.2 Second step DVI configuration

- Clock rate =2.048 MHz
- PCM decoder padding on
- decoder linear
- PCM encoder padding on
- Encoder linear

*strfmt command1 "AT#DVICFG=1,1,2,1,2^M"*

### 7.3.3 Third step MAX9853 configuration

| Register address | Data | Description |
|---|---|---|
| **1a** | **d5** | **charge pump on to ext osc** |
| **1b** | **02** | **DAC_ADC disabled** |
| **04** | **20** | **INTRF1 Codec slave mode, clock polarity** |
| **05** | **00** | S2SDI serial INTRF1 off |
| **07** | **70** | digital filter default |
| **08** | **20** | digital mixer LEFT RIGHT on |
| **0a** | **22** | Left ADC IN Mixer Active |

 

| | | |
|---|---|---|
| **0b** | **10** | Sidetone off INTRF1 active |
| **0c** | **00** | dig audio INTRF1 max gain=0dB |
| **0e** | **1f** | min LINE1 in gain -32dB |
| **0f** | **1f** | min LINE2 in gain -32dB |
| **10** | **20** | Mic L gain +20dB +20dB |
| **12** | **06** | on bias L MIC EXT |
| **13** | **1f** | SIDETONE gain -32dB |
| **14** | **00** | L Amplifier= +6dB |
| **15** | **3f** | R Amplifier Mute |
| **16** | **7f** | L-Speaker LineOut mute |
| **17** | **3f** | R-Speaker LineOut mute |
| **18** | **07** | RECEIVER Speaker mode On |
| **1a** | **f5** | shut down off |
| **1b** | **a2** | Left DAC_ADC enabled |
| **03** | **ca** | S1SDI serial INTRF1 on mono voice 8KHz |

**Table 4. MAX9853 register and data table**

### 7.3.4 Last step DVI Activation and clock mode setting

- enable DVI; audio is forwarded to the DVI block
- DVI port 2 will be used
- clock mode DVI master

*strfmt command1 "AT#DVI=1,2,1^M"*

## 7.4 Results

Under the following constraints :

External Codec Mic input = 5mVrms
BSS AF input = 680mVrms
Downlink PCM gain = 0dB (AT#PCMRXG=0)
Uplink PCM gain = 0dB (AT#PCMTXG=0)

the performance of the UE/HE910V2_DE/CE910_HE920, connected to MAX9853 through the ***DVI*** are the same that in ***Analog Voice mode***, that is :

Ear Output=170mV$_{rms}$
MonSpeech Output=3580mV$_{rms}$