WL865E4-P Wi-Fi/BLE Module HW User Guide

1VV0301580 Rev. 7 – 2019-11-08

TELIT TECHNICAL DOCUMENTATION

[01.2017]

Mod. 0805 2017-01 Rev.6

SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE

NOTICE

While reasonable efforts have been made to assure the accuracy of this document, Telit assumes no liability resulting from any inaccuracies or omissions in this document, or from use of the information obtained herein. The information in this document has been carefully checked and is believed to be reliable. However, no responsibility is assumed for inaccuracies or omissions. Telit reserves the right to make changes to any products described herein and reserves the right to revise this document and to make changes from time to time in content hereof with no obligation to notify any person of revisions or changes. Telit does not assume any liability arising out of the application or use of any product, software, or circuit described herein; neither does it convey license under its patent rights or the rights of others.

It is possible that this publication may contain references to, or information about Telit products (machines and programs), programming, or services that are not announced in your country. Such references or information must not be construed to mean that Telit intends to announce such Telit products, programming, or services in your country.

COPYRIGHTS

This instruction manual and the Telit products described in this instruction manual may be, include or describe copyrighted Telit material, such as computer programs stored in semiconductor memories or other media. Laws in the Italy and other countries preserve for Telit and its licensors certain exclusive rights for copyrighted material, including the exclusive right to copy, reproduce in any form, distribute and make derivative works of the copyrighted material. Accordingly, any copyrighted material of Telit and its licensors contained herein or in the Telit products described in this instruction manual may not be copied, reproduced, distributed, merged or modified in any manner without the express written permission of Telit. Furthermore, the purchase of Telit products shall not be deemed to grant either directly or by implication, estoppel, or otherwise, any license under the copyrights, patents or patent applications of Telit, as arises by operation of law in the sale of a product.

COMPUTER SOFTWARE COPYRIGHTS

The Telit and 3rd Party supplied Software (SW) products described in this instruction manual may include copyrighted Telit and other 3rd Party supplied computer programs stored in semiconductor memories or other media. Laws in the Italy and other countries preserve for Telit and other 3rd Party supplied SW certain exclusive rights for copyrighted computer programs, including the exclusive right to copy or reproduce in any form the copyrighted computer program. Accordingly, any copyrighted Telit or other 3rd Party supplied SW computer programs contained in the Telit products described in this instruction manual may not be copied (reverse engineered) or reproduced in any manner without the express written permission of Telit or the 3rd Party SW supplier. Furthermore, the purchase of Telit products shall not be deemed to grant either directly or by implication, estoppel, or otherwise, any license under the copyrights, patents or patent applications of Telit or other 3rd Party supplied SW, except for the normal non-exclusive, royalty free license to use that arises by operation of law in the sale of a product.

USAGE AND DISCLOSURE RESTRICTIONS

I. License Agreements

The software described in this document is the property of Telit and its licensors. It is furnished by express license agreement only and may be used only in accordance with the terms of such an agreement.

II. Copyrighted Materials

Software and documentation are copyrighted materials. Making unauthorized copies is prohibited by law. No part of the software or documentation may be reproduced, transmitted, transcribed, stored in a retrieval system, or translated into any language or computer language, in any form or by any means, without prior written permission of Telit

III. High Risk Materials

Components, units, or third-party products used in the product described herein are NOT fault-tolerant and are NOT designed, manufactured, or intended for use as on-line control equipment in the following hazardous environments requiring fail-safe controls: the operation of Nuclear Facilities, Aircraft Navigation or Aircraft Communication Systems, Air Traffic Control, Life Support, or Weapons Systems (High Risk Activities"). Telit and its supplier(s) specifically disclaim any expressed or implied warranty of fitness for such High Risk Activities.

IV. Trademarks

TELIT and the Stylized T Logo are registered in Trademark Office. All other product or service names are the property of their respective owners.

V. Third Party Rights

The software may include Third Party Right software. In this case you agree to comply with all terms and conditions imposed on you in respect of such separate software. In addition to Third Party Terms, the disclaimer of warranty and limitation of liability provisions in this License shall apply to the Third Party Right software.

TELIT HEREBY DISCLAIMS ANY AND ALL WARRANTIES EXPRESS OR IMPLIED FROM ANY THIRD PARTIES REGARDING ANY SEPARATE FILES, ANY THIRD PARTY MATERIALS INCLUDED IN THE SOFTWARE, ANY THIRD PARTY MATERIALS FROM WHICH THE SOFTWARE IS DERIVED (COLLECTIVELY “OTHER CODE”), AND THE USE OF ANY OR ALL THE OTHER CODE IN CONNECTION WITH THE SOFTWARE, INCLUDING (WITHOUT LIMITATION) ANY WARRANTIES OF SATISFACTORY QUALITY OR FITNESS FOR A PARTICULAR PURPOSE.

NO THIRD PARTY LICENSORS OF OTHER CODE SHALL HAVE ANY LIABILITY FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING WITHOUT LIMITATION LOST PROFITS), HOWEVER CAUSED AND WHETHER MADE UNDER CONTRACT, TORT OR OTHER LEGAL THEORY, ARISING IN ANY WAY OUT OF THE USE OR DISTRIBUTION OF THE OTHER CODE OR THE EXERCISE OF ANY RIGHTS GRANTED UNDER EITHER OR BOTH THIS LICENSE AND THE LEGAL TERMS APPLICABLE TO ANY SEPARATE FILES, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

APPLICABILITY TABLE

PRODUCTS

- WL865E4-P

Contents

NOTICE **2**

COPYRIGHTS **2**

COMPUTER SOFTWARE COPYRIGHTS **2**

USAGE AND DISCLOSURE RESTRICTIONS **3**

CONTENTS **5**

1. INTRODUCTION **9**

1.1. Scope 9

1.2. Audience 9

1.3. Contact Information, Support 9

1.4. Text Conventions 10

1.5. Related Documents 11

2. PRODUCT DESCRIPTION **12**

2.1. Overview 12

2.2. Main Features 12

2.3. Block Diagram 13

3. PINS ALLOCATION **14**

3.1. Pin-out Table 14

3.2. Pads Layout 19

4. POWER SUPPLY **20**

4.1. Power Supply Requirements 20

4.2. Power Consumption 20

4.2.1. Power Consumption vs Tx Power at 2.4 GHz Band 21

4.2.2. Power Consumption vs Tx Power at 5 GHz Band 22

4.3. General Design Rules 23

5. DIGITAL SPECIFICATIONS **24**

5.1. Logic Levels 24

5.2. Power Up/Down Sequence 25

5.2.1. Power-on Reset Timing 25

5.3. Unconditional Shutdown 26

5.4. Peripherals Interface Summary 26

5.5. Communication Ports 27
5.5.1. High-Speed UART 27
5.5.2. Low-Speed UART 27
5.5.3. SDIO 28
5.5.4. SPI 28
5.5.5. I2C 28
5.5.6. USB 28
5.5.6.1. Bootloader 28
5.5.7. JTAG 28
5.6. General Purpose I/O 29
5.7. ADC Converter 31
5.8. General Digital Interface Recommendations 31
6. RF SPECIFICATIONS 32
6.1. Bands Variants 32
6.1.1. Supported Frequency Bands 32
6.1.1.1. Wi-Fi 32
6.1.1.2. Bluetooth 32
6.2. Tx Output Power 33
6.2.1. Wi-Fi 33
6.2.1.1. 2.4GHz 33
6.2.1.2. 5GHz 34
6.2.2. Bluetooth 34
6.3. Rx Sensitivity 35
6.3.1. Wi-Fi 35
6.3.1.1. 2.4GHz 35
6.3.1.2. 5GHz 36
6.3.2. Bluetooth 36
7. DESIGN GUIDELINES 37
7.1. PCB Design Guidelines 37
7.2. RF PCB Design Guidelines 39
7.2.1. Wi-Fi/BLE Antenna Requirements 39
7.2.2. RF Design Guidelines 40
8. AUDIO SPECIFICATIONS 43
8.1. Electrical Characteristics 43
9. MECHANICAL DESIGN 44

9.1. Mechanical Dimensions 44
9.2. Mechanical Drawing 44
9.2.1. Top View 44
9.2.2. Bottom View 45
9.2.3. Side View 46
10. APPLICATION PCB DESIGN 47
10.1. PCB Footprint 47
10.2. PCB Pad Design 47
10.3. PCB Pad Dimensions 48
10.4. Stencil 48
10.5. Solder Paste 48
10.6. Solder Reflow 49
11. PACKAGING 51
11.1. Tray 51
11.2. Moisture Sensitivity 52
12. CONFORMITY ASSESSMENT ISSUES 53
12.1. European Directive 2014/53/EU 53
12.2. FCC/IC Compliance 53
13. SAFETY RECOMMENDATIONS 57
13.1. Read Carefully 57
14. ACRONYMS 58
15. DOCUMENT HISTORY 60

FIGURE LIST

Figure 2-1 WL865E4-P Block Diagram 13
Figure 3-1 Pad Layout (Top View) 19
Figure 4-1 EMI Suppression on Modem's Power Supply 23
Figure 5-1 Power Sequence 25
Figure 7-1 Layout Example for FAST Digital Lines 39
Figure 7-2 Minimal RF Matching Network Circuitry 39
Figure 7-3 Coplanar Waveguide Dimensioning Example 41
Figure 7-4 Coplanar Waveguide Calculation Tool Example 41
Figure 7-5 RF Track on EVB 42

Figure 9-1 WL865E4-P Module - Top View 44
Figure 9-2 WL865E4-P Module - Bottom View 45
Figure 9-3 WL865E4-P Module - Side View 46
Figure 10-1 WL865E4-P Recommended Footprint 47
Figure 10-2 SMD and NSMD Pad 47
Figure 10-3 Inhibit Area for not Solder Covered Vias 48
Figure 10-4 Solder Reflow Profile 49
Figure 11-1 WL865E4-P Packaging 51

TABLE LIST

Table 3-1 Pinout Table 18
Table 4-1 Power Supply Requirements 20
Table 4-2 General Power Consumption Table 21
Table 4-3 Tx Power Consumption @ 2.4 GHz 22
Table 4-4 Tx Power Consumption @ 5GHz 22
Table 5-1 IO Levels 24
Table 5-2 Power on Reset 25
Table 5-3 Peripherals Interface Summary 26
Table 5-4 WL865E4-P High-Speed UART Configurations 27
Table 5-5 WL865E4-P Low-Speed UART Configurations 27
Table 5-6 GPIO Alternate Function 30
Table 6-1 Frequency Bands Supported for Wi-Fi 32
Table 6-2 Frequency Bands Supported for BLE 32
Table 6-3 IEEE 802.11 EVM @2.4GHz 33
Table 6-4 IEEE 802.11 EVM @5GHz 34
Table 6-5 BLE Transmit Power 34
Table 6-6 Wi-Fi 2.4G Sensitivity at RF Output Pad 35
Table 6-7 Wi-Fi 5G Sensitivity at RF Output Pad 36
Table 6-8 BLE Sensitivity at RF Output Pad 36
Table 10-1 PCB Finishing Recommendation 48
Table 10-2 Recommended Solder Paste Type 48
Table 10-3 Solder Reflow Table 49

1. INTRODUCTION

1.1. Scope

The purpose of this document is to provide product information and hardware design guidelines for the Telit WL865E4-P Wi-Fi/BLE module.

1.2. Audience

This document is intended for Telit customers, who are integrators, about to implement their applications using our WL865E4-P modules.

1.3. Contact Information, Support

For general contact, technical support services, technical questions and report documentation errors contact Telit Technical Support at:

- TS-EMEA@telit.com
- TS-AMERICAS@telit.com
- TS-APAC@telit.com
- TS-SRD@telit.com

Alternatively, use:

https://www.telit.com/contact-us/

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

http://www.telit.com

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

1.4. Text Conventions

Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. 2019-01-28.

1.5. Related Documents

- WL865E4-P AT Command Reference Guide
- WL865E4-P EVB HW User Guide
- WL865E4-P PCB Antenna Integration Application Note

2. PRODUCT DESCRIPTION

2.1. Overview

The WL865E4-P module is a fully integrated dual-band (2.4 GHz/5.0 GHz), dual-mode, combo Wi-Fi (802.11 a/b/g/n) / Bluetooth Low Energy (BLE) 5.0 module, that provides an easy and cost-effective way for the users to add wireless connectivity to their products.

NOTE:

(EN) The integration of the WL865E4-P module within user application shall be done according to the design rules described in this manual.

(IT) L'integrazione del modulo cellulare WL865E4-P all'interno dell'applicazione dell'utente dovrà rispettare le indicazioni progettuali descritte in questo manuale.

(DE) Die Integration des WL865E4-P Mobilfunk-Moduls in ein Gerät muß gemäß der in diesem Dokument beschriebenen Kunstruktionsregeln erfolgen.

(SL) Integracija WL865E4-P modula v uporabniški aplikaciji bo morala upoštevati projektna navodila, opisana v tem priročniku.

(SP) La utilización del modulo WL865E4-P debe ser conforme a los usos para los cuales ha sido deseñado descritos en este manual del usuario.

(FR) L'intégration du module cellulaire WL865E4-P dans l'application de l'utilisateur sera faite selon les règles de conception décrites dans ce manuel.

(HE) האינטגרטור מתבקש ליישם את ההנחיות המפורטות במסמך זה בתהליך האינטגרציה של המודם הסלולרי WL865E4 עם המוצר.

2.2. Main Features

- Dedicated CPU for IoT applications, an Arm Cortex-M4F @ up to 128MHz with 300KB of RAM reserved
- Dedicated Arm Cortex-M0 processor for Bluetooth LE LC, network stack and Ten silica Xtensa for Wi-Fi (802.11 a/b/g/n) stack with isolated memory, RAM and ROM
- Selectable I/O voltage range from 1.8V to 3.3V
- Possible single 3.3V power source
- Supports up to 10 Access-Point Stations and offers low-power consumption

- Advanced hardware-based security featuring secure boot, trusted execution environment, encrypted storage, key provisioning, and wireless protocol security
- Comprehensive set of peripherals and interfaces: SPI, UART, PWM, I2S, I2C, SDIO, ADC, and GPIOs.

2.3. Block Diagram

Figure 2-1 shows a detailed block diagram of the WL865E4-P module.

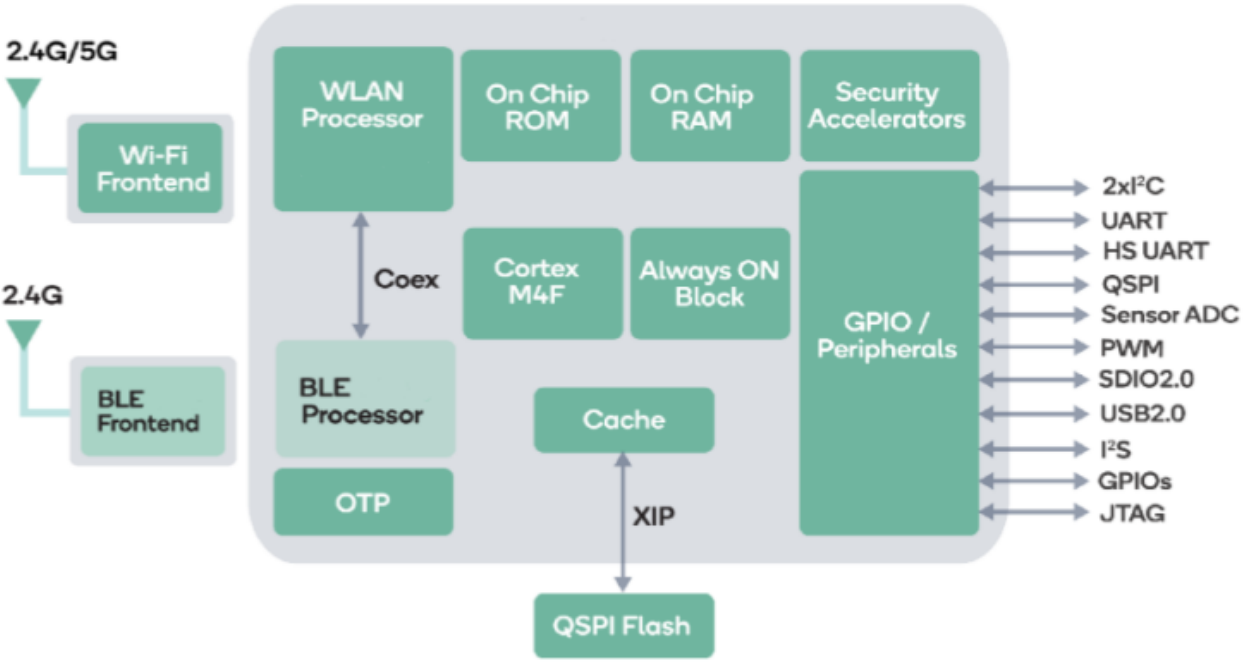

Figure 2-1 WL865E4-P Block Diagram

3. PINS ALLOCATION

3.1. Pin-out Table

Pin	Signal	I/O	Function	Power Bank	Comment
Power Supply					
6	**VDD_WLAN**	I	Wi-Fi Power Supply	Power Net	(3.0V to 3.6V) 3.3V Nominal Power Supply
9	**VDD_VIO**	I	GPIO Power Supply	Power Net	(1.8V to 3.6V) 3.3V Nominal Power Supply
11	**VDD_BLE**	I	BLE Power Supply	Power Net	(3.0V to 3.6V) 3.3V Nominal Power Supply
USB HS 2.0 Communication Port					
12	VUSB	I	USB Power Supply	Power Net	Connect to VDD_BLE
13	USB_D-	I/O	USB Differential Data -	Analog	Used only for programming and testing
14	USB_D+	I/O	USB Differential Data +	Analog	Used only for programming and testing
High-Speed Asynchronous Serial Port (USIF0)					
23	UART0_CTS GPIO_22	I	UART0 FLOW CTRL	VDD_VIO	Baud Rate 115200 - 3Mbps
24	UART0_RTS GPIO_23	O	UART0 FLOW CTRL	VDD_VIO	Baud Rate 115200 - 3Mbps
25	UART0_RXD GPIO_24	I	UART0	VDD_VIO	Baud Rate 115200 - 3Mbps
26	UART0_TXD GPIO_25	O	UART0	VDD_VIO	Baud Rate 115200 - 3Mbps

Low-Speed Asynchronous Serial Port (USIF1)					
27	UART1_RXD GPIO_26	I	UART1	VDD_VIO	Baud Rate 19200 - 115200
28	UART1_TXD GPIO_27	O	UART1	VDD_VIO	Baud Rate 19200 - 115200
Serial Peripheral Interface (SPI)					
53	SPI_M_CS GPIO_11	I/O	SPI Chip Select (Master) (Active LOW)	VDD_VIO	
54	SPI_M_CLK GPIO_12	I/O	SPI Clock (Master)	VDD_VIO	
55	SPI_M_MISO GPIO_14	I/O	SPI MISO (Master)	VDD_VIO	
56	SPI_M_MOSI GPIO_13	I/O	SPI MOSI (Master)	VDD_VIO	
Secure Digital Input Output (SDIO)					
46	SDIO_CLK / SPI_S_CLK GPIO_32	I/O	SDIO Clock SPI Clock (Slave)	VDD_VIO	PWM_6
47	SDIO_CMD / SPI_S_CS GPIO_33	I/O	SDIO Command SPI Chip Select (Slave) (Active LOW)	VDD_VIO	PWM_1
48	SDIO_D3 / SPI_S_MOSI GPIO_34	I/O	SDIO DATA[3] SPI MOSI (Slave)	VDD_VIO	PWM_5
49	SDIO_D2 / USB_BOOT GPIO_35	I/O	SDIO DATA[2] ENTER in BOOT Mode at Start Up, if HIGH.	VDD_VIO	PWM_3
50	SDIO_D1 GPIO_36	I/O	SDIO DATA[1]	VDD_VIO	PWM_4
51	SDIO_D0 / SPI_S_MISO GPIO_37	I/O	SDIO DATA[0] SPI MISO (Slave)	VDD_VIO	PWM_2

Inter-Integrated Circuit Interface (I2C)					
21	I2C_SDA GPIO_06	I/O	I2C Data (Master)	VDD_VIO	
22	I2C_SCL GPIO_07	I/O	I2C Clock (Master)	VDD_VIO	
Analog Interface (ADC)					
3	ADC_IN3 GPIO_17	I/O	12 BITS 1Mhz	VDD_VIO	In ADC mode, VDD_VIO must be 1V8 only
4	ADC_IN2 GPIO_16	I/O	12 BITS 1Mhz	VDD_VIO	In ADC mode, VDD_VIO must be 1V8 only
5	ADC_IN1 GPIO_15	I/O	12 BITS 1Mhz	VDD_VIO	In ADC mode, VDD_VIO must be 1V8 only
Digital Audio Interface (I2S) Master/Slave					
17	I2S_SYNC GPIO_28	I/O	I2S Frame Sync or LR Clock	VDD_VIO	
18	I2S_SCK GPIO_30	I/O	I2S Bit Clock	VDD_VIO	
19	I2S_SDO GPIO_31	I/O	I2S Data Output	VDD_VIO	
20	I2S_SDI GPIO_29	I/O	I2S Data Input	VDD_VIO	
Miscellaneous Functions					
1	RESET#	I	Hardware RESET Power Disable	VDD_VIO	Open Drain Active LOW
2	BT_PRIORITY GPIO_02	I/O	BT_PRIORITY	VDD_VIO	Co-existence 3-wire PTA
15	PWM_0	I/O	Pulse Width Modulated	VDD_VIO	PWM_0

	GPIO_05				
16	LF_CLK_IN GPIO_08	I/O	Optional Ext 32KHz Clock	VDD_VIO	
33	WIFI_ACTIVE GPIO_03	I/O	WIFI_ACTIVE	VDD_VIO	Co-existence 3-wire PTA
34	BT_ACTIVE GPIO_04	I/O	BT_ACTIVE	VDD_VIO	Co-existence 3-wire PTA
43	WAKEUP GPIO_01	I/O	WAKEUP	VDD_VIO	
44	WoW GPIO_09	I/O	Wake on Wireless LAN Open Drain	VDD_VIO	PWM_7
45	GPIO_10	I/O	GPIO	VDD_VIO	
JTAG Pads					
30	JTAG GPIO_18	I/O	JTAG Application SW Debug	VDD_VIO	
31	JTAG GPIO_19	I/O	JTAG Application SW Debug	VDD_VIO	
29	JTAG GPIO_20	I/O	JTAG Application SW Debug	VDD_VIO	
32	JTAG GPIO_21	I/O	JTAG Application SW Debug	VDD_VIO	
RF Pads					
37	ANT_BLE	I/O	BLE 2.4GHz Antenna	RF	
40	ANT_WIFI	I/O	WIFI 2.4/5GHz Antenna	RF	
Power Supply GND					
7	**GND**	I	Ground	Power Net	
8	**GND**	I	Ground	Power Net	

10	**GND**	I	Ground	Power Net
35	**GND**	I	Ground	Power Net
36	**GND**	I	Ground	Power Net
38	**GND**	I	Ground	Power Net
39	**GND**	I	Ground	Power Net
41	**GND**	I	Ground	Power Net
42	**GND**	I	Ground	Power Net
52	**GND**	I	Ground	Power Net
57	**GND**	I	Ground	Power Net

Table 3-1 Pinout Table

3.2. Pads Layout

Figure 3-1 shows the pads layout configuration for the module (top view)

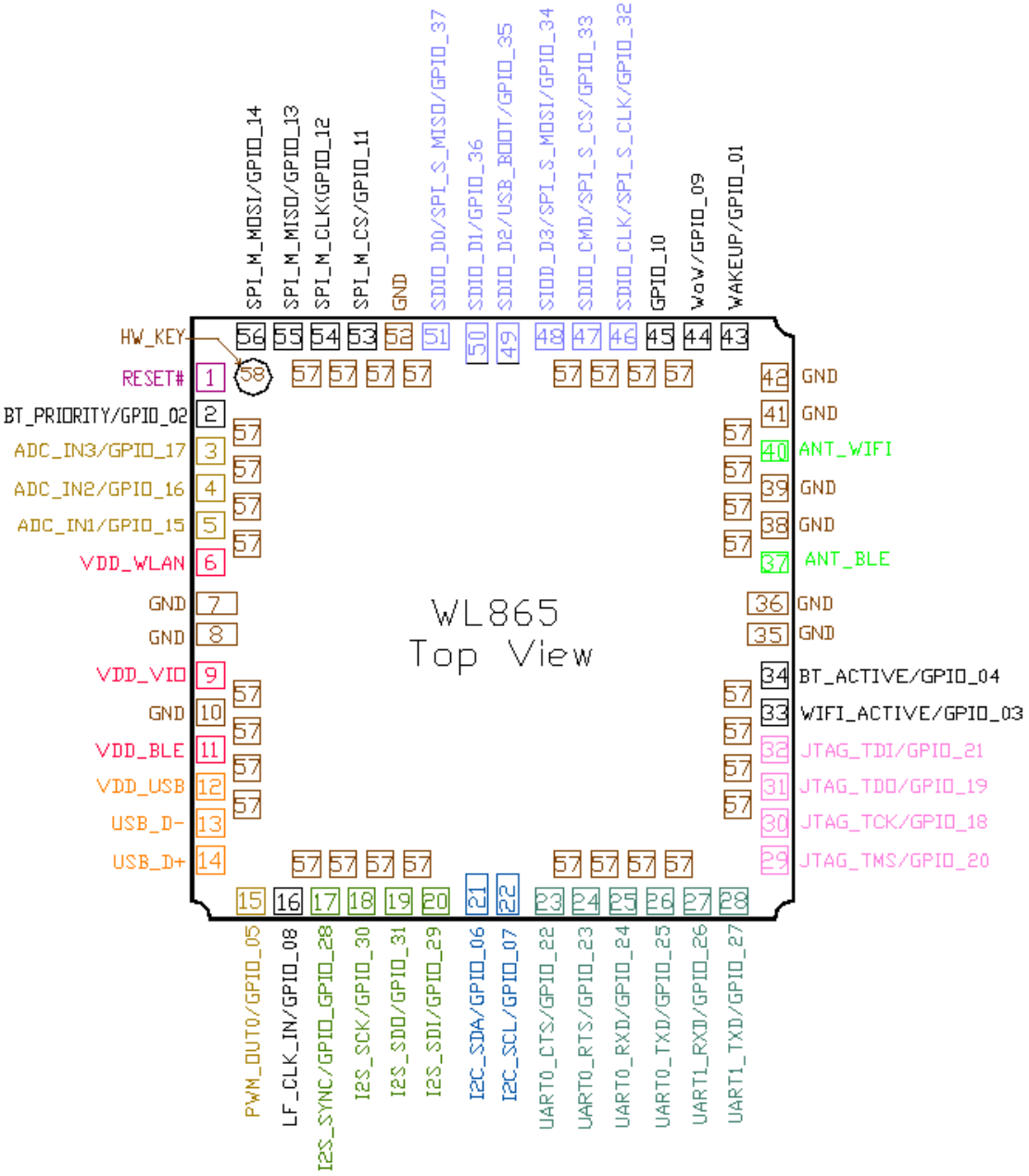

Figure 3-1 Pad Layout (Top View)

4. POWER SUPPLY

4.1. Power Supply Requirements

Power Supply	Minimum	Typical	Maximum
Absolute Maximum to avoid permanent damage. At any power supply pin.	-0.3 V		4.0V
Recommended VDD_BLE, VDD_WLAN, USB_VDD	3.14 V	3.3V	3.46V
Recommended VDD_VIO (see notes)	3.14V or 1.71V	3.3V or 1.8V	3.46V or 1.89V

Table 4-1 Power Supply Requirements

4.2. Power Consumption

Power Consumption	Typical Average
Idle (Radio OFF, UART ON)	5.2mA
Standby (BT MOM, Wi-Fi MOM)	90.44µA
Deep Sleep (Radio OFF)	163µA
Wi-Fi DTIM1 @2.4GHz ch6	2.45mA
Wi-Fi DTIM3 @2.4GHz ch6	1.53mA
Wi-Fi DTIM10 @2.4GHz ch6	1.28mA
Wi-Fi DTIM1 @5GHz ch36	1.96mA
Wi-Fi DTIM3 @5GHz ch36	1.52mA
Wi-Fi DTIM10 @5GHz ch36	1.24mA
BLE Rx	12.84mA
BLE Tx	8.79mA
BLE Connection with 1s and no data transfer	234µA
BLE Scan every 1.2s	330µA
BLE Fast Advertising 60ms	997µA
BLE Slow Advertising 1.2s	251µA

Power Consumption	Typical Average
BLE Beaconing 100ms	702µA
BLE Periodic Wakeup (Slave)	4950µA
BLE Periodic Transfer 1s (Slave)	534µA

Table 4-2 General Power Consumption Table

4.2.1. Power Consumption vs Tx Power at 2.4 GHz Band

RF Test were in conducted and measures related to module's RF Pad.

Wi-Fi 2G4 / CH 6 Standard 802.11x	Modulation	Data Rates	RF Output (dBm)	Current mA@3.3V
b	BPSK	**1 Mbps**	19	339
b	QPSK	**2 Mbps**	19	342
b	CCK	**5.5 Mbps**	19	335
b	CCK	**11 Mbps**	19	328
g	BPSK	**6 Mbps**	19	334
g	BPSK	**9 Mbps**	19	331
g	QPSK	**12 Mbps**	19	328
g	QPSK	**18 Mbps**	18	295
g	16 QAM	**24 Mbps**	18	286
g	16 QAM	**36 Mbps**	18	279
g	64 QAM	**48 Mbps**	16	239
g	64 QAM	**54 Mbps**	15	220
n	BPSK	**MCS0_20**	19	340
n	QPSK	**MCS1_20**	19	335
n	QPSK	**MCS2_20**	19	330

Wi-Fi 2G4 / CH 6 Standard 802.11x	Modulation	Data Rates	RF Output (dBm)	Current mA@3.3V
n	16 QAM	**MCS3_20**	18	294
n	16 QAM	**MCS4_20**	17	264
n	64 QAM	**MCS5_20**	16	238
n	64 QAM	**MCS6_20**	15	219
n	64 QAM	**MCS7_20**	15	209

Table 4-3 Tx Power Consumption @ 2.4 GHz

4.2.2. Power Consumption vs Tx Power at 5 GHz Band

Wi-Fi 5G / CH 100 Standard 802.11x	Modulation	Data Rates	RF Output (dBm)	Current mA@3.3V
a	BPSK	**6 Mbps**	16	293
a	BPSK	**9 Mbps**	16	291
a	QPSK	**12 Mbps**	16	290
a	QPSK	**18 Mbps**	16	288
a	16 QAM	**24 Mbps**	16	283
a	16 QAM	**36 Mbps**	14	248
a	64 QAM	**48 Mbps**	13	234
a	64 QAM	**54 Mbps**	13	232
n	BPSK	**MCS0_20**	16	297
n	QPSK	**MCS1_20**	16	290
n	QPSK	**MCS2_20**	15	274
n	16 QAM	**MCS3_20**	15	267
n	16 QAM	**MCS4_20**	14	252
n	64 QAM	**MCS5_20**	14	249
n	64 QAM	**MCS6_20**	13	236
n	64 QAM	**MCS7_20**	13	235

Table 4-4 Tx Power Consumption @ 5GHz

The equipment must be supplied by an external limited power source in compliance with the clause 2.5 of the standard EN 60950-1.

4.3. General Design Rules

To improve EMI filtering, it is recommended to use an EMI suppression circuitry. Figure 4-1 shows an example circuit with the minimum allowable capacitor values.

To allow capacitor values range up to 330µF, provision must be for C203 and C207 component sizes.

Choose a low ESR (~50 mOhms) for C203 and C207 and make sure to place these capacitors as close as possible to the modems power PADs.

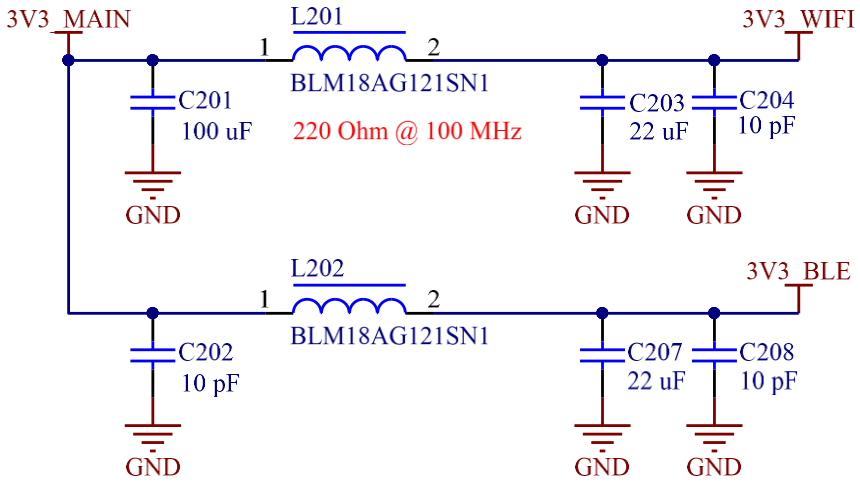

Figure 4-1 EMI Suppression on Modem's Power Supply.

WARNING:

Power Cut may damage modem's memory content.

Use it only when no other option, like RESET or Power Shutdown, is not available.

Read more in section §5.2 and in the *"WL865E4-P AT Command Reference Guide"*.

The Power Net VDD_VIO does not need special EMI Filtering but requires bypass capacitors similar to C203 as shown in Figure 4-1. These bypass capacitors must be placed close to the VDD_IO PAD.

5. DIGITAL SPECIFICATIONS

5.1. Logic Levels

Parameter	Min	Max
Input level on any digital pin	-0.3V	VDD_VIO + 0.3V

Levels with VDD_VIO = 3.3V	Min	Max
V_{IH} Input high level	2.4V	3.6V
V_{IL} Input low level	-0.3V	0.3V
V_{OH} Output high level	3.0V	3.6V
V_{OL} Output low level	-0.3V	0.4V

Levels with VDD_VIO = 3.3V	Typical
I_{IH} Input current	60 µA (Rod is ON) 0.1 µA (Rpd is OFF)
I_{IL} Input current	60 µA (Rod is ON) 0.1 µA (Rpd is OFF)
I_{OH} Output current	5 mA (x4 drive strength) 3.3 mA (x2 drive strength) 2.6 mA (x1 drive strength)
I_{OL} Output current	5 mA (x4 drive strength) 3.3 mA (x2 drive strength) 2.6 mA(x1 drive strength)

Table 5-1 IO Levels

5.2. Power Up/Down Sequence

The RESET# is the main power enable/disable pin, for both Wi-Fi and BLE. All power supplies must be stable for a minimum of 10 µs before RESET# is de-asserted (that is, when greater than VIL for VDD_VIO). If VDD_VIO = 3.3V, then VDD_BLE, VDD_WLAN, and VDD_VIO can share the same 3.3V power.

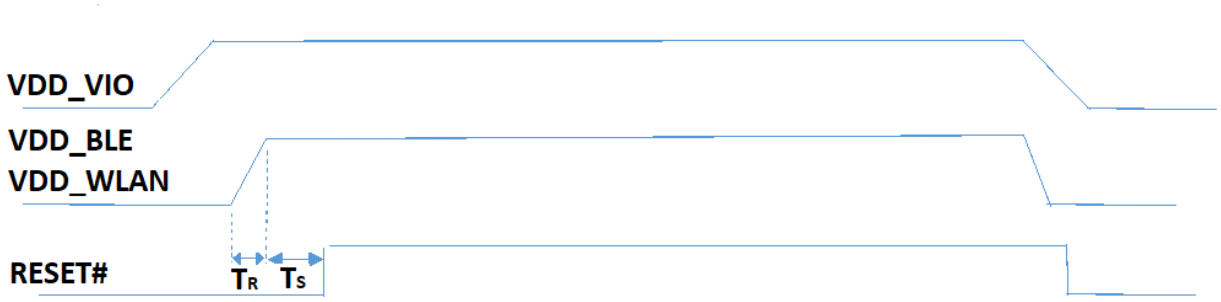

Figure 5-1 Power Sequence

5.2.1. Power-on Reset Timing

Parameter	Description	Min	Max	Unit
T_R	Rise time of the power to 90% of final voltage	N/A	25	ms
T_S	Minimum time before RESET# is de-asserted	10	N/A	µs

Table 5-2 Power on Reset

STOP

WL865E4-P module supports single VIO only.

- Module's power sequence is critical to the design to avoid damage to the internal power management
- If SENSE ADC is used, all VIO must be of 1.8V
- If SENSE ADC is not used, VIO can be either of 1.8V or 3.3V
- If VIO=3.3V, then no power sequence is required.
- If VIO=1.8V, then 1.8V VIO must be Powered ON first before 3.3V, and Power OFF after 3.3V ramping down.

Either add VDD_BLE and VDD_WLAN enabled circuitry, controlled by VDD_VIO or in case of 3V3 only, you can use all three power nets connected.

Due to possible instant current peak sink, each of the three main power nets should be dimensioned to support 1A@3V3.

5.3. Unconditional Shutdown

The RESET# pin is used for performing unconditional Hardware RESET. This function is controlled using an Open-Drain configuration.

The RESET# pin has an internal PU of 120 KOhm.

5.4. Peripherals Interface Summary

The WL865E4-P module supports the following peripherals Interfaces.

Peripherals	Features
QSPI	Internal Serial Flash, 8/64/96MHz
SDIO (Slave) SPI (Slave)	48Mhz clock rate
SPI Master	48Mhz clock rate, 4-wire
USB 2.0	FW upgrade only
I2S (Master / Slave)	One port – 2 audio channels
PCM (Master / Slave)	8/16-bit, 48KHz
I2C (Master)	One I2C interface
UART	One Debug UART up to 115200 bps
High-speed UART	One HS-UART from 115200 bps up to 3 Mbps
ADC	1 ADC, 12-bit, 1M samples/sec, VDD_VIO=1.8V 3-channels single ended or 1 single + 1 differential
PWM	8-channels
Co-existence	PTA 3-wire Master Interface (BT_PRIORITY, WIFI_ACTIVE, BT_ACTIVE)

Table 5-3 Peripherals Interface Summary

5.5. Communication Ports

5.5.1. High-Speed UART

High-Speed Universal Asynchronous Receiver/Transmitter (HS-UART) interfaces, which may be configured to serve as either a host interface link or a debug message console.

Property	WL865E4-P Configuration
Baud rate	115200 bps(default), no auto-baud rate detection, it can be changed by the host to up to 3 Mbps by using AT commands
Data bits	8 bits
Flow control	CTS/RTS
Parity	None
Stop bits	1
Bit order	LSBit first

Table 5-4 WL865E4-P High-Speed UART Configurations

5.5.2. Low-Speed UART

Low-Speed Universal Asynchronous Receiver/Transmitter (UART) interface, which is configured to serve as a debug port

Property	WL865E4-P Configuration
Baud rate	Up to 115200 bps, no auto-baud rate detection, debug port
Data bits	8 bits
Flow control	None
Parity	None
Stop bits	1
Bit order	LSBit first

Table 5-5 WL865E4-P Low-Speed UART Configurations

5.5.3. SDIO

One SDIO Slave interface:

- Compliant to SDIO v2.0 specification
- Interface clock frequency up to 48 MHz
- Data transfer modes: 4-bit SDIO, 1-bit SDIO, SPI

5.5.4. SPI

Two general-purpose SPI interfaces with interface clock frequency up to 48 MHz One SPI is configured as master only and the second SPI can be configured as slave with pin-muxed with SDIO interface pins.

5.5.5. I2C

The I2C Master/Salve interface has weak internal pull-up. If necessary, add external pull-ups (1K to 10K).

5.5.6. USB

The USB 2.0 interface is used only for Bootloader.

The VUSB is of only 3V3 volts. It can be directly connected to VDD_BLE. The USB plug/unplug detection is done through the data pins.

5.5.6.1. Bootloader

The firmware boot up can be performed only through an USB interface.

To put the module into USB-BOOT mode, you need to restart the module (Power cycle/Reset) with SDIO_D2 / USB_BOOT pin HIGH. Once the USB is detected, you can release SDIO_D2 / USB_BOOT high.

The Qualcomm HS-USB QLoader 9008 driver will be automatically installed on our PC.

Use Telit “WL865E4 Loader.exe” for programming the serial flash with your binary through the USB.

To initiate a force USB BOOT Mode, the following Bootstrap signals used for JTAG selection must be LOW:

- UART0_TX,
- SDIO_CLK and,
- SPI0_M_MOSI.

5.5.7. JTAG

To add SW debug capabilities to your design use JTAG.

To enable JTAG, restart the module (Power cycle or Reset) and ensure that the following Bootstrap signals are set as shown below:

- UART0_TX -> LOW
- SDIO_CLK -> LOW
- SPI0_M_MOSI -> HIGH

5.6. General Purpose I/O

The module has 37 GPIO which can be configured as Input, Output or as Alternate Function.

Table 5-6 below lists the GPIO numbers and their alternate functions with direction and Internal PU/PD at startup.

GPIO Number	Alternate Functions	Direction	Internal PU/PD
GPIO_01	WAKEUP	Input	PD
GPIO_02	BT_PRIORITY PTA 3-wires master interface for system Co-existence with external devices.	Input/Output	
GPIO_03	WIFI_ACTIVE PTA 3-wires master interface for system Co-existence with external devices.	Input/Output	
GPIO_04	BT_ACTIVE PTA 3-wires master interface for system Co-existence with external devices.	Input/Output	
GPIO_05	PWM_0	Output	
GPIO_06	I2C_SDA	Input/Output	PU
GPIO_07	I2C_SCL	Output	PU
GPIO_08	LF_CLK_IN external 32KHz for Low Power Accuracy	Input	
GPIO_09	WoW (Wakeup On Wireless) / PWM_7	Input	
GPIO_10	SW_RESET, WHATCH DOG, etc	Input/Output	
GPIO_11	SPI_MASTER_CS	Output	PU
GPIO_12	SPI_MASTER_CLK	Output	PD
GPIO_13	SPI_MASTER_MISO	Input	PU
GPIO_14	SPI_MASTER_MOSI	Output	PU
GPIO_15	ADC_IN1 (ADC only if VDD_VIO=1V8)	Input	
GPIO_16	ADC_IN2 (ADC only if VDD_VIO=1V8)	Input	
GPIO_17	ADC_IN3 (ADC only if VDD_VIO=1V8)	Input	

GPIO Number	Alternate Functions	Direction	Internal PU/PD
GPIO_18	JTAG_TCK	Output	PU
GPIO_19	JTAG_TDO	Output	
GPIO_20	JTAG_TMS	Output	PU
GPIO_21	JTAG_TDI	Input	PU
GPIO_22	UART0_CTS	Input	
GPIO_23	UART0_RTS	Output	
GPIO_24	UART0_RXD	Input	
GPIO_25	UART0_TXD	Output	
GPIO_26	UART1_RXD	Input	PU
GPIO_27	UART1_TXD	Output	PD
GPIO_28	I2S_SYNC	Input/Output	
GPIO_29	I2S_SDI	Input	
GPIO_30	I2S_SCK	Input/Output	
GPIO_31	I2S_SDO	Output	
GPIO_32	SDIO_CLK / SPI_SLAVE_CLK / PWM_6	Input	PD
GPIO_33	SDIO_CMD / SPI_SLAVE_CS / PWM_1	Input	
GPIO_34	SDIO_D3 / SPI_SLAVE_MOSI / PWM_5	Input/Output	PD
GPIO_35	SDIO_D2 / PWM_3	Input/Output	PD
GPIO_36	SDIO_D1 / PWM_4	Input/Output	PD
GPIO_37	SDIO_D0 / SPI_SLAVE_MISO / PWM_2	Input/Output	PD

Table 5-6 GPIO Alternate Function

5.7. ADC Converter

The ADC, as alternate GPIO function, can be used only if VDD_VIO is equal to 1V8.

- 12-bit ADC up to1Msps
- Alternatively, 1 differential input, -1.75V to +1.75V, common mode 0.875V.

5.8. General Digital Interface Recommendations

A voltage translator must be used if components interfacing with Telit components have digital signals with higher I/O interface voltage than the WL865E4-P module.

Using voltage translator components in your design makes the system ready for operation at the full VDD_VIO voltage range, 1.8V to 3V3. However, using resistor divider and/or emitter follower circuits, as voltage translators does not protect the module against latch-up. Furthermore, you cannot guarantee a constant voltage on the divider net.

The use of open collector buffers or bi-directional voltage level translators with unidirectional signals is in principle correct, but they are less immune to RF and are dependent on Pull-Up/Downs that could be present at any side of the voltage translator; some have different power range for both Vcca and Vccb, in some cases you must guarantee Vcca < Vccb, and their OE should be powered only from the Vcca signal. Hence, we recommended unidirectional level shifters; if bi-directional buffers are used, then those designed for PU/PD like TXS, NXS, FXLA and NVT200x are preferred, they work better if strong PU/PD are internally present.

Also, it is recommended to use a dual supply buffer component for unidirectional signals like UART. For example, SN74AVC2T245, SN74AVC4T774 or SN74LVC2T45, for 5V signals. These are more immune to RF and are independent on Pull-Ups or Pull-Downs that could be present at any side of the voltage translator. Place a 33pF capacitor on both power supplies. The Power bank side connected to the module should be powered with the same VDD_VIO to prevent latch-up from happening.

When using level shifters, for better testability, prefer the use of those having OE pins. Test pulling the “EN” lines of the level shifts with the addition of a 10K resistor to GND or VCC, depending on level shifter used. This will create access points that would put shifts in tri-state and can be conveniently used for testing and firmware updates originating from external serial ports such as a PC.

It is recommended to connect the WL865 Reset signal to control the EN pin of the level shifter, this will guarantee tri-state on not necessary pins during BOOT UP activity.

6. RF SPECIFICATIONS

6.1. Bands Variants

WL865E4-P is a dual-band (2.4GHz and 5GHz) module which supports Wi-Fi (802.11 a,b,g and n) as well as BLE 5.0.

DFS operational mode is slave without radar detection

Internal Wi-Fi and BLE Coexistence is guaranteed by the non-use of multi-transmission task.

To take care of external coexistence, 3-wire PTA is present for this scope.

6.1.1. Supported Frequency Bands

6.1.1.1. Wi-Fi

Technology	Frequency Range (GHz)	Channel Spacing (MHz)
Wi-Fi 2.4 GHz	2.401 ≤ Fc ≤ 2.495	5
Wi-Fi 5 GHz	5.170 ≤ Fc ≤ 5.835	5

Table 6-1 Frequency Bands Supported for Wi-Fi

6.1.1.2. Bluetooth

Technology	Frequency Range (GHz)	Channel Number (k)
BLE 5	2.402 ≤ Fc ≤ 2.480	Fc=2402 + k × 2 MHz, where k = 0, ..., 39

Table 6-2 Frequency Bands Supported for BLE

6.2. Tx Output Power

6.2.1. Wi-Fi

6.2.1.1. 2.4GHz

Wi-Fi 2G4 Transmit power with IEEE 802.11 EVM and spectral mask compliance at RF output pad at 25 °C.

Wi-Fi 2G4 / CH 6 Standard 802.11x	Modulation	Data Rates	RF Output (dBm)	EVM (dB)	IEEE EVM Limit (dB)
b	BPSK	**1 Mbps**	19	-30,4	-14
b	QPSK	**2 Mbps**	19	-25,6	-14
b	CCK	**5.5 Mbps**	19	-27,5	-14
b	CCK	**11 Mbps**	19	-26,5	-14
g	BPSK	**6 Mbps**	19	-15,4	-5
g	BPSK	**9 Mbps**	19	-15,3	-8
g	QPSK	**12 Mbps**	19	-15	-10
g	QPSK	**18 Mbps**	18	-15,7	-13
g	16 QAM	**24 Mbps**	18	-19,3	-16
g	16 QAM	**36 Mbps**	18	-19,8	-19
g	64 QAM	**48 Mbps**	16	-23,5	-22
g	64 QAM	**54 Mbps**	15	-27	-25
n	BPSK	**MCS0_20**	19	-14,7	-5
n	QPSK	**MCS1_20**	19	-14,3	-10
n	QPSK	**MCS2_20**	19	-14,4	-13
n	16 QAM	**MCS3_20**	18	-19,2	-16
n	16 QAM	**MCS4_20**	17	-21	-19
n	64 QAM	**MCS5_20**	16	-24	-22
n	64 QAM	**MCS6_20**	15	-27	-25
n	64 QAM	**MCS7_20**	15	-28,6	-27

Table 6-3 IEEE 802.11 EVM @2.4GHz

6.2.1.2. 5GHz

Wi-Fi 5G transmit power with IEEE 802.11 EVM and spectral mask compliance at RF output pad at 25 °C.

Wi-Fi 5G / CH 100 Standard 802.11x	Modulation	Data Rates	RF Output (dBm)	EVM (dB)	IEEE EVM Limit (dB)
a	BPSK	**6 Mbps**	16	-17	-5
a	BPSK	**9 Mbps**	16	-17	-8
a	QPSK	**12 Mbps**	16	-16,8	-10
a	QPSK	**18 Mbps**	16	-16,7	-13
a	16 QAM	**24 Mbps**	16	-22.6	-16
a	16 QAM	**36 Mbps**	14	-26,5	-19
a	64 QAM	**48 Mbps**	13	-28	-22
a	64 QAM	**54 Mbps**	13	-28	-25
n	BPSK	**MCS0_20**	16	-16,4	-5
n	QPSK	**MCS1_20**	16	-16,2	-10
n	QPSK	**MCS2_20**	15	-16,8	-13
n	16 QAM	**MCS3_20**	15	-25,2	-16
n	16 QAM	**MCS4_20**	14	-27	-19
n	64 QAM	**MCS5_20**	14	-28,6	-22
n	64 QAM	**MCS6_20**	13	-28	-25
n	64 QAM	**MCS7_20**	13	-28	-27

Table 6-4 IEEE 802.11 EVM @5GHz

6.2.2. Bluetooth

BLE transmit power with at RF output Pad at 25 °C. Current consumption 19,4 mA

Packet Type	Channel Number	Output Power (dBm)
LE 1M	1	1,9
LE 2M	1	1,76

Table 6-5 BLE Transmit Power

6.3. Rx Sensitivity

6.3.1. Wi-Fi

6.3.1.1. 2.4GHz

Wi-Fi 2G4 Rx sensitivity tested at RF output pad at 25 °C.

Wi-Fi 2G4 / CH 6 Standard 802.11x	Modulation	Data Rates	Sensitivity (dBm)	IEEE EVM Limit (dB)
b	BPSK	**1 Mbps**	-94,8	-80
b	QPSK	**2 Mbps**	-92,4	-80
b	CCK	**5.5 Mbps**	-92,3	-76
b	CCK	**11 Mbps**	-88,4	-76
g	BPSK	**6 Mbps**	-92,6	-82
g	BPSK	**9 Mbps**	-91,6	-81
g	QPSK	**12 Mbps**	-90,9	-79
g	QPSK	**18 Mbps**	-88,3	-77
g	16 QAM	**24 Mbps**	-85,1	-74
g	16 QAM	**36 Mbps**	-81,5	-70
g	64 QAM	**48 Mbps**	-77,3	-66
g	64 QAM	**54 Mbps**	-76,1	-65
n	BPSK	**MCS0_20**	-92,6	-82
n	QPSK	**MCS1_20**	-90,3	-79
n	QPSK	**MCS2_20**	-88,1	-77
n	16 QAM	**MCS3_20**	-83,5	-74
n	16 QAM	**MCS4_20**	-80,1	-70
n	64 QAM	**MCS5_20**	-76,1	-66
n	64 QAM	**MCS6_20**	-74,4	-65
n	64 QAM	**MCS7_20**	-72,5	-64

Table 6-6 Wi-Fi 2.4G Sensitivity at RF Output Pad

6.3.1.2. 5GHz

Wi-Fi 5G Rx sensitivity tested at RF output pad at 25 °C.

Wi-Fi 5G / CH 100 Standard 802.11x	Modulation	Data Rates	Sensitivity (dBm)	IEEE EVM Limit (dBm)
a	BPSK	**6 Mbps**	-92,1	-82
a	BPSK	**9 Mbps**	-90,8	-81
a	QPSK	**12 Mbps**	-89,3	-79
a	QPSK	**18 Mbps**	-87,1	-77
a	16 QAM	**24 Mbps**	-83,4	-74
a	16 QAM	**36 Mbps**	-80,3	-70
a	64 QAM	**48 Mbps**	-76,2	-66
a	64 QAM	**54 Mbps**	-74,7	-65
n	BPSK	**MCS0_20**	-91,6	-82
n	QPSK	**MCS1_20**	-88,9	-79
n	QPSK	**MCS2_20**	-86,6	-77
n	16 QAM	**MCS3_20**	-82,1	-74
n	16 QAM	**MCS4_20**	-78,7	-70
n	64 QAM	**MCS5_20**	-74,8	-66
n	64 QAM	**MCS6_20**	-73,1	-65
n	64 QAM	**MCS7_20**	-71,7	-64

Table 6-7 Wi-Fi 5G Sensitivity at RF Output Pad

6.3.2. Bluetooth

Rx sensitivity tested at RF output pad at 25 °C. Current consumption 21,6 mA.

Packet Type	Channel Number	Rx Sensitivity (dBm)
LE 1M	1	-97.1
LE 2M	1	-89

Table 6-8 BLE Sensitivity at RF Output Pad

7. DESIGN GUIDELINES

To avoid harmonics, provisions must be made on the module and on any other board connected, close to it, of filtering capacitors to GND, placed very close to the component and on its same path and layer, in the following cases only if those components are not shielded:

- Power Sources and signals on input-output connectors
- At power supply output PADs
- At component's power supply input PADs (even if shielded)
- Diodes in forward conduction, like LEDs, on anode and/or cathodes if not directly tied to a power net
- Transistor bases, mainly for bipolar ones, phototransistors and opto-isolator
- At analog microphone pads
- At Operational Amplifiers Inputs and supplies.

Select capacitors that have their self-resonant frequency similar to the frequency generated on your board or on boards close to your board.

For example, to effectively filter the Wi-Fi RF bands, these small signal capacitors must be self-resonant (SRF) at about 2.4 and 5.5GHz. Example capacitor values, depending on manufacture and its mechanical dimensions should be around 1pF to 10pF.

The coexistence between BT and Wi-Fi 2.4GHz and the LTE band 7 and 41 is critical.
A coexistence mechanism done in the application's software is necessary.

7.1. PCB Design Guidelines

The GND of the PCB or RF Chip antenna is part of antenna when using a monopole, especially the part that lies in front of the monopole. Leave a wide ground area, without components and tracks, in front of antenna on all layers. In the inner layers, the width could be less. 5mm is an optimum value but not always reachable.

If the antenna is placed directly on the board, leave a wide ground area for it.

The position of the external antenna with respect to other boards is very important. Because the conductive planes close to the antenna will modify the impedance seen by the antenna. Any board associated to the system must be RF proof.

Move the components, tracks, vias, and connectors away from the antenna area to reduce their coupling with RF signal; you can also bury tracks in the inner layers of a multi-layer PCB.

Since, components and PCBs are getting smaller while component's density increases, another problem that becomes important is the heat dissipation. For that reason, pay special attention to the PCB stack up and component placement. The following PCB design rules will help RF immunity and improve heat dissipation.

- Use at least a six layers PCB technology.
- Layer2 and Layer4 should be mainly ground.
- On top of Layer1 and at the bottom of Layer6, place mainly ground plane interrupted just by component pads and RF antenna tracks. Minimum tracks connecting Layer3 to Layer5. This is done to avoid ground interruption and its heat dissipation.

- Use Layer3 and Layer5 only for signals, where power lines are wider tracks and surrounded by ground to reduce the risk of crosstalk with other signals.
- Use one layer for horizontal lines only, and the another one for vertical lines. Fill the remaining empty space with ground.
- Use several vias to connect all ground planes and areas in all layers with possible through hole drills.
- Place warmer components on the PCB side facing up and do not place anything near them, leaving space for air.
- If it is a closed application, consider opening holes on top and bottom of the cover for ventilation

The design can be done in 4 layers only, if the number of interconnection gives you the possibility to route them on layer2 and layer3 in a way that power lines and signals lines do not intersect, and the module is operating continuously so the heat dissipation is not a must. All the rest suggestion described above must be fulfilling. The audio, USB, and ADC lines must be routed avoiding intersection with any other signal.

Top and Bottom layers should be mainly a ground plane interrupted just by component's pads, vias and RF tracks. Connect all ground areas avoiding isolated island with several vias. In this way, the signal tracks are more protected from picking up RF due to the Faraday-Cage effect. Long exposed tracks can easily pick-up RF power and especially in your case with many RF power sources you can generate high frequency intermodulation harmonics that the same exposed tracks can then irradiate very efficiently.

All the PCB borders should be ground in all layers and also fill all the free space in internal planes with ground. All the ground, either planes or areas, must be well interconnected, with a fence of GND vias one each 2mm, to guarantee a strong equipotential node. Avoid unconnected copper islands and signal or vias on PCB border.

Power tracks should face only ground tracks or planes. Power lines should not run externally and/or side by side with other signal lines, place ground in between. Power lines should not have signal lines running or crossing under them, place ground plane area under and above all its path.

The Bypass capacitors must be placed close to Telit module's power input pads or at least on the same path. In case of switching power supply another Bypass low ESR capacitor must be placed close to the inductor output to reduce the ripple.

Some protection diode must be placed close to the input connector where the power source is drained.

It is not advisable to route analog or digital audio lines, memory address and data bus, fast digital signals like SPI or SDIO, clocks, quartz, serial and long signal tracks on an outer layer. It'll be better to bury it on an inner layer with a ground plane under and above it to shield the signal from RF and crosstalk, see figure below.

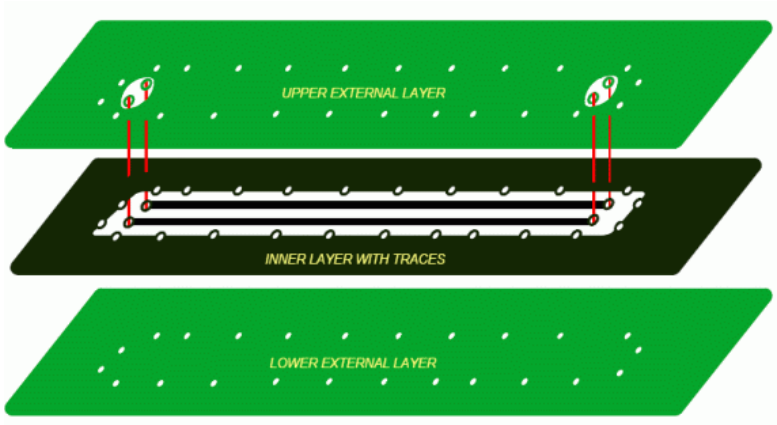

Figure 7-1 Layout Example for FAST Digital Lines

7.2. RF PCB Design Guidelines

7.2.1. Wi-Fi/BLE Antenna Requirements

Special care must be taken during the design of the RF section on the application board.

RF performance degradation, and infringements of emission limits, may arise if the following recommendations are not respected.

Telit's WL865E4-P interface features an SMA connector for an external antenna of 50 Ω impedance, but other antenna integrated choices are possible, such as a chip or a printed one. In case an integrated antenna is used, it is recommended to place it at the edge of the application board.

To tune the antenna impedance to 50Ω, it is recommended to foresee a PI matching network between the WL865E4-P and the antenna during first prototyping. If not required you can also use a series 0Ω-resistor, leaving the two shunt components unpopulated.

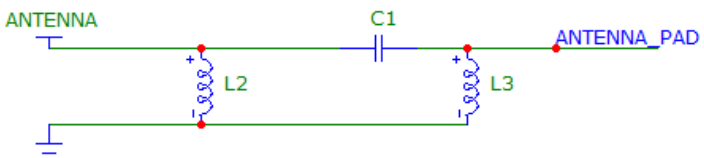

Figure 7-2 Minimal RF Matching Network Circuitry

To reuse Telit's FCC certification for our module, the antenna on the application board shall have a gain equal or lower to the one recommended by Telit, the separation distance between the user and/or bystander and the device's radiating element must be greater than 20cm and no other radiating element must be present inside the application closer than 20cm to our antennas. However, a separate test for any other radiating element could be necessary.

For external antenna, it is recommended to use T-AT9552 antenna from ATEL-ANTENNAS which is a WLAN, dual band 2.4-5.8GHz with SMA M and has a Gain of 2.5 dBi at 2400 ÷ 2500MHz and 4.5 dBi at 4900 ÷ 5925MHz.

NOTE – For PCB antenna reference design refer to "*WL865E4-P PCB Antenna Integration Application Note*".

7.2.2. RF Design Guidelines

- The WL865E4-P module provides a 50Ω antenna pad, which must be routed to the antenna connector (or the integrated antenna) with a transmission line
- Keep as close as possible to 50Ω impedance in the RF track, including the RF Pad.
- To avoid step impedance, make RF trace equal or wider than the Pad width
- The antenna line must be as short as possible, maintain a constant cross-section, avoid any stubs, sharp bends, and meanders.
- Eliminate the right angle on your antenna waveguide design. It can be isolated from any other noise source such as trace will not be crossed by other lines in adjacent layers. Instead, a continuous ground plane is recommended under the antenna trace, and a ground via curtain should connect it to the coplanar ground planes.
- The size depends on the stack up and on the structure that you are going to realize.

For example, the details of the antenna trace on the WL865 interface board are described below.

1. Select a Grounded Coplanar Waveguide (G-CPW) line. This G-CPW transmission line ensures good impedance control and can be implement in an outer PCB layer.
2. Use a SMA female connector to feed the line.
3. The interface board is realized on a FR4, 4-layers PCB. Substrate material is characterized by relative permittivity εr = 4.6 ± 0.4 @ 1 GHz, TanD= 0.019 ÷ 0.026 @ 1 GHz.

Figure 7-3 and Figure 7-4 demonstrates an example of a waveguide having the same width as the RF Pad.

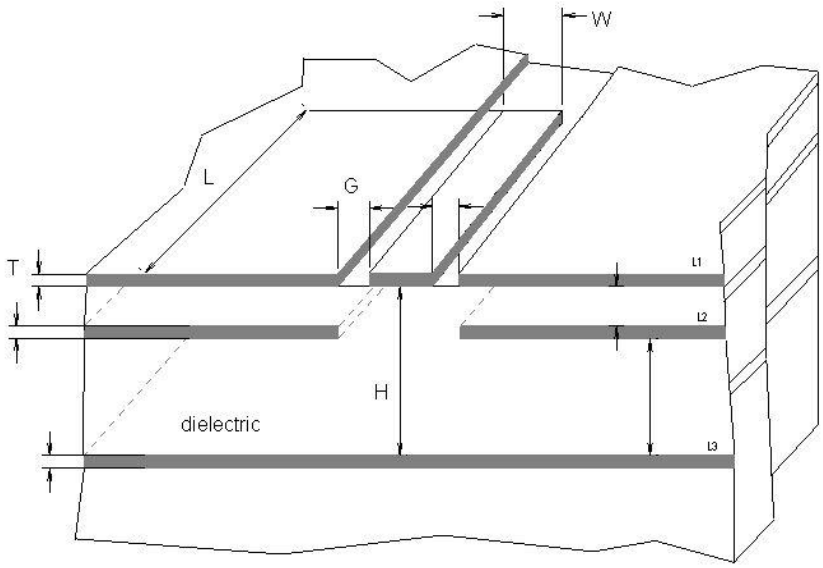

Figure 7-3 Coplanar Waveguide Dimensioning Example

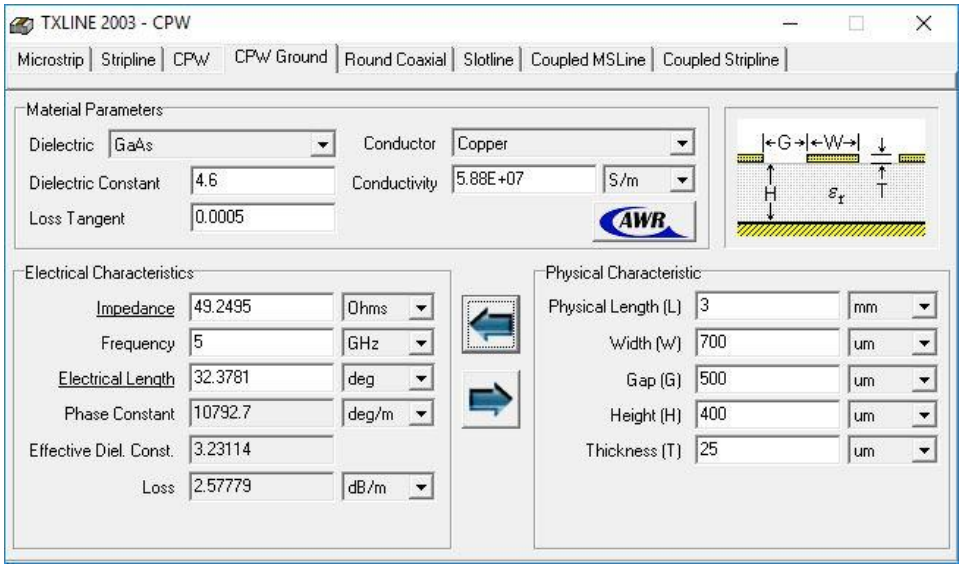

Figure 7-4 Coplanar Waveguide Calculation Tool Example

4. The GND plane must be cut close to the Antenna pad, otherwise the impedance value can change drastically.

The following example demonstrates the RF track used in the WL865E4-P EVB design.

Note: Keep an appropriate clear area from RF PAD to GND on your board.

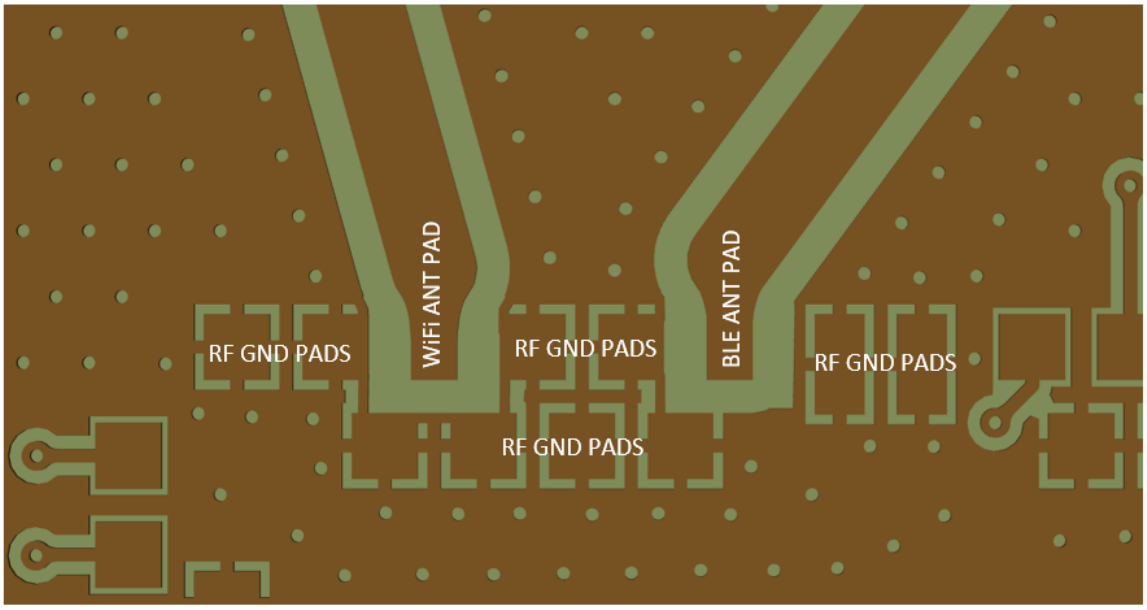

Figure 7-5 RF Track on EVB

8. AUDIO SPECIFICATIONS

8.1. Electrical Characteristics

The digital audio data interface supports I2S. The voltage of these interface pins have the same electrical characteristics as the digital pins and are related to the power bank VDD_VIO.

Since, many external processors and applications have fast transient signals, it is recommended to add an RC filter on all DVI lines (R~22Ohm and C~10nF). If the DVI lines, I2S, are run on external layers it is possible that RF will disturb the lines, to resolve this, add in parallel, to 10nF, another capacitor of about 10pF to 33pF.

9. MECHANICAL DESIGN

9.1. Mechanical Dimensions

The WL865E4-P overall dimensions are:

- Length: 24.4 mm
- Width: 24.4 mm
- Thickness: 2.6 mm
- Weight: 3.23 g

9.2. Mechanical Drawing

9.2.1. Top View

Figure 9-1 shows the mechanical Top view of the WL865E4-P module.

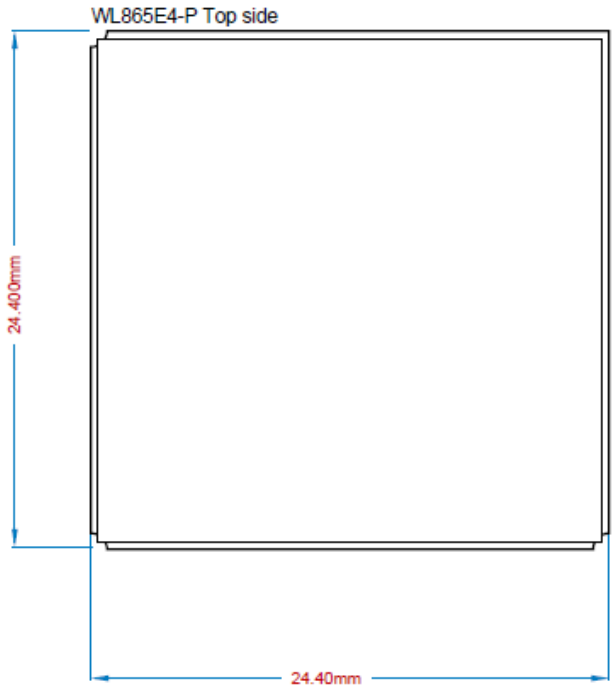

Figure 9-1 WL865E4-P Module - Top View

9.2.2. Bottom View

Figure 9-2 shows the mechanical Bottom view of the WL865E4-P module.

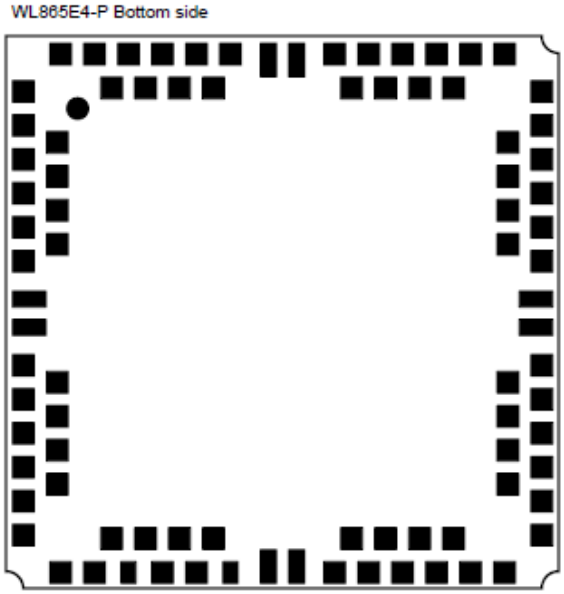

Figure 9-2 WL865E4-P Module - Bottom View

9.2.3. Side View

Figure 9-3 shows the mechanical Side view of the WL865E4-P module.

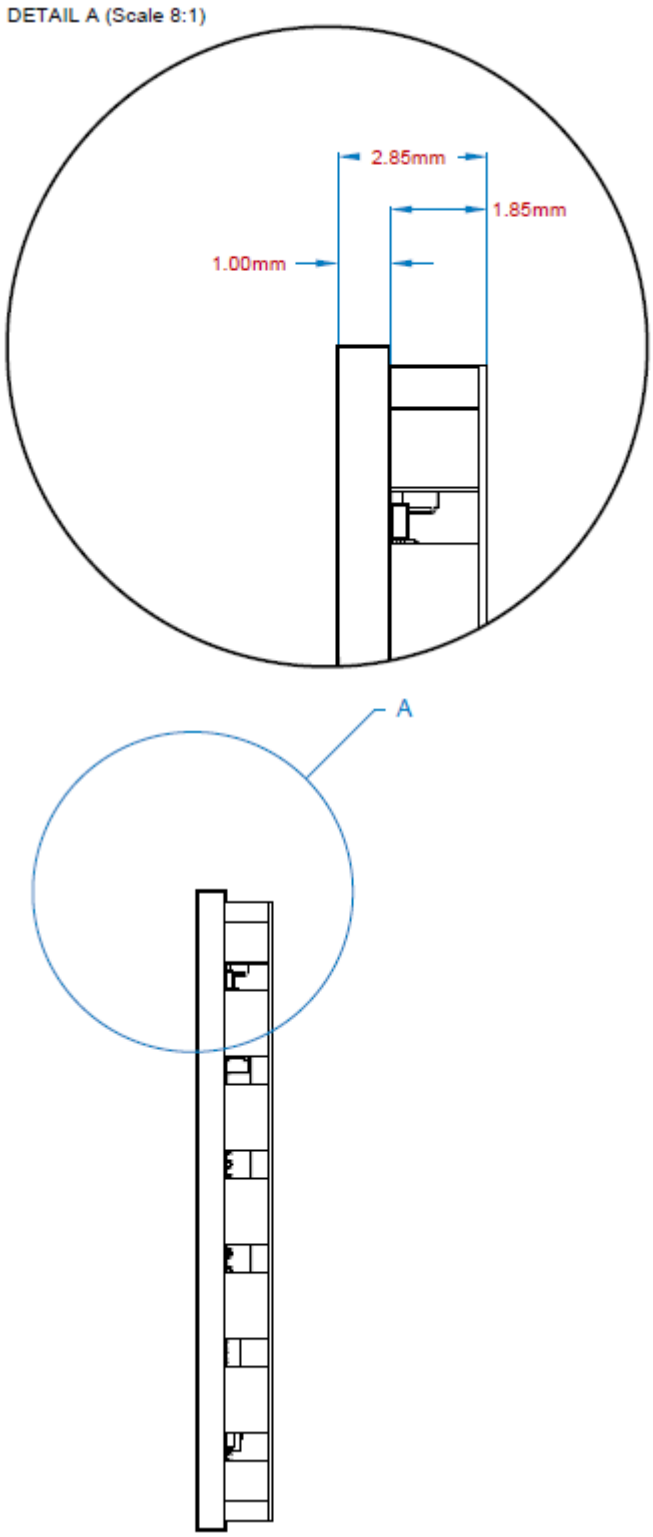

Figure 9-3 WL865E4-P Module - Side View

10. APPLICATION PCB DESIGN

10.1. PCB Footprint

Figure 10-1 shows the recommended PCB footprint.

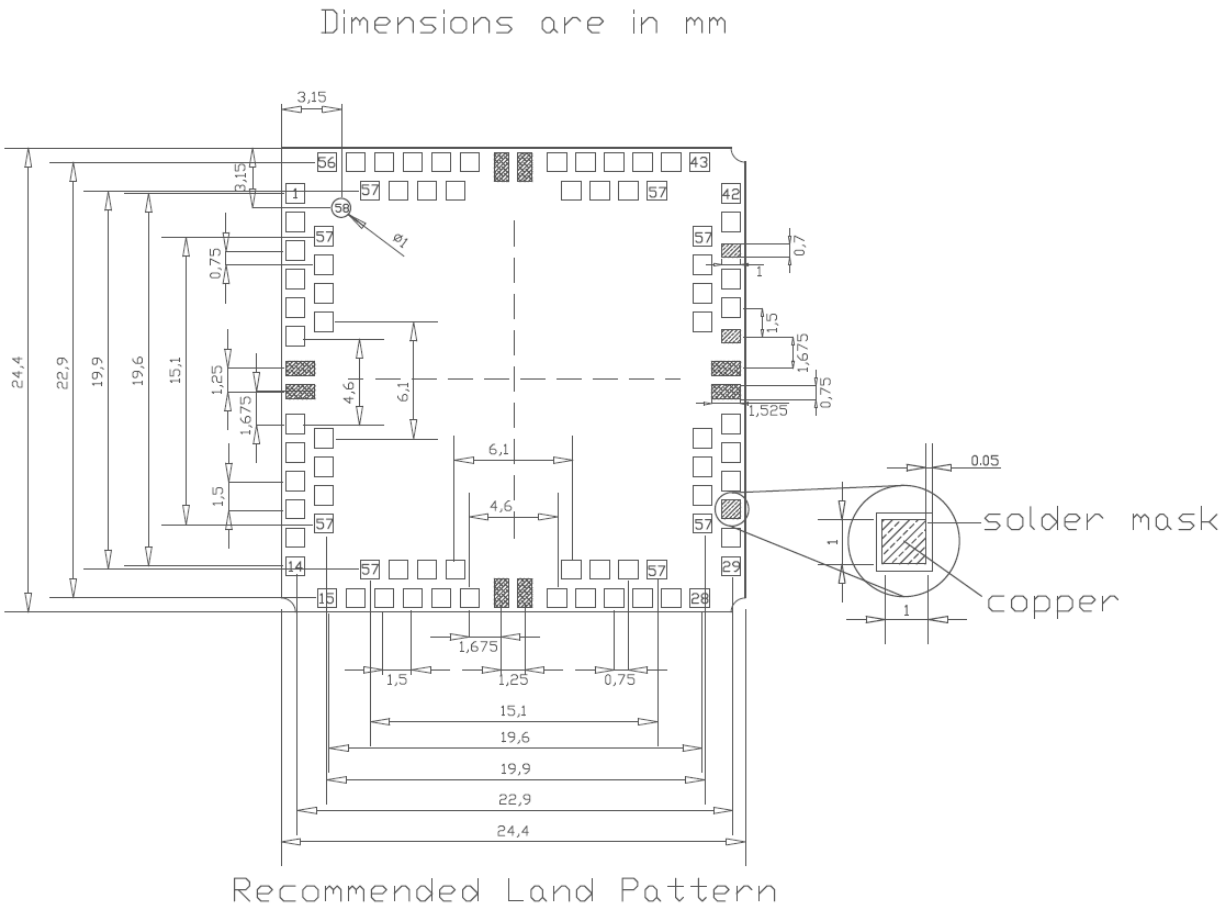

Figure 10-1 WL865E4-P Recommended Footprint

10.2. PCB Pad Design

For the solder pads, it is recommended to use Non-Solder Mask Defined pad (NSMD) on the PCB.

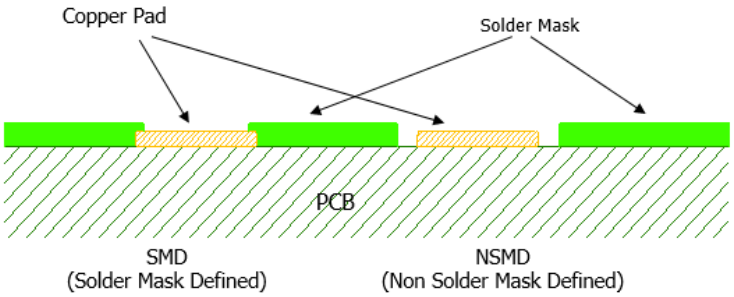

Figure 10-2 SMD and NSMD Pad

10.3. PCB Pad Dimensions

It is not recommended to place via or micro-via not covered by solder resist in an area of 0.3 mm around the pads unless it carries the same signal of the pad itself as shown below.

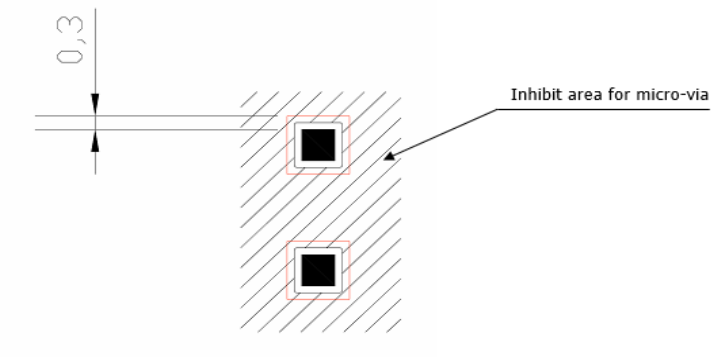

Figure 10-3 Inhibit Area for not Solder Covered Vias

The holes in pad are allowed only for blind holes and not for through holes. Table 10-1 shows the recommended PCB pad surfaces

Finish	Layer thickness [µm]	Properties
Electro-less Ni / Immersion Au	3 –7 / 0.03 – 0.15	Good solderability protection, high shear force values

Table 10-1 PCB Finishing Recommendation

The PCB must be able to resist the higher temperatures which can occurs during the lead-free process. This issue should be discussed with the PCB-supplier. Generally, the wettability of tin-lead solder paste on the described surface plating is better compared to lead-free solder paste.

It is not necessary to panel the application PCB. However, it is recommended to use milled contours and predrilled board breakouts; scoring or v-cut solutions are NOT recommended.

10.4. Stencil

Stencil's apertures layout can be the same as the recommended footprint (1:1). It is recommended to use a stencil foil with thickness ≥ 120 µm.

10.5. Solder Paste

	Lead free
Solder paste	Sn/Ag/Cu

Table 10-2 Recommended Solder Paste Type

To avoid or minimize the cleaning efforts after assembly, it is recommended to use a "no clean" solder paste.

10.6. Solder Reflow

Figure 10-4 and Table 10-3 shows the recommended solder reflow profile.

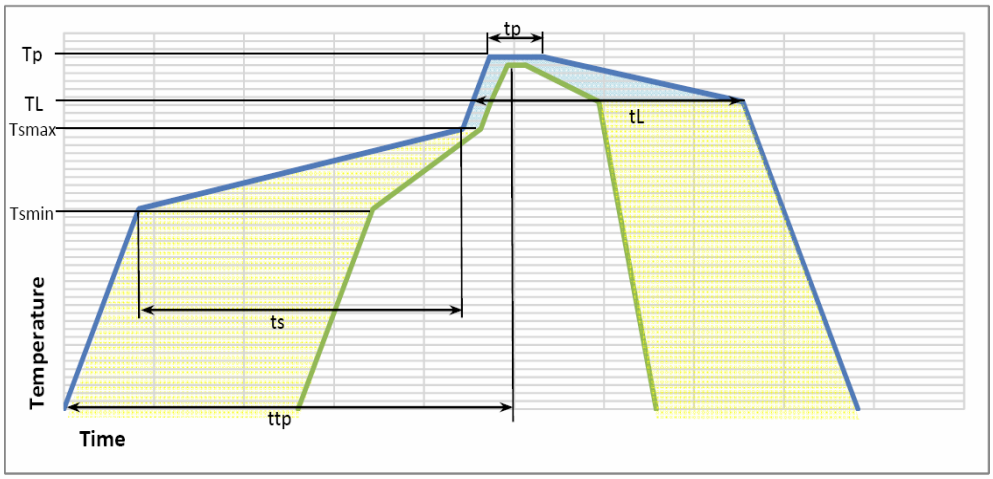

Figure 10-4 Solder Reflow Profile

Profile Feature	Pb-Free Assembly
Average ramp-up rate (T_L to T_p)	3 °C/second max.
Preheat • Temperature Min. (T_{smin}) • Temperature Max. (T_{smax}) • Time (min to max) (t_s)	 150 °C 200 °C 60-180 seconds
T_{smax} to T_L • Ramp-up rate	 3 °C/second max
Time maintained above: • Temperature (T_L) • Time (t_L)	 217 °C 60-150 seconds
Peak temperature (T_p)	245 +0/-5 °C
Time within 5 °C of actual peak temperature (t_p)	10-30 seconds
Ramp-down rate	6 °C/second max.
Time 25 °C to peak temperature	8 minutes max.

Table 10-3 Solder Reflow Table

All temperatures refer to topside of the package, measured on the package body surface.

WARNING:

The WL865E4-P module withstands only one reflow process.

The above solder reflow profile represents the typical SAC reflow limits and does not guarantee adequate adherence of the module to the customer application throughout the temperature range. Customer must optimize the reflow profile depending on the overall system considering such factors as thermal mass and warpage.

11. PACKAGING

11.1. Tray

The WL865E4-P modules are packaged on trays of 50 pieces each when small quantities are required (i.e. for test and evaluation purposes).

These trays are not designed for use in SMT processes for pick and place handling.

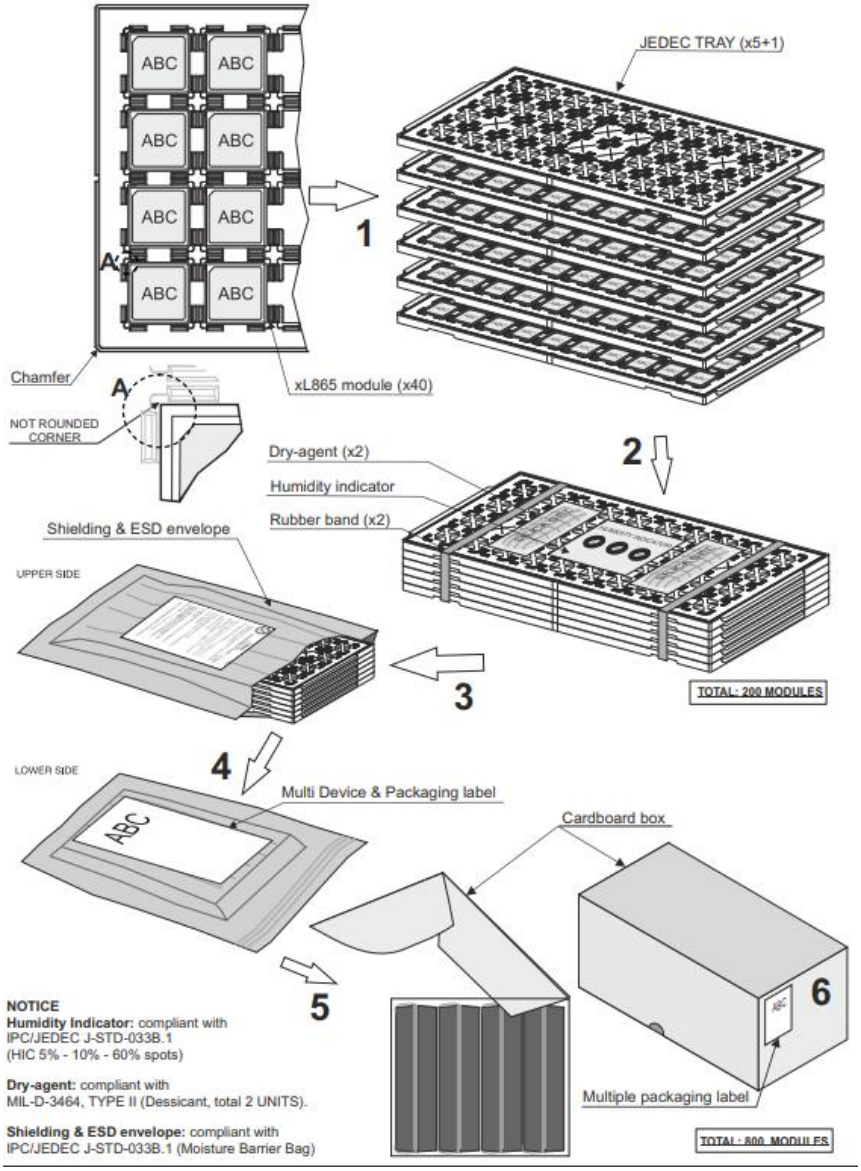

Figure 11-1 WL865E4-P Packaging

WARNING:

The maximum temperature for these trays shall not exceed 65°C.

11.2. Moisture Sensitivity

The WL865E4-P module is classified as a LEVEL 3 moisture sensitive device in accordance with IPC/JEDEC J-STD-020.

Moreover, the customer must take care of the following conditions:

a) The shelf life of the product inside the dry bag is 12 months starting from the bag seal date, when stored in a non-condensing atmospheric environment of < 40°C and < 90% relative humidity (RH).

b) Environmental condition during the production: <= 30°C / 60% RH according to IPC/JEDEC J-STD-033B.

c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours, if condition b) “IPC/JEDEC J-STD-033B paragraph §5.2” is respected.

d) Baking is required if conditions b) or c) are not respected

e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more.

12. CONFORMITY ASSESSMENT ISSUES

12.1. European Directive 2014/53/EU

Hereby, Telit Communications S.p.A declares that the WL865E4-P Module is in compliance with Directive 2014/53/EU.

The full text of the EU declaration of conformity is available at the following internet address: http://www.telit.com\red.

12.2. FCC/IC Compliance

Hereby, Telit Communications S.p.A declares that the WL865E4-P Module is in compliance with:

- USA: Applicable parts of the Title 47 of the Code of Federal Regulations (CFR);
- Canada: Radio Standard Procedure RSP-100, applicable Radio Standards Specifications (RSS).

  Note: In Canada, the device won't operate in the frequency range 5600 – 5650 MHz (channels within this range won't be used)"

Modification statement

Telit has not approved any changes or modifications to this device by the user. Any changes or modifications could void the user's authority to operate the equipment.

Telit n'approuve aucune modification apportée à l'appareil par l'utilisateur, quelle qu'en soit la nature. Tout changement ou modification peuvent annuler le droit d'utilisation de l'appareil par l'utilisateur.

Interference statement

This device complies with Part 15 of the FCC Rules and Industry Canada licence-exempt

RSS standard(s). Operation is subject to the following two conditions:

(1) this device may not cause interference, and

(2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes :

(1) l'appareil ne doit pas produire de brouillage, et

(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Wireless notice

This device complies with FCC/ISED radiation exposure limits set forth for an uncontrolled environment and meets the FCC radio frequency (RF) Exposure Guidelines and RSS-102 of the ISED radio frequency (RF) Exposure rules. This transmitter must not be co-located

or operating in conjunction with any other antenna or transmitter. The antenna should be installed and operated with minimum distance of 20 cm between the radiator and your body.

Le présent appareil est conforme à l'exposition aux radiations FCC / ISED définies pour un environnement non contrôlé et répond aux directives d'exposition de la fréquence de la FCC radiofréquence (RF) et RSS-102 de la fréquence radio (RF) ISED règles d'exposition. L'émetteur ne doit pas être colocalisé ni fonctionner conjointement avec à autre antenne ou autre émetteur. L'antenne doit être installée de façon à garder une distance minimale de 20 centimètres entre la source de rayonnements et votre corps.

FCC Class B digital device notice

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation.

This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.

- Increase the separation between the equipment and receiver.

- Connect the equipment into an outlet on a circuit different from that to which the

receiver is connected.

- Consult the dealer or an experienced radio/TV technician for help.

CAN ICES-3 (B) / NMB-3 (B)

This Class B digital apparatus complies with Canadian ICES-003.

Cet appareil numérique de classe B est conforme à la norme canadienne ICES-003.

List of applicable FCC rules

Parts 15C, 15E, 2.1091

Limited module procedures

N/A

Trace antenna designs

See 6.4 Antenna design

Antennas

This radio transmitter has been approved by FCC and ISED to operate with the antenna types listed below with the maximum permissible gain indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Type Max Gain

Omnidirectional 2.5dBi@2.4GHz band and 4.5dBi@5GHz band.

Le présent émetteur radio a été approuvé par ISDE pour fonctionner avec les types d'antenne énumérés ci-dessous et ayant un gain admissible maximal. Les types d'antenne non inclus dans cette liste, et dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

Type Gain maximal

Omnidirectional 2.5dBi@2.4GHz band and 4.5dBi@5GHz band

Label and compliance information

The product has a FCC ID label on the device itself. Also, the OEM host end product manufacturer will be informed to display a label referring to the enclosed module. The exterior label will read as follows: “Contains Transmitter Module FCC ID: RI7WL865E4” or “Contains FCC ID: RI7WL865E4”.

Information on test modes and additional testing requirements

The module has been evaluated in mobile stand-alone conditions. For different operational conditions from a stand-alone modular transmitter in a host (multiple, simultaneously transmitting modules or other transmitters in a host), additional testing may be required (collocation, retesting…).

If this module is intended for use in a portable device, you are responsible for separate approval to satisfy the SAR requirements of FCC Part 2.1093 and IC RSS-102.

Additional testing, Part 15 Subpart B disclaimer

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the

grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed. The end product with an embedded module may also need to pass the FCC Part 15 unintentional emission testing requirements and be properly authorized per FCC Part 15.

The transmissions are controlled by the application software in the module. The application software ceases to trigger transmissions in case of either absence of information to transmit or operational failure occurs.

Therefore, the device is in compliance with FCC section 15.407 (c) requirements.

13. SAFETY RECOMMENDATIONS

13.1. Read Carefully

Be sure the use of this product is allowed in the country and in the environment required. The use of this product may be dangerous and has to be avoided in the following areas:

- Where it can interfere with other electronic devices in environments such as hospitals, airports, aircrafts, etc.
- Where there is risk of explosion such as gasoline stations, oil refineries, etc. It is the responsibility of the user to enforce the country regulation and the specific environment regulation.

Do not disassemble the product; any mark of tampering will compromise the warranty validity. We recommend following the instructions of the hardware user guides for correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to be conformed to the security and fire prevention regulations. The product has to be handled with care, avoiding any contact with the pins because electrostatic discharges may damage the product itself. Same cautions have to be taken for the SIM, checking carefully the instruction for its use. Do not insert or remove the SIM when the product is in power saving mode.

The system integrator is responsible for the functioning of the final product; therefore, care has to be taken to the external components of the module, as well as any project or installation issue, because the risk of disturbing the GSM network or external devices or having impact on the security. Should there be any doubt, please refer to the technical documentation and the regulations in force. Every module has to be equipped with a proper antenna with specific characteristics. The antenna has to be installed with care in order to avoid any interference with other electronic devices and has to guarantee a minimum distance from the body (20 cm). In case this requirement cannot be satisfied, the system integrator has to assess the final product against the SAR regulation.

The European Community provides some Directives for the electronic equipment introduced on the market. All of the relevant information is available on the European Community website:

http://ec.europa.eu/enterprise/sectors/rtte/documents/

The text of the Directive 99/05 regarding telecommunication equipment is available,

while the applicable Directives (Low Voltage and EMC) are available at:

http://ec.europa.eu/enterprise/sectors/electrical/

14. ACRONYMS

TTSC	Telit Technical Support Centre
USB	Universal Serial Bus
HS	High Speed
DTE	Data Terminal Equipment
UMTS	Universal Mobile Telecommunication System
WCDMA	Wideband Code Division Multiple Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
UART	Universal Asynchronous Receiver Transmitter
HSIC	High Speed Inter Chip
BLE	Bluetooth low energy
SPI	Serial Peripheral Interface
ADC	Analog – Digital Converter
DAC	Digital – Analog Converter
PWM	Pulse Width Modulation
I/O	Input Output
GPIO	General Purpose Input Output

CMOS	Complementary Metal – Oxide Semiconductor
MOSI	Master Output – Slave Input
MISO	Master Input – Slave Output
CLK	Clock
MRDY	Master Ready
SRDY	Slave Ready
CS	Chip Select
RTC	Real Time Clock
PCB	Printed Circuit Board
ESR	Equivalent Series Resistance

15. DOCUMENT HISTORY

Revision	Date	Changes
0	2017-12-15	First issue
1	2019-03-29	General Review of all chapters
2	2019-05-01	Minor changes
3	2019-07-02	Updated GPIO and RF tables
4	2019-08-08	Added FCC/IC COMPLIANCE
5	2019-10-11	Added Power Supply Design Rules Updated RF tables Added Current Consumption in Power Saving Added description for Bootloader and JTAG Updated chapter 2 Product Description with WL865E4- P module features and a block diagram Minor editorial changes and restructuring of the document
6	2019-10-21	New version for BT current consumption measurements
7	2019-11-08	Updated section 4.2 Power Consumption with Wi-Fi and BLE current consumption measurements Added mechanical dimensions of the WL865E4-P module Updated Canada regulatory compliance information

SUPPORT INQUIRIES

Link to **www.telit.com** and contact our technical support team for any questions related to technical issues.

www.telit.com

Telit Communications S.p.A.
Via Stazione di Prosecco, 5/B
I-34010 Sgonico (Trieste), Italy

Telit IoT Platforms LLC
5300 Broken Sound Blvd, Suite 150
Boca Raton, FL 33487, USA

Telit Wireless Solutions Inc.
3131 RDU Center Drive, Suite 135
Morrisville, NC 27560, USA

Telit Wireless Solutions Co., Ltd.
8th Fl., Shinyoung Securities Bld.
6, Gukjegeumyung-ro8-gil, Yeongdeungpo-gu
Seoul, 150-884, Korea

Telit Wireless Solutions Ltd.
10 Habarzel St.
Tel Aviv 69710, Israel

Telit Wireless Solutions
Technologia e Servicos Ltda
Avenida Paulista, 1776, Room 10.C
01310-921 São Paulo, Brazil

[01.2017]

Mod. 0805 2017-01 Rev.6